OVERVIEW

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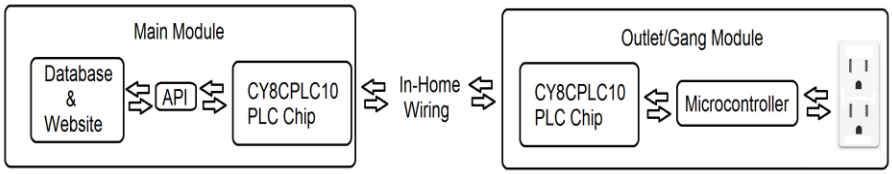
POWER LINE COMMUNICATION

The Power Management System consists of a centralized database that receives usage data from outlet modules, as well as sending commands to them. Without a reliable form of communication between the outlets and the main module, the system cannot perform it's designated roll. Thus it was vital to investigate the possibilities when incorporating PLC in the design.



RISK SPECIFICATION

Marketing Requirements

1. The system shall allow for control of individual outlets.
2. The system shall be safe.
3. The system shall have low cost in comparison to competitive products.
4. The system shall be of reasonable size in comparison to existing systems.
5. The system shall communicate usage data and commands between outlets and the main module.

RISK SPECIFICATION

Engineering Specifications

Marketing requirements	Engineering Requirements	Justification
3	A. Production cost should not exceed $200 for the main unit and $50 for the outlet modules.	This is based upon analysis of a competitive market and current design requirements.
2	B. Control circuits shall be isolated from power line by 1250V RMS minimum.	Electrical isolation is required by safety agencies for equipment connected to the AC power line.
2	B. The system shall use only UL recognized components.	Safety agency approvals will be required to sell product commercially.
4	B. The system shall be able to fit into current standard electrical outlets.	To be fully integrated and competitive, the system must be able to replace current outlets.
1,5	B. Wall units shall be identifiable.	This allows the system to know what information is coming from what wall unit and to provide individual control.
1,5	B. All modules should be able to transmit at a BPS rate sufficient to relay commands and usage data at the chosen sampling frequency.	In order to have reliable communication, the modules must have an adequate minimum communication rate.

RISK INVESTIGATION

Power Line Communication:

- "Mature" Technology -> Find a chip that provides target BPS
- The "right" chip will incorporate collision handling
- Frequency will be predetermined by chips, and will avoid low harmonics of 60 hz

Goal is to find a chip that meets our data rate requirement, which will hopefully handle collisions.

RISK INVESTIGATION

Transmission of Power Measurements:

1) Power (Watt value)
2) Voltage, Current, and Power Factor

Single Component Power:
$B > M * (P + [[log_2(M)]] + Power) * (F_D)$

Triple Component Power:
$B > M * (P + [[log_2(M)]] + V + I + PF) * (F_D)$

M=Modules or Outlets, P=Extra Packet Info, []=Optional ID, F_D=Transmission Frequency

Estimate for SP, M=100, P=0, ID=8 Bits, Pow=14 Bits, F_D=10 : 22000 bps

RISK INVESTIGATION

Complexity Differences

Part	Packet Bits	Provided Data Rate	Collision Provisions	Interface
CY8CPLC10	56	2400	Yes	I2C
CY8CPLC20	56	2400	Yes	I2C, UART
ST7540	0	4800	No	UART/SPI
ST7570	112-336	2400	Yes	UART
ST7590		128000	Yes	UART/SPI
MAX2992		300000	Yes	UART/SPI
ATSAM4CP16B		128000	Yes	UART/SPI
TDA5051A	0	1200	no	Digital

RISK MITIGATION

Avoiding complex chips requires reduction of data sent

Transmission Frequency Options:

1) All transmit real time (> once per second)
2) All transmit slowly (< once per second)
3) Hybrid (Real time & Sub real time)

Combine Power Measurement per gang, not per outlet (1/2 data)

- Separate On/Off

RISK MITIGATION

Further, can reduce bits sent for each power component.

SP: 14 bits of precision too high – perhaps 11

TP: V: 5-6 bit measure from 100 V, I:10-11 bits, PF:5-6 bits

New Equations:

SP: $B>(MF_D+M_RF_R-M_RF_D)*(P+[[log_2(M)]]+Power)$

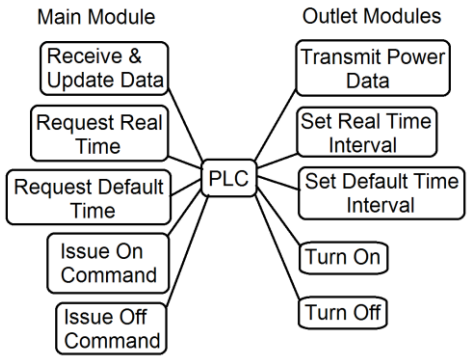
TP: $B>(MF_D+M_RF_R-M_RF_D)*(P+[[log_2(M)]]+V+I+PF)$

Assuming CY8CP10/20 (p=56), new bit values, and M_R(modules)=5,

SP: 536 bps (out of 2400)

TP: 632 bps (out of 2400)

RISK MITIGATION



RISK MITIGATION

While the CY8CPLC10/20 Chip has not been chosen yet, it is a balanced chip:

- 28 Pins (between 16&48) making it middle ground for size/routing concerns
- Full Collision handling means no compromise
- Adequate speed for maintained real time statistics given modifications

Options for circuit coupling are transformer vs capacitive coupling, which will be decided based on microcontroller's coupling. (loss of isolation advantage if using a transformer when the microcontroller isn't)

TESTING

Vital to choose & test chip(s) as soon as possible.

At least four phases of testing recommended

1) Microcontroller & PLC
2) (Microcontroller & PLC)x2
3) Full unit test, test sending commands to relay/switch, etc
4) Completion Tests

UNCERTAINTIES

Coupling Circuitry (Determined by microcontroller)

PLC chip choice

- Smaller chip is more easily integrated, but doesn't leave huge speed margin
- Examination of number of pins vs routing complexity
- Chip prices

Fit within single gang box, or require 2?

REFERENCES

A special thanks to Dr. Kwasinski for his support & advice.

Datasheets:

http://www.cypress.com/?docID=45757

http://www.cypress.com/?docID=50840

http://www.st.com/web/en/resource/technical/document/datasheet/CD00096923.pdf

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Application Notes:

http://www.cypress.com/?docID=46702

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