Energy Management System

A modular solution for power monitoring and management for homes and small businesses

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1 OVERVIEW

1.1 NEEDS STATEMENT

Many homeowners and businesses are not aware of their power usage habits. This lack of awareness leads to potentially inefficient power usage. Existing products are either too expensive or do not include all functionality, such as the ability to remotely control, monitor, and manage power consumption. A system is needed to allow for monitoring and basic management of a home's or business's power usage for a reasonable price.

1.2 OBJECTIVE STATEMENT

The objective of this project is to design and prototype a system that will provide intuitive monitoring and control of power consumption within a residential or light commercial building. The user may track past usage data, as well as control and schedule the operation of all connected electrical loads. The outcome of the project will be the development of a limited scale proof-of concept prototype.

1.3 DESCRIPTION

The Energy Management System is designed to allow homeowners and businesses to easily monitor and manage their power usage. The system primarily consists of two module types, as shown in Figure 1: the main module and numerous separate remote outlet modules. The main module can be installed anywhere in the building, while the outlet modules should replace current outlets in their electrical boxes. Each outlet module consists of a DE-0 Nano with an onboard Cyclone IV FPGA that uses a hall-effect sensor to measure current, an optically isolated amplifier using sigma-delta modulation to measure voltage, and a TRIAC to allow the outlet load to be switched on and off. The FPGA uses I2C to control a power line communication chip, which enables communication with the main module across existing power lines. Through this medium, the FPGA periodically sends power, voltage, and current measurements at varying rates specified by the main module, whereas the main module might send commands for operation back to the FPGA. The main module is a Raspberry Pi 2 connected to the counterpart PLC chip. The Raspberry Pi 2 hosts a Java web application that users can use to not only view usage in the forms of graphs, but also to control the current limit, measurement rate, and whether an outlet is on/off (both remotely and through a schedule). To manage the data, the Raspberry Pi 2 records the power usage information in a MySQL database and compresses it periodically. The result is a modular system that combines many of the best remote monitoring and management features, relatively low price in production, ease of installation, and device safety.

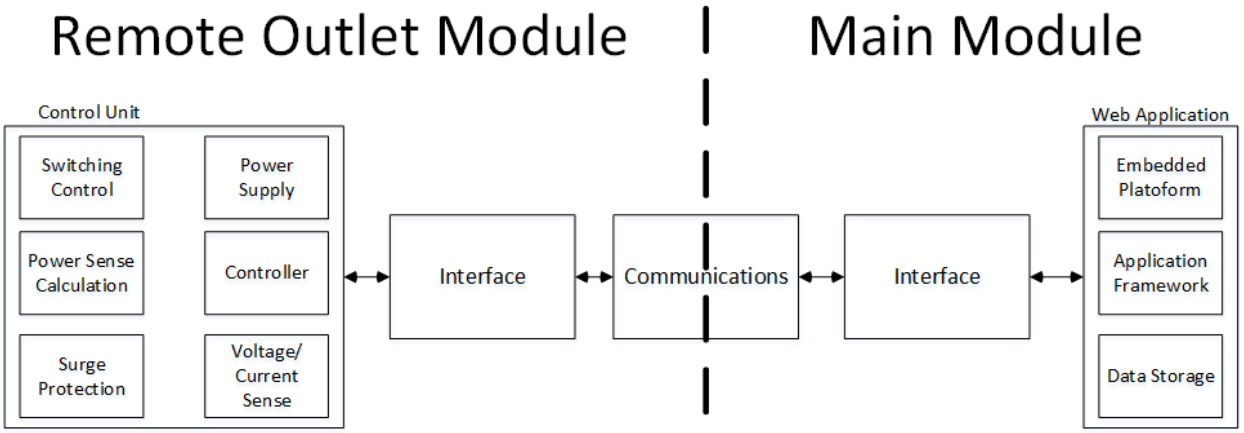


Figure 1. Energy Management System Top Level Diagram

1.4 MARKETING PICTURE

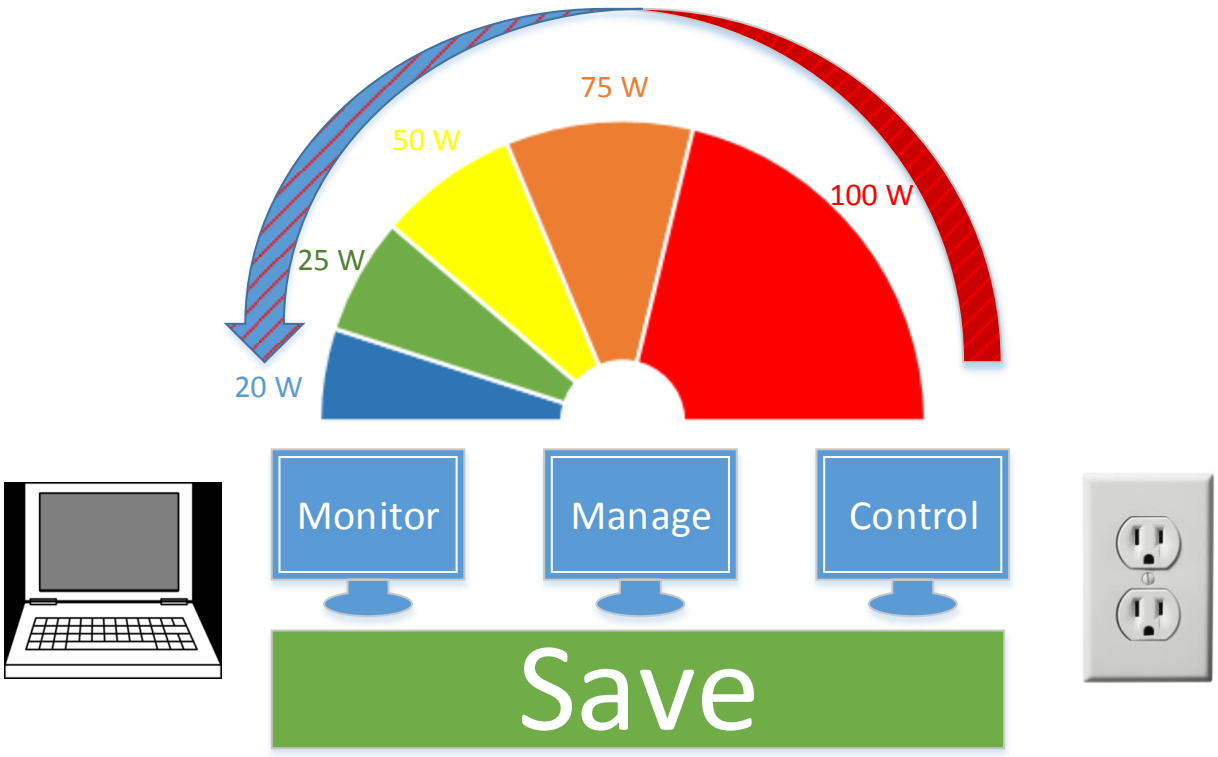


Figure 2. Marketing Diagram

2 REQUIREMENTS SPECIFICATION

2.1 MARKETING REQUIREMENTS

1. The system shall accurately monitor power consumption.
2. The system shall allow for control of whether a single gang of outlets is powered.
3. The system shall allow for a schedule to turn gangs on and off automatically.
4. The system shall be safe.
5. The system shall provide intuitive visual representations of usage data.
6. The system shall have low cost in comparison to competitive products.
7. The system shall be easy to install by a professional.
8. The system shall have an easy to use interface.
9. The system shall be of reasonable size in comparison to existing systems.
10. The system shall consume minimal power.
11. The system shall communicate usage data and commands between outlets and the main module.

2.2 ENGINEERING REQUIREMENTS

Marketing requirements	Engineering Requirements	Justification
6	A. Production cost shall not exceed $200 for the main unit and $50 for the outlet modules.	This is based upon analysis of a competitive market and current design requirements.
7	B. Installation time of an outlet module within an electrical box shall not exceed 30 minutes during typical installation.	Using a professional electrician, the outlets can be installed within this time frame.
4	C. The system shall survive a 2500V impulse voltage per IEC-60664-1.	This will prevent devices from being damaged due to transient spikes on the power line.
4	D. Control circuits shall be isolated from power line by 1250V RMS minimum.	Electrical isolation is required by safety agencies for equipment connected to the AC power line.
1	E. The control unit shall be capable of varying the load power from 0 to full power for resistive loads.	Dimming function allows reducing load power consumed for energy savings. This is only applicable for purely resistive loads, (e.g., lightbulbs, heaters, etc.).
1	F. The system shall measure power consumption with an accuracy of ± 10 %	This will allow the system to measure usage accurately enough for the typical user.

1,2,3,5,8	G. A web interface or web application shall allow the monitoring and management of the system.	This will allow a user to be able to manage the system and perform various tasks associated with the system.
8	H. The user shall be able to understand complete system functionality within an hour.	Analysis shows that an intuitive interface should require minimal time to operate.
4	I. The system shall use only UL recognized components.	Safety agency approvals will be required to sell product commercially.
9	J. The system shall be able to fit into current standard electrical outlets.	To be fully integrated and competitive, the system must be able to replace current outlets.
10	K. The system shall have greater than 95% efficiency at maximum rated load.	To achieve energy savings and to avoid excessive heating of the wall units.
2,3	L. Wall units shall be identifiable.	This allows the system to know what information is coming from what wall unit and to provide individual control.
11	M. All modules shall transmit at a BPS rate sufficient to relay commands and usage data at the chosen sampling frequency.	In order to have reliable communication, the modules must have an adequate minimum communication rate.

3 CONCEPT SELECTION

3.1 EXISTING SOLUTIONS

In today's market, there are a variety of solutions available for power usage monitoring and the scheduling and remote control of outlets and other loads (such as lights). A kill-A-Watt meter, such as the P4400, is a pass-through adapter that plugs into a single outlet, and provides advanced information about current power consumption through that outlet. The Kill-A-Watt adapter is quite large, so while it is cost-effective at only $15 per unit, it takes up multiple outlet slots (for usage data of only a single outlet), which makes it less of a full home solution. More advanced Kill-A-watt units also provide graphical analysis of power consumption. Many power companies, such as RGE, will provide web access to usage data for customers. As they have only black box access, the data available show only the power consumption for the entire building (and not per outlet). Additionally, most companies provide only average usage data for a given day, week, or month, without being able to show minute-by-minute usage data.

In the remote control (On/Off) department, radio frequency units that replace outlets inside their electrical boxes (such as WC-6015-WH at $20/unit) are another viable option. The replaced outlet gang consists of one outlet that may be controlled via a remote radio controller, and an outlet that

is always on. These RF outlets provide no power measurement data, and provide only local control with the use of a remote. The Belkin WeMo units are similar in structure to the Kill-A-Watt meter, with a different feature set. The base WeMo modules ($40 and above) are adapters that plug into a wall outlet, and consume more space than a single wall outlet. These modules provide per outlet usage data, and allow the scheduling and remote operation of outlet modules. The WeMo modules do not include surge/overcurrent protection, and have no means to provide graphical analysis of the data.

Finally, complex Lutron systems are able to provide both building and per outlet power consumption data graphically, and allow for both remote and scheduled control of the loads. The primary limitation of the Lutron HomeWorks system is that it is geared almost in its entirety to the operation of only lights and shades. The chart below summarizes the various features provided by the existing solutions.

		Kill-A-Watt	RGE	RF Outlets	Belkin WeMo	Lutron HomeWorks
Power Consumption	Building		✓			✓
	Outlet	✓			✓	✓*
Protection	Overcurrent					
	Surge		✓			
Remote ON/OFF	Local			✓	✓	✓*
	Global				✓	✓*
	Scheduled				✓	✓*
	Graphical Analysis	✓	✓*			✓

* = Limited Domain

If the Lutron HomeWorks solution extended to outlets, its domain would overlap with this project. However, given its high cost and lack of outlet data and control, it is not an appropriate solution. All other modules discussed lack significant required features and are not ideal solutions. While the RF outlets are relatively simple, and could be utilized by a central unit to schedule and control outlets within a home, they would require significant modification in order to provide data acquisition and surge protection. For these reasons, the best solution is to manually create outlet modules that satisfy the project requirements.

The concept selection for the Energy Management System was broken up by sub-module such that relevant concepts could be considered for each subsystem of the Energy Management System.

3.2 SYSTEM ELECTRONICS

The system electronics were broken into the following submodules: power sense circuitry, switching control, surge protection, and AC to DC power rectification. Each submodule of the system electronics was individually surveyed.

3.2.1 AC to DC Conversion Concepts Considered

There are many pre-existing power supplies to generate DC control power from the AC line, which are used in products similar to the Energy Management System. The following provides an overview of solutions considered.

3.2.1.1 Capacitive Coupled Circuit

Capacitive coupled circuits are common in circuits similar in scope to the Energy Management System, for example the popular Kill-A-Watt meters make use of a capacitive coupled circuit. Capacitive coupled circuits are very inexpensive as they consist of only resistors, capacitors and transistors. This type of solution is also relatively small in terms of space, which would make it ideal for a small remote unit. The downfall of this type of circuit is the limited amount of power which it can deliver to the load. Depending on the power to be delivered this may or may not be an issue. For example in the Kill-A-Watt meter the necessary power was very small and was achievable with a capacitive coupled circuit. A capacitive coupled circuit also does not provide any isolation between the digital and power signals, which can be a safety issue.

3.2.1.2 Linear Supply

A 60-Hz transformer along with a bridge rectifier and capacitor is a common option, which would occupy a lot of space. A transformer is also more efficient for signals faster than 60 Hz but is inefficient for a 60-Hz input. One advantage of this solution is it does provide electrical isolation.

3.2.1.3 Switch Mode Supply (Flyback)

Switch mode supplies convert from one voltage level to another by switching a transistor between fully on and fully off at high frequency, typically 50 to 100 kHz, ideally dissipating no power. The output voltage is regulated by the duty cycle, ratio of on time to switching frequency. A high frequency output filter converts the switched waveform to DC, determined by the average value of the switching. Switch mode supplies are more efficient than a linear supply and are often smaller since they do not require a 60Hz transformer. Switch mode supplies also can be purchased as dedicated integrated circuits, which require only a handful of external components. Electrical isolation can be provided by using small high frequency transformers, (e.g., flyback converter).

3.2.2 Surge Protection

Surge protection is needed in modern electrical appliances to protect devices from voltage spikes. Typical voltage spikes, which can be caused by lightning, can damage electronics. Therefore, it is important to implement a method of minimizing transient currents and voltages seen by sensitive electronics. Important specifications, which typically define surge protectors, are clamping

voltage, or the voltage at which unwanted energy is protected from the line, joule rating, which specifies how much energy can be absorbed without failure, and response time, which indicates how fast a device is able to respond in the presence of a spike. Several methods of surge protection are outlined below.

3.2.2.1 Gas Discharge Tube (GDT)

GDTs consist of a device with an enclosed gas, which conducts at certain voltage level. They are able to handle more current than other devices of similar size but have a short life expectancy and are only able to handle only a small number of large transients. GDTs also have a slow response time, and additional suppression components are often needed to fully protect loads.

3.2.2.2 Transient Voltage Suppression (TVS)

TVS solutions provide the fastest response time to voltage spikes but are able to absorb the least amount of energy. Failure of TVS solutions can lead to a permanent short circuit, which results in the bus's being shorted out. TVS circuits are used most frequently in high-speed low power applications such as digital logic.

3.2.2.3 Metal Oxide Varistor (MOV)

MOVs have a low life expectancy when exposed to many transients, and after failure occurs, a partial or complete short circuit can exist. MOVs can become very hot if a failure occurs, and it is often necessary to connect a MOV with a thermal fuse to prevent thermal runaway, which leads to fires and explosions. However, MOVs are the most common surge protector in AC electronics due to their low cost and reasonably good performance. UL recognized MOVs are frequently used in power line surge protection applications.

3.2.2.4 Thyristor Surge Protection Device (TSPD)

A TSPD switches to an on state once a voltage threshold is exceeded with a high current capability of up to 200A. TSPDs have no effect on a circuit during normal operation, and similar to an MOV conduct only during the on state. The on state is triggered by a transient voltage that exceeds the voltage threshold of the device. TSPDs provide high surge current ratings and low device capacitance. TSPDs are used in AC applications, which require high surge current handling. They are not typically found in household appliances.

3.2.3 Switching Control

3.2.3.1 TRIAC

A TRIAC is a PNPN thyristor semiconductor, which is able to conduct current in both directions when it is turned on. TRIACs are commonly used for AC phase control. TRIACs are non-isolated devices, and opto-isolation of the TRIAC gate drive signal would be needed to provide isolation

of control circuits from the AC line. To turn on a TRIAC, it is necessary to apply a positive or negative current to the gate with respect to the main terminal. TRIACs are frequently used in AC switching applications due to their ability to control large currents with small gate current pulses. After triggering via a gate pulse, TRIACs latch on independent of the gate pulse. The line current must go to zero by external means for the TRIAC to turn off. TRIACs can also be false triggered on via high rates of voltage change across their main terminals. Therefore an RC snubber circuit is needed to prevent the TRIAC from turning on due to a voltage transient on the main power line causing a large dV/dt value between the two main terminals of the device. TRIACs are commonly used in light dimmers, and small electrical motors due to the ability to perform bidirectional phase control. Phase control involves sensing the AC line zero crossing and then waiting for an adjustable phase delay before triggering the TRIAC on to control the voltage applied to the load.

3.2.3.2 Relay

A relay is an electromechanical device which functions as a switch. Relays consist of a magnetic winding or coil, which generates a magnetic field when current is passed through it. The field moves an arm of a contact to make or break an electrical connection. The relay coil is electrically isolated from the output contacts. Relays have a delay, on the order of milliseconds, between command and result due to the physical nature of the relay. Relays are available in a wide range of physical sizes and current handling capability, and versions are available for both DC and AC switched circuits. They are a cost effective solution for AC on/off switching, but they cannot provide variable voltage control such as needed for lamp dimming.

3.2.3.3 Transistor

A transistor solution can be realized using BJT or MOSFET transistors. In order to accomplish AC switching, a diode bridge will need to be constructed, with the transistor in the center of the bridge. The diode bridge is required to make the unidirectional transistor capable of controlling AC currents. Also a continuous gate drive is necessary when the switch is to be on. The advantages of a transistor configuration is switching can occur at a high frequency to provide variable load power. Like a TRIAC, a transistor would require an isolated drive signal to provide isolation between the control and power circuits. The diode bridge required would increase physical size and semiconductor power losses versus the TRIAC solution. Unless there is a need for high frequency switching the TRIAC is a better load switch for phase control applications.

3.2.4 Power Sensing

Power sensing needs can be broken into two aspects: current and voltage sensing. A controller will then use the current and voltage measurements to determine various metrics, such as but not limited to average power dissipated, power angle, etc.

3.2.4.1 Current Sensing

3.2.4.1.1 Sampling Resistor

A low ohm resistor can be put in series with the current to sense, and the voltage across the resistor can be measured. Since the value of the resistor and the voltage drop is known, the current can be

determined using Ohms law. A sampling resistor does have a small effect on the load since a small resistor is being added in series with the load. A sampling resistor will also dissipate power. In order to achieve an accurate measurement the sampling resistor must have a tight tolerance.

3.2.4.1.2 Hall Effect Sensor

A Hall effect IC sensor can be used to measure current. Any wire with current traveling through it produces a perpendicular magnetic field. A hall sensor is able to measure the magnetic field and produce an output voltage in relation to the magnetic field. Digital Hall sensors are often used in position sensing applications specifically to determine the rotor position referenced to a stator. Analog Hall sensors are often used in current sensing applications. Many prepackaged Hall effect current sensors are available. These sensors have the advantage of providing electrically isolated current sensing with no power loss.

3.2.4.1.3 Integrated Circuit

An integrated circuit performs current sensing by running the current to be measured into the IC. The integrated circuit typically produces an output such as an analog voltage proportional to the sensed current that can be fed into an ADC and processed by a controller. These current sensing integrated circuits are typically based on Hall effect sensing. They have the advantages of larger Hall effect sensors.

3.2.4.2 Voltage Sensing

A voltage sensor detects the amount of voltage and generates a proportional output signal relative to the sampled voltage. Several possible implementations are examined.

3.2.4.2.1 Differential Amplifier

Differential amplifiers amplify differential signals, and reject signals common to both inputs. By choosing the input and feedback resistors a gain can be obtained such that the sensed voltage is scaled to a range, which can be processed by an ADC. Knowing the gain of the differential amplifier, a controller can determine the input voltage. A differential amplifier does not provide electrical isolation, and therefore with this particular solution the power electronics are isolated only from the control electronics by high impedance. A differential amplifier used for line voltage sensing would have large voltage dividers with very high input resistances to scale the line voltage down to the 3- or 5-volt range required for a microcontroller.

3.2.4.2.2 Optical Isolator

An optical isolation amplifier IC is used to produce an output voltage which is proportional to the input voltage on the other side of the optical isolation barrier. Several optical isolation solutions exist, from simple input LEDs optically coupled to photo diodes or phototransistors to complex ICs with primary and secondary control integrated circuits that then transmit digital signals optically across the isolation barrier. The input voltage is typically resistively divided down such that it is in a pre-defined range of for example 0 to 2V as required by the ACPL-C870-000E part manufactured by Avago.

3.2.5 Controller

A number of manufactures offer low cost microcontrollers intended for electronic watt-hour meter and smart grid applications. Several offer evaluation boards and embedded software for energy management. The main functions of the controller will be to acquire the AC current and voltage values in real-time, perform instantaneous power calculations, determine zero crossings, control the load switch, calculate the voltage to current phase angle, calculate the line frequency, send data through the power line communication interface, and provide overcurrent load shutdown. It is also desirable for the controller to be low power and low cost. The availability of proven design tools and evaluation boards is a factor in controller selection. A minimum of two onboard ADCs is necessary to handle voltage and current conversions. Ideally the two ADCs are able to sample simultaneously. Timers are also necessary to perform frequency calculations. I/O is also needed to allow for status LEDs and load switching. The controller to be selected is highly coupled with the on-going power line communication (PLC) investigation, and therefore controller requirements are subject to change relative to what may be discovered from this separate investigation. An I^2C serial link is required for interface to the PLC module.

3.2.5.1 Texas Instruments – MSP430 Low Power Family

The MSP430 family is a 16-bit microcontroller designed for low cost, and low power applications. The MSP430 base microcontroller provides a 16-bit multiplier, a 16-bit timer, 3 sigma-delta converters (ADCs) which have a dynamic range of 1:2400. Serial interfaces of UART and SPI are also provided which can run at 8-MHz. Eleven I/Os are also available for various applications. The MSP430 also has a small footprint as it comes in a package of 24 pins at a size of 35-50 mm. Development boards and software, including example code, are provided by Texas Instruments. An extensive library of energy metering functions exists and is publicly available.

3.2.5.2 Peripheral Interface Controller (PIC) – PIC16F873A

The PIC16F873A manufactured by Microchip is an 8-bit microcontroller with 5 channels of 10-bit ADC and a synchronous serial port capable of SPI or UART protocols. The PIC comes in a 28-pin package thus allowing it to fit nicely on a small PCB. MPLAB® development tools are also available to support the PIC microcontroller family. The device has been used in power meter applications, and design examples are available.

3.2.5.3 STMicro – STPMXX Family

The STPM family is a group of ICs designed specifically for the application of the measurement of energy in a single-phase system. The STPMXX is highly customized to accomplish the task of energy detection, and therefore additional processing power may be necessary to handle the power line interface circuitry. A good library of energy metering functions exists and is publicly available.

3.2.5.4 DE-0 Nano FPGA Development Board- Altera Cyclone IV FPGA(EP4CE22F17C6N)

The DE-0 nano development board consists of a Cyclone IV FPGA, a 50 MHz oscillator, three GPIO headers, an 8 channel 200 ksps Texas Instruments 12-bit A/D converter, 32MB SDRAM and various other peripherals that will not be needed for the scope of this project. The onboard FPGA contains 22,320 logic elements, 66 embedded multipliers, and 4 phase locked loops. The FPGA provides a large advantage over a standard microprocessor as it will allow for custom design of the necessary digital control circuits. This solution provides the possibility to process data at speeds higher than any other proposed controller solution. The parallel nature of the FPGA also allows for an increased calculation bandwidth. The team also has large amounts of FPGA design and development experience and is more comfortable programming in VHDL than C or C++.

3.2.6 System Electronics Concept Selection

In order to determine the concept selection that best meets the desired functionality Pugh tables were generated. Due to the nature of this investigation, some sub-modules have multiple valid possibilities, and certain uncertainties still exist. The Pugh selection criteria rated design concepts on key characteristics and assigns a +, 0, or – rating for each criteria relative to the other concepts. The ratings are then tallied to rank the different concepts relative to each other. While it is possible to assign different weights to the selection criteria based on their relative importance, in this analysis a simple unweighted approach was used.

3.2.6.1 Power Supply

The Pugh table for the AC to DC power supply is shown in Table 1.

Table 1. Pugh Concept Selection for Power Supply

	Concepts		
Selection Criteria	**Capacitive Coupled Circuit**	**Linear Supply**	**Switch Mode Supply**
Power Delivered	0	+	+
Isolation	-	+	0
Size	+	-	+
Cost	+	-	-
Positive	2	2	2
Neutral	1	0	1
Negative	1	2	1
Net Score	1	0	1
Rank	1	2	1
Continue	Yes	No	Yes

After performing a Pugh analysis, it was determined that both a switch mode supply and a capacitive coupled supply are feasible. A switch mode supply is an easier and more direct solution, but it is much more expensive and takes up more space than a capacitive coupled circuit. Due to the high cost of the switch mode supply, it would not be considered for a production environment, and a capacitive supply comparable to those used in other similar products such as the Kill-a-Watt meter would be used. However, for the first iteration of this project a packaged switch mode controller made by Recom will be selected as it mitigates this risk, at the expense of cost, and will allow the development team to focus on other risks which are not as easily mitigated. A second iteration may be developed with a capacitively coupled power supply, which will provide a vast reduction in cost per unit.

3.2.6.2 Surge Protection

The Pugh table for the surge protection function is shown in Table 2.

Table 2. Pugh Concept Selection for Surge Protection

	Concepts			
Selection Criteria	GDT	TVS	MOV	TSPD
Cost	-	0	+	0
Energy Dissipated	+	-	0	+
Response Time	-	+	0	0
Clamping Voltage	0	0	0	+
Length of Life	-	-	+	0
Positive	1	1	2	2
Neutral	1	2	3	3
Negative	3	2	0	0
Net Score	-2	-1	2	2
Rank	4	3	1	1
Continue	No	No	Yes	No

After performing a Pugh analysis, the MOV and TSPD concepts tied. It was determined that the varistor (MOV) will be placed between line and neutral to handle power surges, because it is the more common solution used in household appliances.

3.2.6.3 Load Switching

The Pugh table for load switching is shown in Table 3.

Table 3. Pugh Concept Selection for Load Switching

	Concepts		
Selection Criteria	TRIAC	Relay	Transistor
Cost	0	0	0
Switching Speed	+	0	+
Isolation	0	+	-
Interfacing	0	0	-
Power Dissipated	+	-	0
Phase Control	+	0	0
Positive	3	1	1
Neutral	3	4	3
Negative	0	1	2
Net Score	3	0	-1
Rank	1	2	3
Continue	Yes	No	No

Based on the results of Pugh analysis, a TRIAC was selected as the concept to be implemented for load switching.

3.2.6.4 Power Sensing

Power sensing was divided into two sub-tasks: current and voltage sensing. With instantaneous current and voltage characteristics, the chosen controller will be able to perform all necessary power calculations.

3.2.6.4.1 Current Sensing

The Pugh Table for current sensing is shown in Table 4.

Table 4. Pugh Concept Selection for Current Sensing

Current Sense

	Concepts		
	Sampling Resistor	Hall Effect Sensor	Integrated Circuit
Effect on circuit	-	+	+
Accuracy	-	0	+
Cost	+	0	0
Positive	1	1	2
Neutral	0	2	1
Negative	2	0	0
Net Score	-1	1	2
Rank	3	2	1
Continue	No	No	Yes

Based on the results of Pugh analysis, an integrated circuit was selected as the concept to be implemented for current sensing.

3.2.6.5 Voltage Sensing

The Pugh Table for voltage sensing is shown in Table 5.

Table 5. Concept Selection for Voltage Sensing

	Concepts	
Selection Criteria	Differential Amplifier	Optical Isolator
Accuracy	0	0
Cost	+	-
Interfacing	0	0
Isolation	0	+
Linearity	+	0
Positive	2	1
Neutral	3	3

Negative	0	1
Net Score	2	0
Rank	1	2
Continue	Yes	No

Based on the results of Pugh analysis, a differential amplifier was selected as the concept to be implemented for voltage sensing.

3.2.6.6 Controller

The Pugh Table for controller selection is shown in Table 6.

Table 6. Concept Selection for Controller

	Concepts			
Selection Criteria	TI MSP430	STMicro	PIC	DE-0
Cost	+	0	+	-
Size	+	+	+	+
Development Tools	+	-	0	+
Development Time	0	0	0	+
Interface	0	0	0	+
Positive	3	1	2	4
Neutral	2	3	3	0
Negative	0	1	0	1
Net Score	3	0	2	3
Rank	2	4	3	1
Continue	Yes	Yes	Yes	Yes

Based on the results of Pugh analysis, the DE-0 Nano development platform was selected as the medium to use as the controller. The teams' familiarity with FPGAs, and VHDL was a strong reason why the DE-0 Nano was selected. However, due to unknown impact of power line communications, continued investigation of the controller choice is expected.

3.3 POWER LINE COMMUNICATION

In order to simplify user setup, to avoid concerns with obstacles such as walls in unknown environments, and to avoid saturating clients' routers with power usage data, power line communication was chosen to communicate between the outlet modules and the main module, which will accumulate power usage data. For operation within a large building, three-phase power would be a concern for this communication. In such a situation, three communication modules may be necessary to ensure the main module is able to communicate with all of the remote outlet modules. However, for the scope of a typical home sized prototype, it is assumed that the modules will all be in phase.

As a mature technology, power line communication (PLC) chips are relatively simple to utilize, and will take care of many of the complex facets of communication automatically. Some of the concerns associated with PLC are interference, data rates, collision handling, and interfacing with the chip. The majority of interference on the main lines of a home occurs at low harmonic frequencies of the base frequency of 60 Hz. The majority of PLC chips account for this by utilizing a much higher frequency than 60 Hz to avoid the issue entirely. While it is possible to manually implement a collision handling protocol, it is far more desirable to purchase a PLC chip with integrated collision handling.

As the communication rate for many modules is specified in a bps format, including the package's header and other transmission information (CRC error detection/repair bits, etc), the necessary transmission rate will depend on the chosen chip. As an estimate, the transmission rate, in bits/sec must at least meet this requirement:

$$B > M * (P[bits] + D[bits]) * (F_s) \quad \textbf{(1)}$$

Where B, M, P, D, and F_s are respectively the minimum supported bitrate of an adequate chip [bits/second], the number of outlet modules, any non-data transmission information (such as packet headers, CRC bits, etc), the number of actual data bits per transmission, and the sampling frequency of a single module. Note that this is merely a minimum requirement – sending commands from the main module will add further data requirements but will be considerably less frequent, and so was not included here. Additionally, resending of data may also impact the necessary transmission rate, but is chip dependent.

Based on Equation 1, if the packet sent consisted of only an 8-bit ID (identifying the outlet out of 200 outlets) and a 14-bit (accurate to 1 mA) power consumption, sampling in real-time at 10 transmissions/second, then the required data rate would be 44000 bits/second. This means for these calculations, any feasible chip would have a transmission rate considerably over 44000 bps. A selection of chips, including chips from STMicroelectronics and Cypress, were then analyzed using this low estimate process, as shown in the chart below. This chart also includes information about the interface utilized for each chip. The column marked "Collision Provisions" indicates whether the chip has collision handling capabilities.

Table 7. Power Line Communication Chip Selection Chart

Part	Packet Bits	Provided Data Rate	Collision Provisions	Interface
CY8CPLC10	56	2400	Yes	I2C
CY8CPLC20	56	2400	Yes	I2C, UART
ST7540	0	4800	No	UART,SPI

ST7570	112-336	2400	Yes	UART
ST7590		128000	Yes	UART,SPI
MAX2992		300000	Yes	UART,SPI
ATSAM4CP16B		128000	Yes	UART,SPI
TDA5051A	0	1200	no	Digital

The results of the comparison are namely that there are two categories of chips being considered. The first category of chips are relatively simple, with few pins, a bigger chip area, and a slower data rate; including chips such as the CY8CPLC10, CY8CPLC20, ST7540, ST7570, and TDA5051A. These chips are less expensive but have an insufficient data rate considering the estimation made using Equation 1.

The second category of chip has a smaller surface area with a higher density of pins, usually incorporating a method to handle collisions, and even provide programmability. Many of these chips have 50 or 100 pins, which make them a concern for routing on a PCB.

Based on these considerations, the primary decision was to utilize a "simple" chip that also handles collisions, if the data rate can be reduced enough to allow it to be used. If the data rate is not reducible, then a more complex and expensive chip must be utilized. The Cypress CY8CPLC20 was chosen due to the fact that there were development boards available to the team.

3.4 WEB APPLICATION

There were two main concepts that needed to be considered when thinking about building the web application. The first was which embedded platform to use and the other was how to serve (or host) the application and which, if any, framework to use to aid in the building of the application. Both of these elements were important and would affect the overall design and functionality of the application. When deciding which embedded platform to use and how to serve the application, each element was looked at separately and a separate decision was made for each.

3.4.1 Embedded Platform

When considering the embedded platform it was first decided that the project requires a platform that is very easy to set up and get connected to the network, has enough computing power to serve a fluid application and host a database, is easy to develop on and make changes to, and is relatively small and low power. We decided to go with an embedded platform that runs a variation of Linux to allow for the ease of setup, computing power, and flexibility. This narrowed the search down to two competing products, the BeagleBone Black and the Raspberry Pi 2. Both of these platforms are very powerful and run a Linux distribution. Both also come with some trade-offs such as being

larger than a standard microcontroller, consuming more power than a typical microcontroller, and having more overhead because of the Linux distribution. Despite these drawbacks, it was decided that one of these devices would be best for what was needed. The two choices were then examined closely to decide on the best one. Table 8 shows a comparison of the specifications of both of these devices.

Table 8. Comparison of Embedded Platforms

Product	Raspberry Pi 2 Model B+	BeagleBone Black Rev C
Price	$35	$55
Size	3.370" x 2.224"	3.4" x 2.15"
Processor	Broadcom BCM2836	AM3358BZCZ100
Cores	4	1
Clock Speed	900 MHz	1 GHz
RAM	1 GB	512 MB
Onboard Flash	None	4 GB
External Storage	microSD	microSD
Operating Voltage	5V	5V
Power	230 - 800 mA	210 - 460 mA
Digital GPIO	40	65
Analog Inputs	None	7
I^2C	Yes	Yes
SPI	Yes	Yes
Ethernet	10/100 RJ45	10/100 RJ45
USB	4	1
Video Out	HDMI	micro HDMI

After looking at the comparison of the two units, the choice was clear. The **Raspberry Pi 2 was chosen** as the embedded platform. The most significant reason for the choice was the cost. Both devices perform similarly and have similar specifications in most areas so a $20 price difference made the Pi the obvious choice. The Pi also has double the RAM of the BeagleBone, which made it an even better fit. The device will have to host a web application, a database, and the Linux distribution so more RAM will be beneficial. The Pi does lack in digital I/O and analog inputs when compared to the BeagleBone, but the main unit will not require many inputs so the Pi will perform just fine. Both devices have Ethernet, USB, and some communication buses so, again, the cost of the Pi was the deciding factor. In addition to the specifications, both devices were tested for their ease of use. The simple task of loading the Linux distribution and installing some basic software on both devices was performed. From this subjective test, the Pi was easier to setup and work with than the BeagleBone, providing yet another positive for the Pi.

3.4.2 Application Framework

The other important element to consider for the web application was the application framework that is going to be used to build the application. The framework that is used will determine how the application looks, how the application runs, and how the application will be developed. It was very important to choose the correct framework that would help achieve a clean looking and fluid web application and allow for ease of setup and development. There are many different application frameworks in different programming languages that can accomplish a whole suite of different tasks. When searching for the right framework many different aspects were evaluated, including the memory consumption, the programming language used, the documentation, the ease of setup, and the flexibility. The many different choices were narrowed to just three that were looked into more closely: a Java implementation, a Django implementation, and a HTML, JavaScript, and PHP implementation. A summary of these three frameworks can be seen in Table 9.

Table 9. Comparison of Frameworks

Framework	Java Application	Django	HTML/JavaScript/PHP
Idle Memory Consumption	~150 MB	20-30 MB	?
Language	Java	Python	HTML/JavaScript/PHP
Documentation	5	4	5
Ease of setup (5 = easiest)	4	3	5

Table 9 shows some of the information that was considered about each framework. A very rough memory test was run for Java and Django. A basic server was set up to run a boiler-plate web application with each framework, and the memory consumption was recorded. This test was not run for the HTML/JavaScript framework because of the variability in memory consumption of different JavaScript libraries, hosting methods, and many other factors. For each framework, a subjective score was determined for the documentation and the ease of setup. All three frameworks had very good documentation, with Django lagging slightly because it is a newer framework. After considering all these factors and others as well, it was determined that both Django and Java were both good choices. It was decided that a **Java application would be best**. The main reason for the choice was the team's familiarity with Java web applications. Members of the team have worked with Java web applications in the past, so it was decided it would be more time efficient to use Java. The greater memory usage of the Java application should not cause a problem as the Raspberry Pi should have enough memory. A Java application will also be more powerful in terms of a graphing and scheduling interface.

3.5 DATA STORAGE

The power consumption readings from each of the outlet modules must be stored, so they may be accessed at any time through the web application. The most appropriate method of storing information is in a database, which is accessed with a database management system.

3.5.1 Database Management System

Several factors were examined in order to determine which database management system (DBMS) was appropriate. The first was the operating system on which the DBMS would run. The second was the licensing available through each DBMS, to determine if money would need to be spent. The third factor was the variety of available programming languages, specifically the ones used in the main unit. A fourth, but lesser factor, was the data type variety that could be stored in the database. The Pugh analysis table, seen below in Table 10, was used to determine the most appropriate DBMS solution. A +1, -1, and 0 represent the solution is desirable, undesirable, and not applicable, respectively.

Table 10. Pugh Analysis on DBMSs

Solution	Microsoft SQL Server	MySQL	PostgreSQL	SQLite
Windows Server OS	-1	0	0	0
Linux OS	0	+1	+1	+1
Commercial License	-1	0	0	0
Open Source License	0	+1	+1	+1
Supports Java	+1	+1	+1	+1
Supports PHP	+1	+1	+1	+1
Supports Python	+1	+1	+1	+1
Sufficient Data Types	+1	+1	+1	-1
Total Rating	2	6	6	4
Rank	4	1	1	3

According to Table 10 above, Microsoft SQL Server came last in the overall rankings. This was due to its availability only on the Windows Server OS platform, as well as its need for a commercial license. This was undesirable, due to the main unit having a Linux-based embedded platform. SQLite came third in the rankings, due to its lack of desired data types supported. While managing the readings and outlet modules could be achieved using the primitive data types, it would be easier from a development standpoint to have more advanced data types. MySQL and PostgreSQL were both placed first in the rankings, as their criteria met all of the requirements for the Energy Management System. MySQL was chosen as the database management system.

3.5.2 Database Storage Engine

There are several storage engines for MySQL, all of them performing similarly to accomplish the same tasks: creating, reading, updating, and deleting data from a database. The Pugh analysis in Table 11 shows the comparison of several storage engines, and analyzes them to choose the most appropriate solution for the MySQL DBMS.

Table 11. Pugh Analysis on MySQL Storage Engines

Solution	Memory	InnoDB	MyISAM
Reliability	-1	+1	+1
Row-level Locking	+1	+1	-1
Table-level Locking	0	0	+1
Read-heavy Performance	+1	0	+1
Write-heavy Performance	+1	+1	-1
Transaction Support	+1	+1	0
Storage Medium	-1	+1	0
Total Rating	2	5	1
Rank	2	1	3

As seen in Table 11 above, InnoDB is the most desired choice for the storage engine. Memory came second; however, it was undesirable due to its storage medium and reliability. As the name suggests, all of the tables in the database are stored in memory. Once enough changes have been made, the database is then flushed to disk. However, if the main unit lost power, any readings or changes not flushed to the storage device would be lost. InnoDB and MyISAM update the file on the storage device after every query. Row-level locking is important, as it allows the table to be written even when a certain row is locked. MyISAM supports only table-level locking, which could potentially cause backups, as the outlet readings could not be written to until the table is unlocked. This leads to poor write-heavy performance, which could occur if multiple real-time readings were taking place.

4 DESIGN

4.1 OVERVIEW

The Energy Management System is a system designed to allow for monitoring and management of power usage with the objective of providing energy conservation for a home or small business. The system provides an easy method of monitoring, managing and controlling power consumption of all connected electrical loads. The system consists of two main components, the main unit and separate outlet modules. The main unit is installed at the breaker panel of the home or business. It monitors overall power consumption, collects usage data from the outlet modules, and compiles the information. The Energy Management System also has a web application where all of the usage data can be viewed in graphical form. From the web application, the user can control whether an outlet module is on or off, and can limit its power. In addition, a schedule can be created to automatically turn outlet modules on and off at certain times of the day. The outlet modules are replacement outlets for the home or business that monitor and control the power consumption of only that outlet as directed by the main unit. Figure 3 shows a high level diagram of the Energy

Management System. Figure 4 shows the completed project, with the main components of the design labelled.

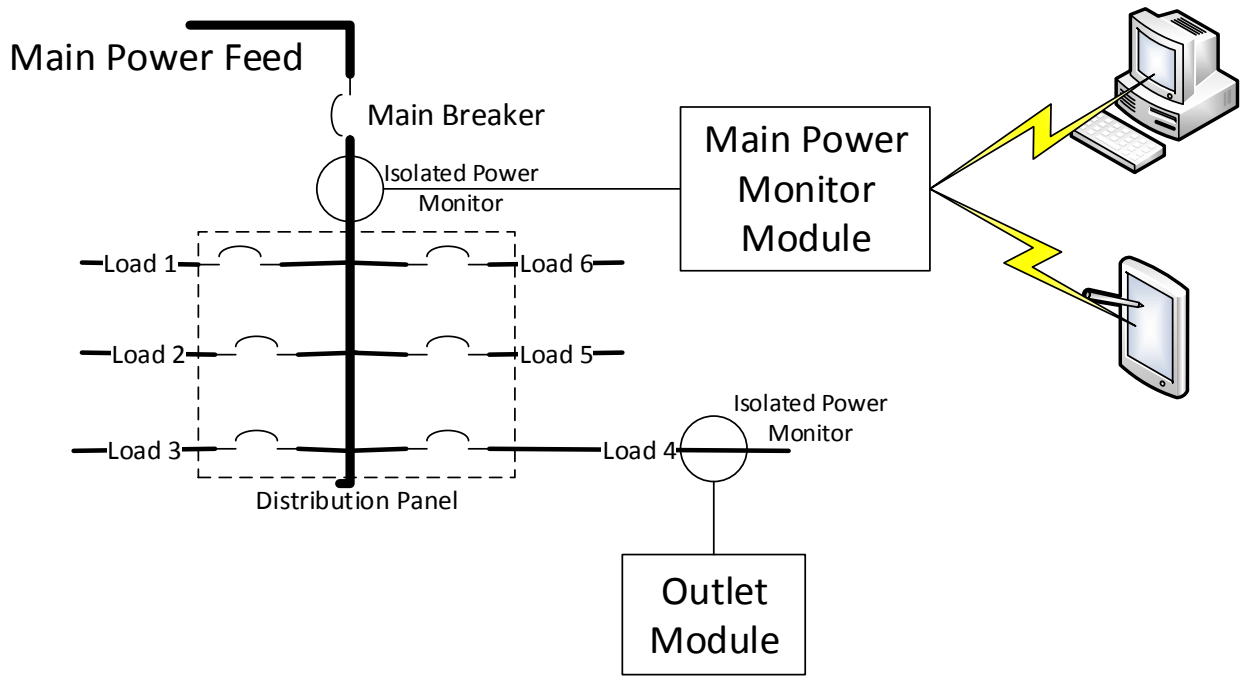


Figure 3 - High-Level System Diagram

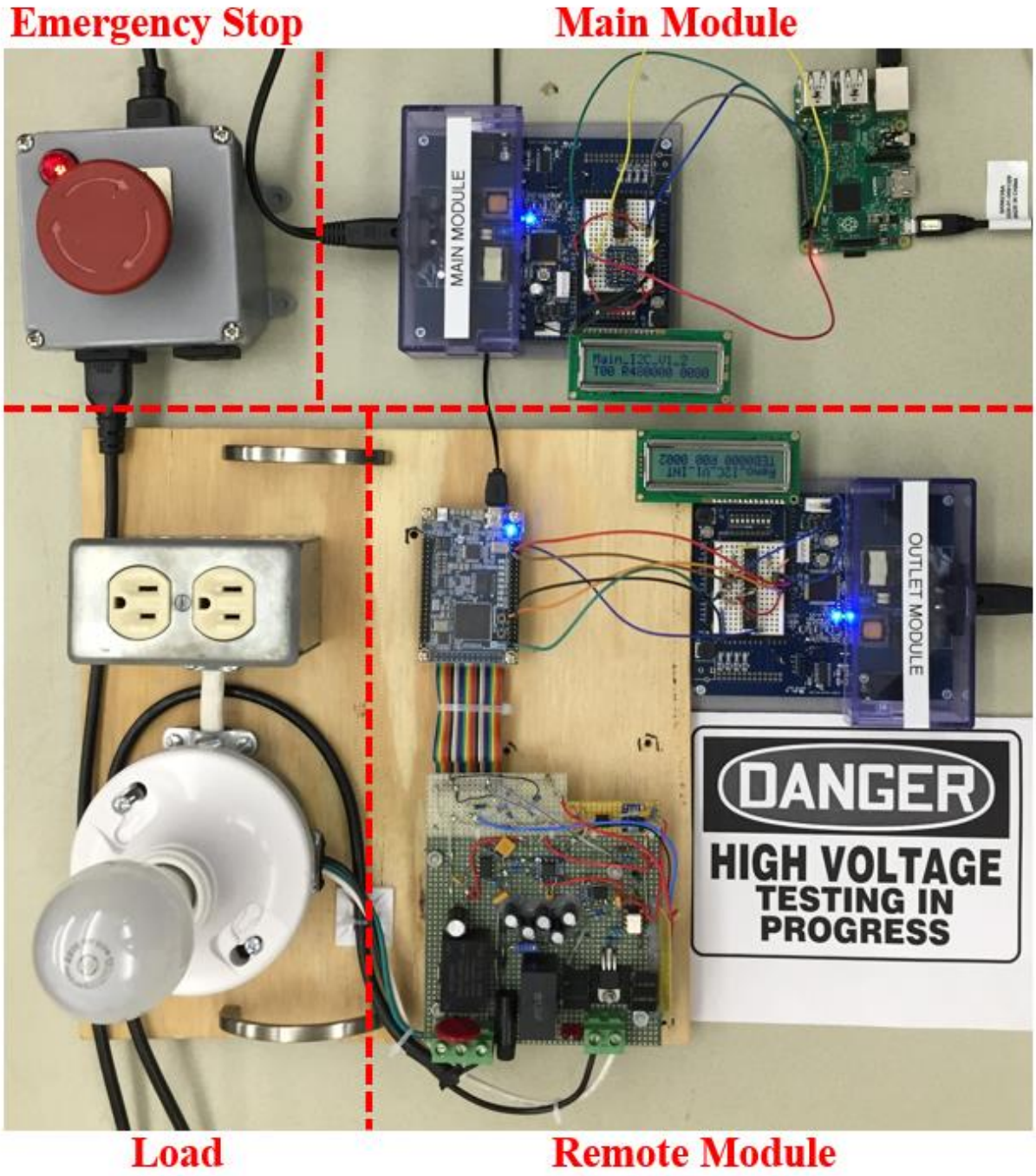


Figure 4 Energy Management System Prototype

The main unit will be composed of two principal hardware components. The main control unit, shown functionally in Figure 5, consists of the master controller, data storage, and communication interfaces. The breaker-monitoring unit, shown functionally in Figure 6, consists of the main breaker power sensing and power line communication functions.

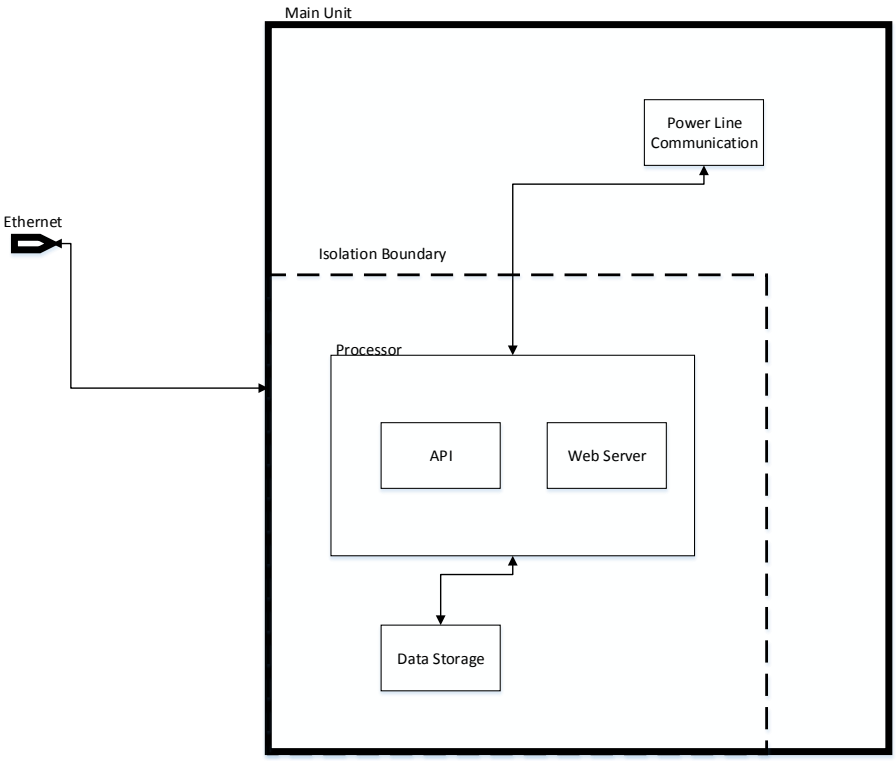


Figure 5 - Main Unit Functional Diagram

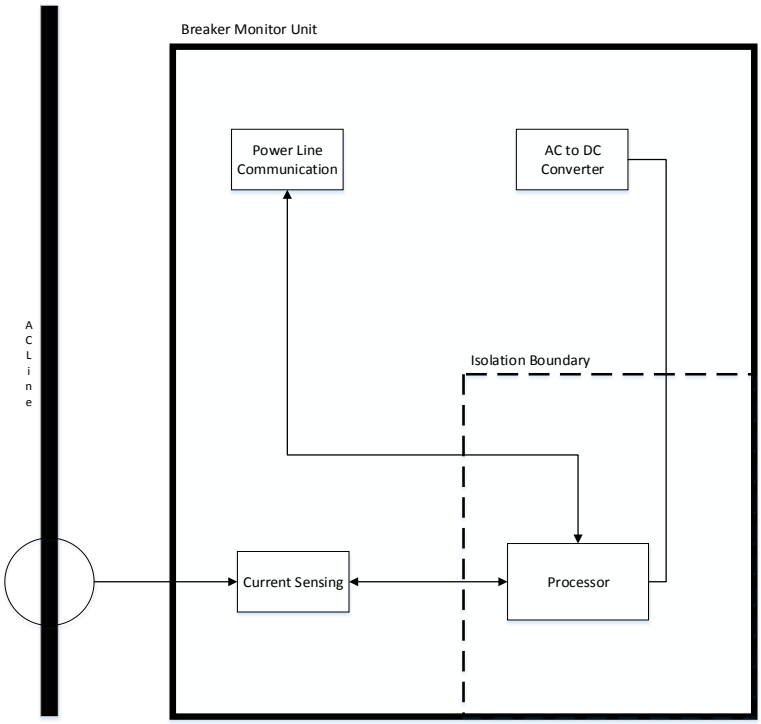


Figure 6 - Breaker Monitor Functional Block Diagram

The remote outlet module, shown functionally in Figure 7, consists of current and voltage sensing, power commutation, load switching and the power line communication interface. The remote outlet module consists of the following submodules: power sense circuitry, switching control, surge protection and a power supply.

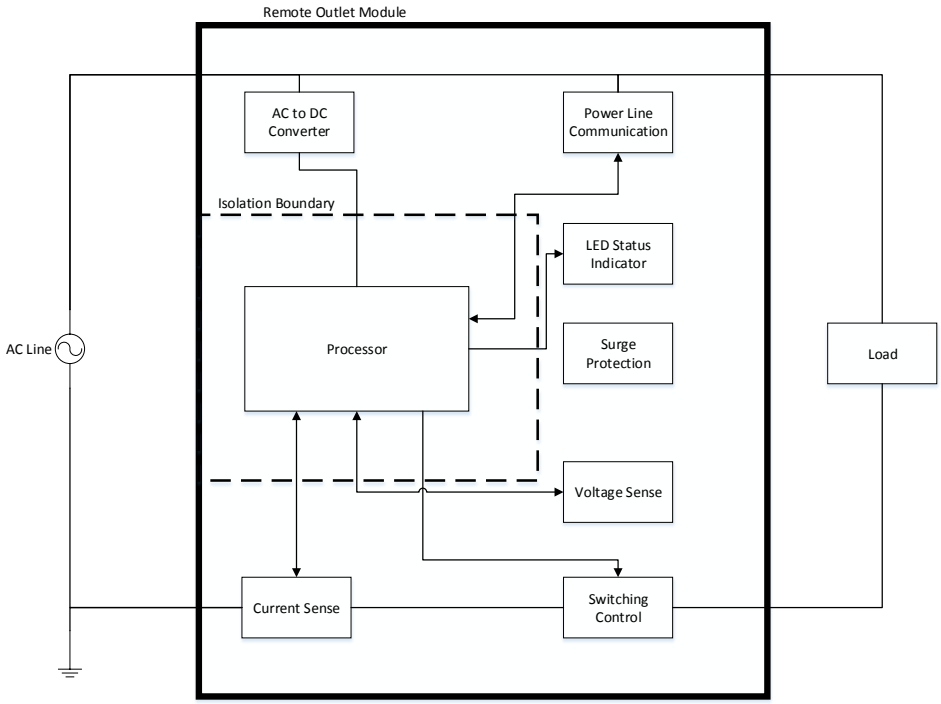


Figure 7 – Remote Outlet Module Functional Block Diagram

4.2 SYSTEM ELECTRONICS

The system electronics were broken into the following submodules: power sense circuitry, switching control, surge protection, and AC to DC power rectification. Therefore, the design section will be broken into these four areas.

4.2.1 Connectors

The control remote outlet electronics will need to interface a load and also the FPGA. The schematic for all of the connectors is provided in Figure 8.

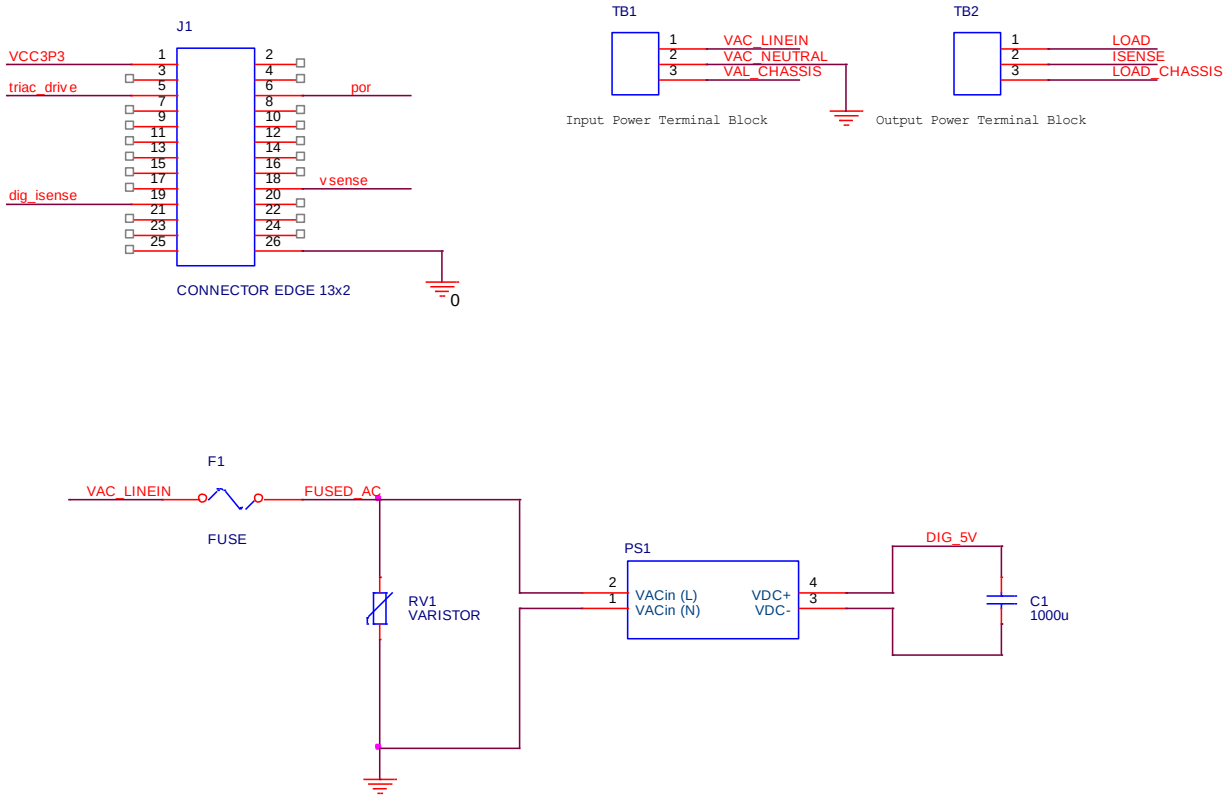


Figure 8 - Remote Outlet Module Connectors

Design Notes for the Connectors:

- J1 – Is a connector to the DE-0 NANO FPGA to be connected directly to the J3 connector located on the bottomside of the DE0 nano board. The connections on this connector are as follows:
  - VCC3P3 : pin 1 : power input : 3.3V from DE-0 Nano development board
  - Por : pin 6 : digital output : power on reset active high signal to the FPGA. When low logic level remote outlet module indicates valid status with all components powered and operational.
  - Triac_drive : pin 7 : digital output : active high signal used to turn on the load.
  - Vsense : pin 18 : analog output : Analog output proportional to line voltage. This is connected to channel 5 of the on-board TI ADC on the DE-0 Nano board.
  - Isense : pin 19 : analog output : Analog output proportional to load current. This is connected to channel 6 of the on-board TI ADC on the DE-0 Nano board.
  - GND : pin 26 : power input : ground from DE-0 nano development board.

The pinout for the connector on the DE-0 Nano board which the J1 connector of the remote outlet module will mate with is shown in Figure 9.

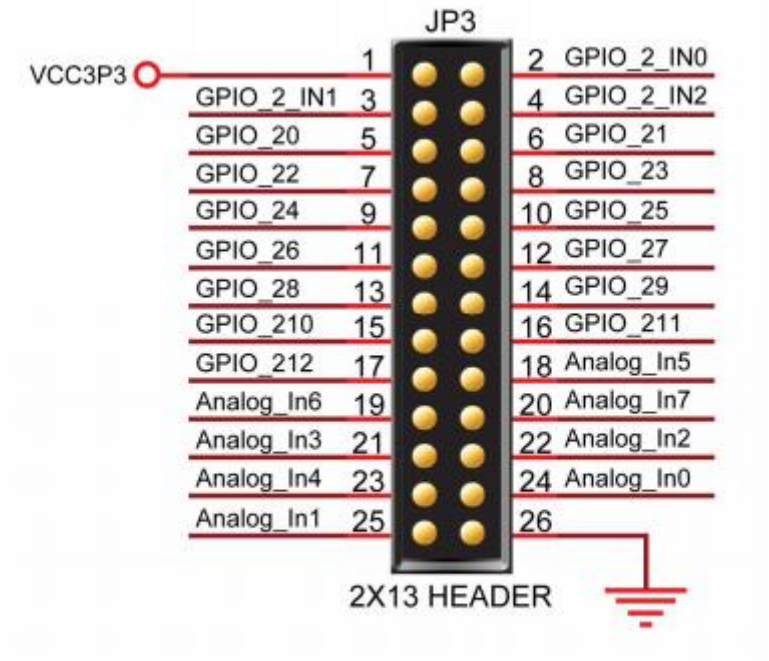


Figure 3-10 Pin distribution of the 2x13 Header

Figure 9 - FPGA Connector to Interface with Hardware

- TB1 – terminal block for input AC power
- TB2 – terminal block output to load

4.2.2 Power Supply

Based on the analysis done for this project, it was decided to proceed following an iterative design process. Therefore, for iteration one a switch mode packaged power supply from Recom will be used. This will provide electrical isolation during testing, and will provide a working solution that mitigates the risk of power supply design. In reality this product would not be feasible at production due to cost. Therefore, time permitting a second iteration with a capacitively coupled supply may be used. This implementation will provide a much cheaper alternative to the switch mode supply, and also take up less board space. This implementation will also need to be run with everything connected directly to line potentials, (including the controller), which while cheaper will be less safe for the purposes of prototyping. This solution is also dependent upon achieving an overall design with low power demands making a capacitively coupled power supply feasible.

4.2.2.1 Generation 1 - Power Supply Implementation

A schematic showing the implementation of the power supply is in Figure 10. The RAC01-05SC is a switch mode supply, which is capable of 2W with an output of 5V. These switch mode supplies provided by RECOM have many different variations, and if requirements change in terms of necessary DC voltage, or power needed a new RECOM part can be quickly chosen.

Design Notes for Power Supply Block:

- Line - Neutral: 120 VRMS signal from power line
- DIG_5V: DC 5V output signal with reference to DIG_GND. This DC voltage is isolated from the AC side and will be used to power all other control circuitry.
- RAC01-05SC refers to RECOM switch mode supply. More details regarding this part can be found in part data sheet provided in the appendix.
- RV1 is a MOV, capable of handling power surges on the power line. The V150ZA05P was chosen to limit the voltage at 165 VRMS. This component will have no effect on circuitry during normal operation. During power surges, the MOV will dissipate excess energy thus protecting all other circuitry.
- F1 is a slow blow fuse, which offers protection for the power source in event of a short circuit failure in the remote unit circuitry. In the case that the MOV does fail, due to an excessive number of power surges, the MOV will often become a partial or complete short, thus providing a direct path between power and ground for current to flow only limited by the resistance of the wire. Therefore, a fuse is used to provide protection in the case that the MOV fails. A slow blow fuse was chosen in an attempt to limit nuisance faults.

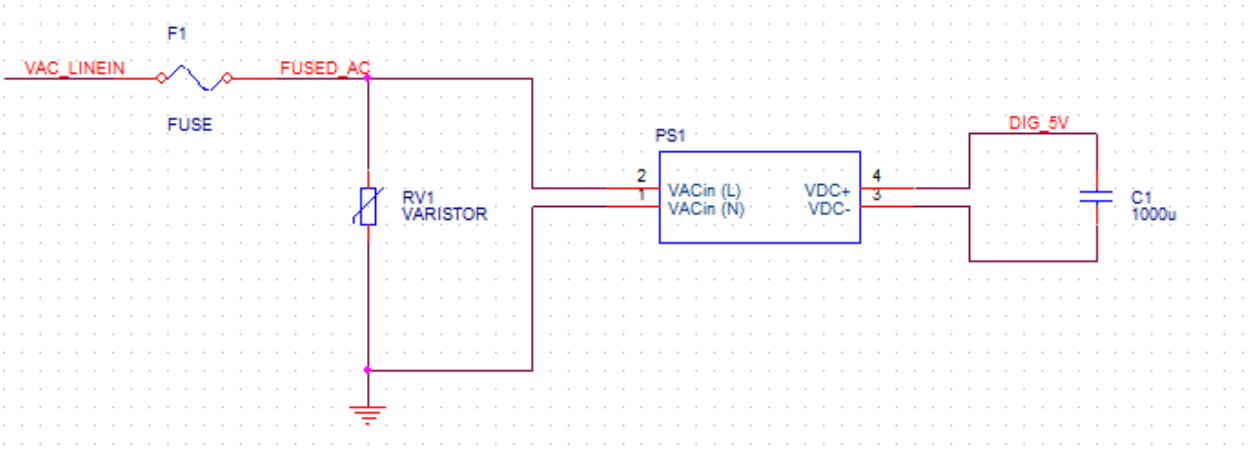


Figure 10. Power Supply Schematic

4.2.2.2 Generation 2 – Power Supply Implementation

Figure 11 shows an initial design for the second generation DC power supply.

Design Notes for Capacitively Coupled Power Supply:

- Based on the necessary DC voltages, and currents needed part values will change. Due to the many design factors still seen as unknowns.
- The basic operation of the circuit is as follows.
    - During positive half-cycles of the 120 VRMS sine wave, D1 is forward biased thus charging up the C3 capacitor. The rate of charging of the C3 capacitor is controlled

by the C1 and R1 impedances. C1 is used to reduce the power dissipated, and R1 is used to limit in-rush currents when power is initially applied.

- During negative half-cycles of the 120 VRMS sine wave, D2 is forward biased to maintain AC current through C1, and maintain a net DC value of 0.
- The R2 resistor was selected to bias the Q1 transistor. The D5 zener diode is used to keep the base of the Q1 transistor at a given voltage. This allows the Q1 transistor to act as a voltage regulator, with an output voltage given by Vz(D5) – 0.7V or approximately 5 VDC, with a 6.2V Zener.

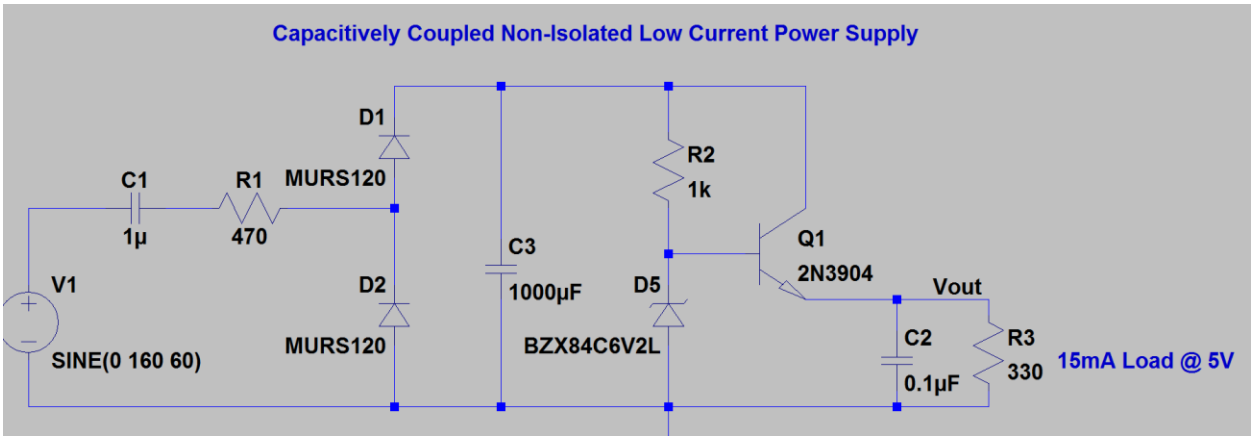


Figure 11. Capacitively Coupled Power Supply

4.2.3 Power On Reset (POR)

This block will generate a reset signal for the controller, which shall indicate the status of the outlet hardware. This reset pulse indicates if the remote outlet monitor circuitry is powered on and functioning. If the remote outlet module is not currently operational, the reset signal is high. The reset signal goes low to indicate to the FPGA that the remote outlet module is operational. The schematic for the power on reset circuit is shown in Figure 12.

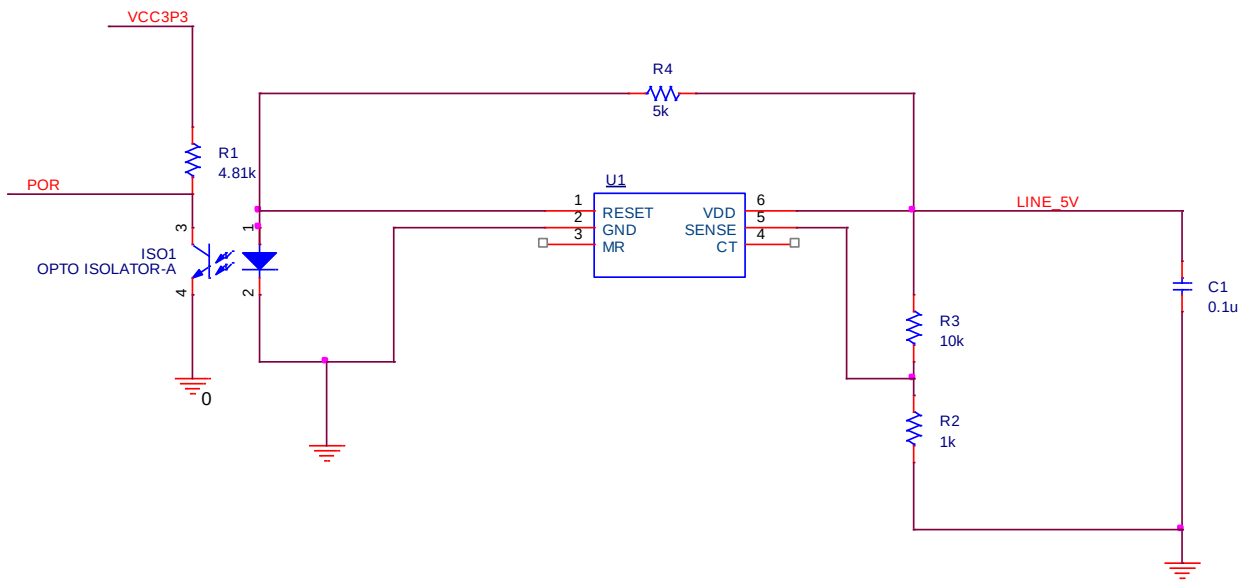


Figure 12 - POR Circuitry

POR Design Notes:

- The Line 5V signal is divided down via the R3 and R4 voltage divider and monitored by the TPS3808G01 reset supervisor chip. The reset supervisor is then used to control current through an opto-isolater and the output of the opto is provided to the input of the FPGA as the POR input.
- The TI reset supervisor connections are as follows:
  - Pin 4 : Ct - is left unconnected thus providing a fixed input delay of 25 ms
  - Pin 3 : MR – is left unconnected as MR is not to be used
  - Pin 6 : Chip is powered off the 5V_line. If the 5V line is low than reset will be active and there will be no current through the LED, thus forcing POR output to pull to 3.3V through R1. When the 5V line is not present there also will be no current through the LED. U1 will become functional at a voltage less than the forward voltage of the LED.
  - Pin5 – Configurable sense input. The function of the sense input is provided in Figure 13.

SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then $\overline{RESET}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{RESET}$ assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 11.

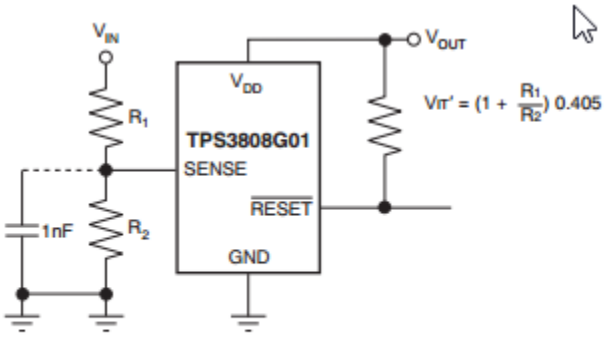


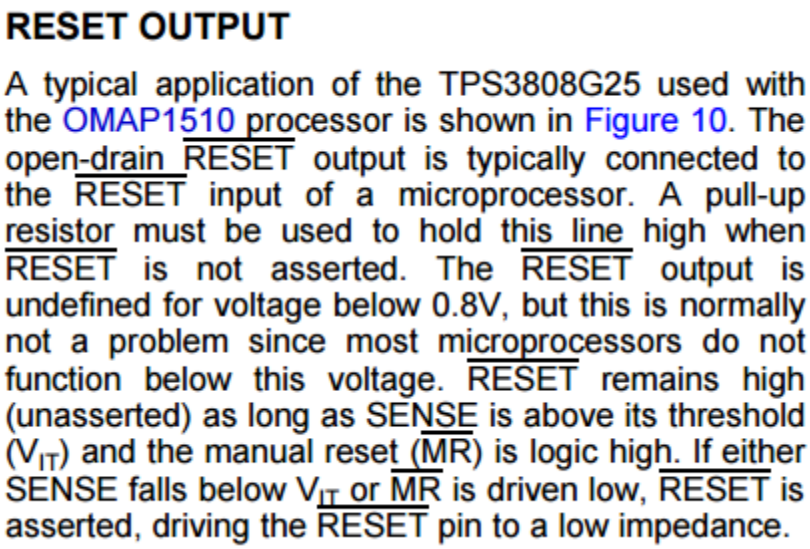
Figure 11. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage

Figure 13 - Description of Sense Function

- Resistor values of 10k and 1k were chosen to set the threshold voltage for the reset monitor. The following equation shows the voltage threshold for the reset monitor based on the chosen resistors of R3 and R2.

$$V_{It} = \left(1 + \frac{10k}{1k}\right) * .405 = 4.455\,V$$

- The functionality of the Reset output is explained in Figure 14.



RESET OUTPUT

A typical application of the TPS3808G25 used with the OMAP1510 processor is shown in Figure 10. The open-drain RESET output is typically connected to the RESET input of a microprocessor. A pull-up resistor must be used to hold this line high when RESET is not asserted. The RESET output is undefined for voltage below 0.8V, but this is normally not a problem since most microprocessors do not function below this voltage. RESET remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset (MR) is logic high. If either SENSE falls below V_{IT} or MR is driven low, RESET is asserted, driving the RESET pin to a low impedance.

Figure 14 - Reset Output Functionality

- Pull-up resistor R4 of 5k results in 1 mA of current through the LED which turns on the opto-transistor thus connecting the por output to gnd.

The POR circuitry was tested by monitoring the POR output circuitry during a power on event on the 5VDC input. Figure 15 shows the operation of the POR circuitry. Channel 1, shows the 5V input power ramping up. Channel 2, shows the POR output circuitry. It can be seen that a delay of 25 ms exists between the reset de-asserting, and the output being valid, due to the pin 4 being left open.

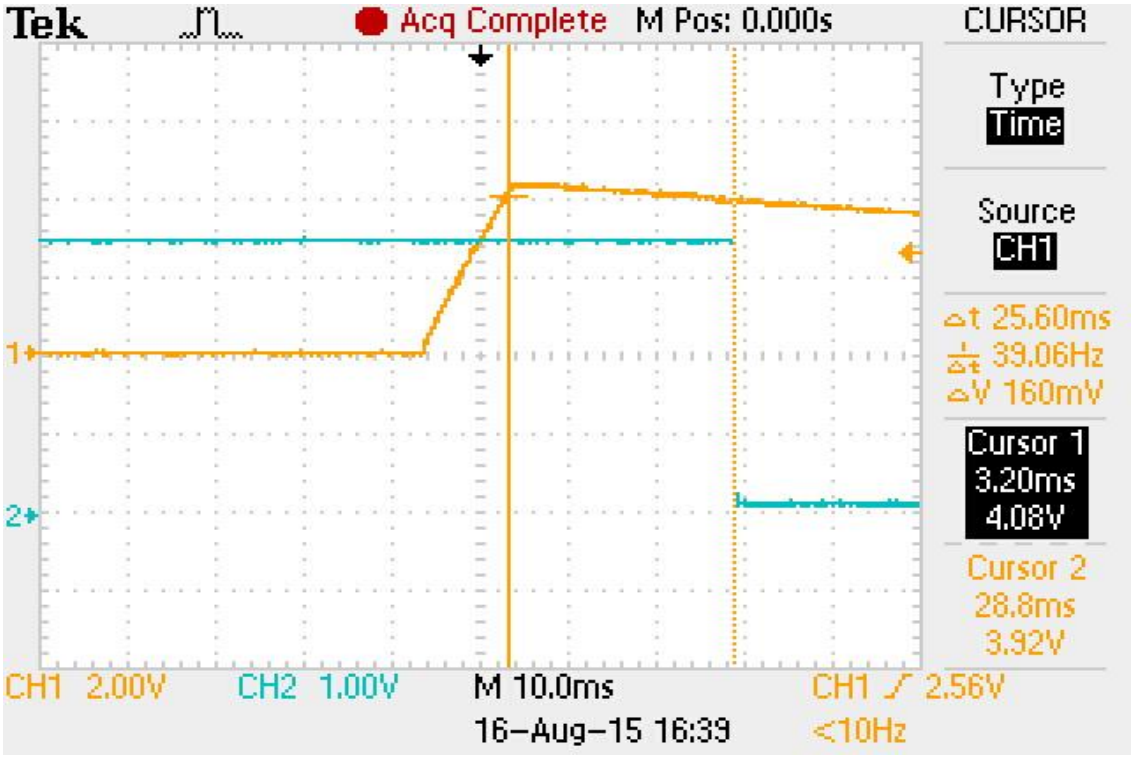


Figure 15 - POR Circuitry

4.2.4 Load Switch

The load switch must be capable of switching the power across the load, while preferably having its control circuit electrically isolated from the AC line. This circuit will be used to allow the FPGA to switch the load ON and OFF.

A schematic showing the implementation of the load switch is in Figure 17.

Design Notes for load switch:

- MOC3063M refers to an optically coupled TRIAC driver with zero crossing circuitry. The functional schematic for the MOC3063M, per the data sheet, is shown in Figure 16. The MOC3063 is an optical TRIAC driver, thus allowing an isolated source to drive a TRIAC. The M0C3063 also has zero crossing circuitry thus eliminating the need for timing the TRIAC fire pulse with the AC line zero cross. To turn the TRIAC ON, the LED between pins 1 and 2 must be illuminated (current flowing thru device). To turn the TRIAC OFF, the LED between pins 1 and 2 must be non-illuminated (no current flow thru device).
- Due to the built in zero crossing circuit the MOC3063M TRIAC driver cannot be used for implementing phase control switching of the TRIAC. There are pin compatible opto TRIAC drivers without internal zero crossing circuitry which can be used if it is later determined that the design should be capable of lamp dimming.

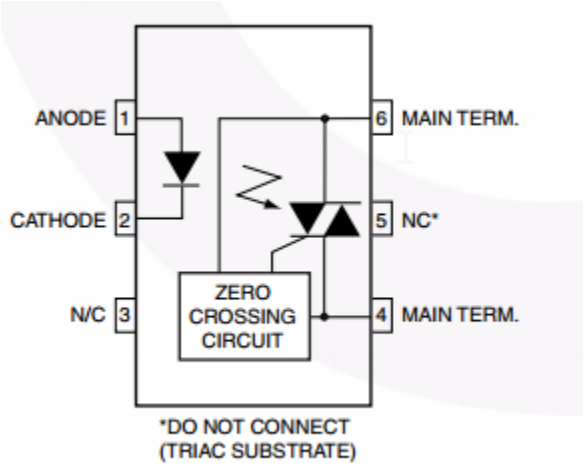


Figure 16. MOC3063 Functional Diagram

- The operation of the load switch is as follows:
  - OFF – When off functionality is required the FPGA will drive its output low. This will turn off the Q2 transistor thus providing no current flow thru the light emitting diode.
  - ON – When on functionality is required the FPGA will drive its output high. This will cause a base current turning on the Q2 transistor and providing a current to flow illuminating the diode of the MOC3063 part.
- R5 is provided to limit the current when the load switch is on to (3.3V – V_{led}) / 510 ohms.
- R3 is chosen to limit the Q2 base current to (3.3V-0.7V)/10 kohms.
- R4 is chosen such that the transistor will be connected to ground when the FPGA output is open thus insuring the load switch will remain off when not driven by the FPGA, which is seen as good practice as this guarantees the device will not falsely turn on.
- An RC snubber (R1 and C1) is designed to limit the rate of change in voltage with respect to time thus preventing the TRIAC from erroneously turning on.
- The TRIAC Q1 is used to switch the AC power across the load. When the gate is pulsed ON the TRIAC acts as a short circuit, whereas when the gate is OFF the TRIAC acts as an open circuit once any existing load current drops below the holding current. The TRIAC is bidirectional and therefore will conduct current for both the positive and negative cycles. The TRIAC was selected to safely switch 20 amp continuous loads in 120 VRMS circuits. It will need to be mounted on a heat sink to run high current loads continuously.
- R4 is used to connect the gate of the TRIAC to the main terminal when the gate is not being driven to zero thus preventing the TRIAC from false latching on.

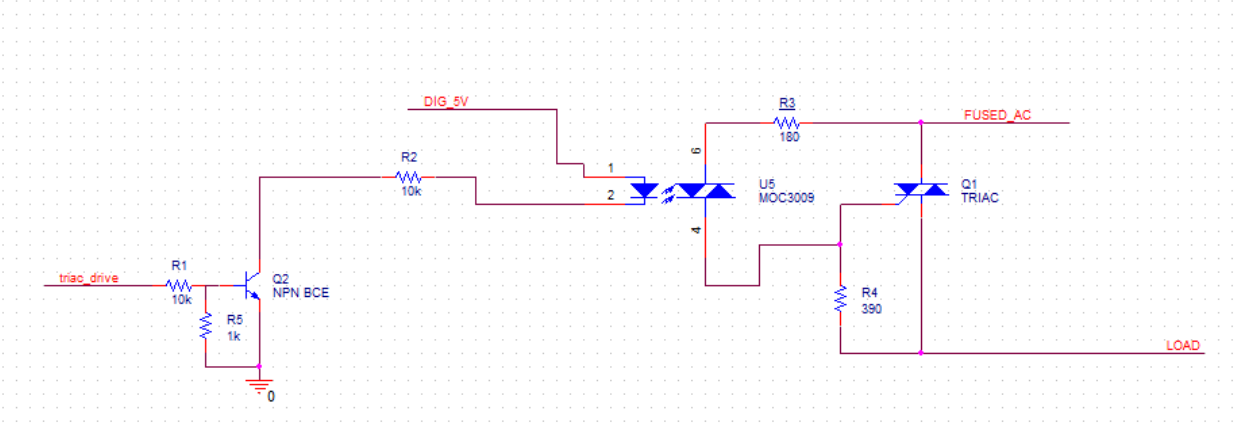


Figure 17. Load Switch Schematic

Detailed Design Notes for the Load Switch are as follows:

Per the MOC3043M datasheet →IFT = LED trigger current = 5 mA max. At 5 mA Vf is approximately 1.1 V. Assuming that Vce of the 2N3904 transistor is 0.1V then:

$$R3 = \frac{5 - 1.2}{5mA} = 760\ ohms$$

Pick 680 ohms → standard value

$$I_c(2N3904) = \frac{5 - 1.2}{680} = 5.6mA$$

Assume forced beta = 10 for 2N3904

$$I_B(2N3904) = \frac{5.6mA}{10} = 0.56mA$$

Then

$$R1 = \frac{3.3 - 0.6}{0.56mA} = 4.8kohms$$

Pick 3.9kohms standard value for R1

Pick R2 = 10k

$$I_{R1} = \frac{3.3 - 0.6}{3.9k} = 0.69mA$$

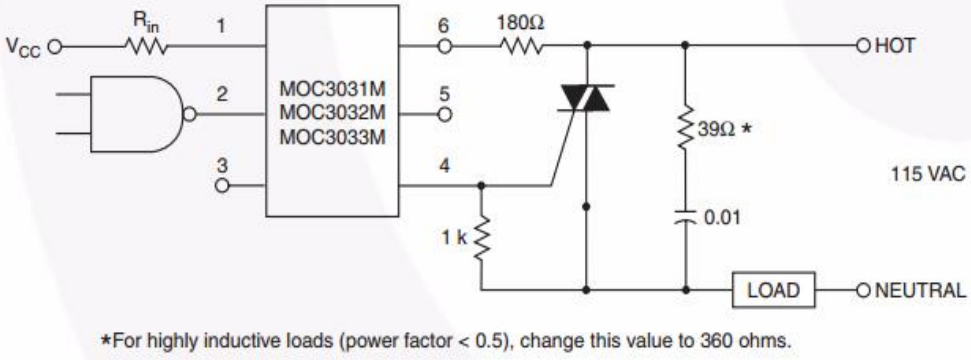
$$I_{R2} = \frac{0.6}{10k} = 0.06mA$$

$$I_B(2N3904) = I_{R1} - I_{R2} = 0.69 - 0.06 = 0.63mA$$

Required 0.56mA so OKAY

Typical circuit (Fig 12, 13) for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 5mA for the MOC3033M and MOC3043M, 10mA for the MOC3032M and MOC3042M, or 15mA for the MOC3031M and MOC3041M. The 39 ohm resistor and 0.01µF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.



*For highly inductive loads (power factor < 0.5), change this value to 360 ohms.

Figure 12. Hot-Line Switching Application Circuit (MOC3031M, MOC3032M, MOC3033M)

Figure 18 Hot-Line Switching Application Circuit

The 180 ohm resistor limits the turn on current when the triac is triggered if firing at peak of line voltage

$$I_{trig} = \frac{160V}{180ohms} = 0.9\ A$$

This is below the isolator 1 amp peak current rating and triggering will typically be well below the peak of the line voltage

4.2.5 Power Sensing

Power sensing has been broken into two sub-modules of current and voltage sensing. Through the acquisition of the voltage and current characteristics important power parameters can be tracked. Current sensing circuitry which generates an analog voltage proportional to the sensed current,

and voltage sensing circuitry which generates a voltage proportional to the sensed voltage will be fed into ADC converters of the chosen controller which will then use this information to determine the current and voltage waveforms in real-time.

4.2.5.1 Current Sensing

This block provides a proportional analog signal to the ADC located on the DE-0 nano board which corresponds to the load current. The current signal is centered on 1.65V and has a resolution of 67 mV per Amp. The designed current sensing circuit schematic is shown in Figure 21.

Design Notes for Current Sensing:

- The ACS722 refers to a Hall effect current IC manufactured by Allegro. A block diagram showing the chip functionality, from the data sheet, is shown in Figure 19.

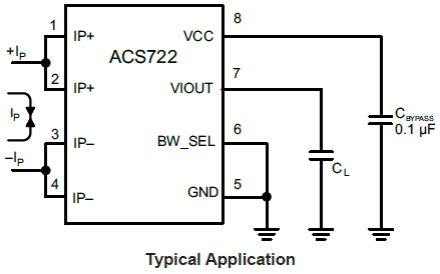


Figure 19. Hall Current Sensor IC Typical Usage per Datasheet

- The ACS722 will measure a bidirectional current, which is run through pins 1, 2 and 3, 4. An output voltage will be generated on pin 7 which will be proportional linearly to the sensed current with an offset of Vcc / 2. Figure 20 shows the expected voltage outputs for various current levels.
- The ACS722 consists of a precise, low-offset, linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage.

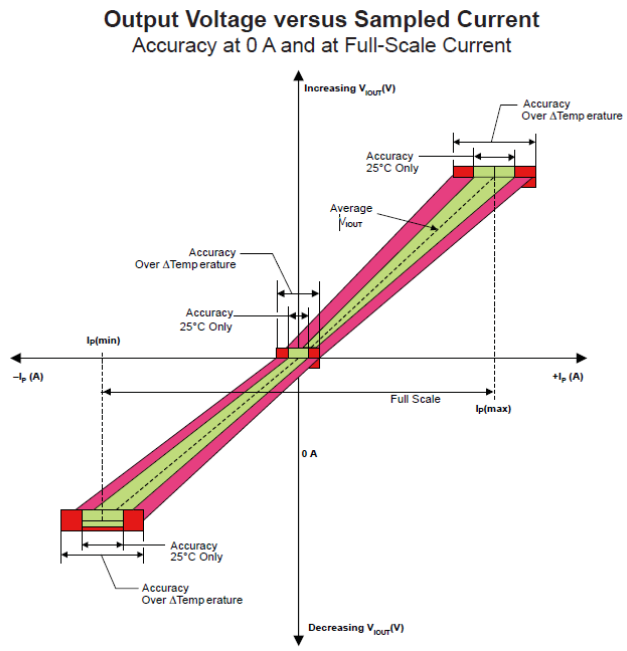


Figure 20. Input Current vs Output Voltage Characteristics of Current Sense Chip

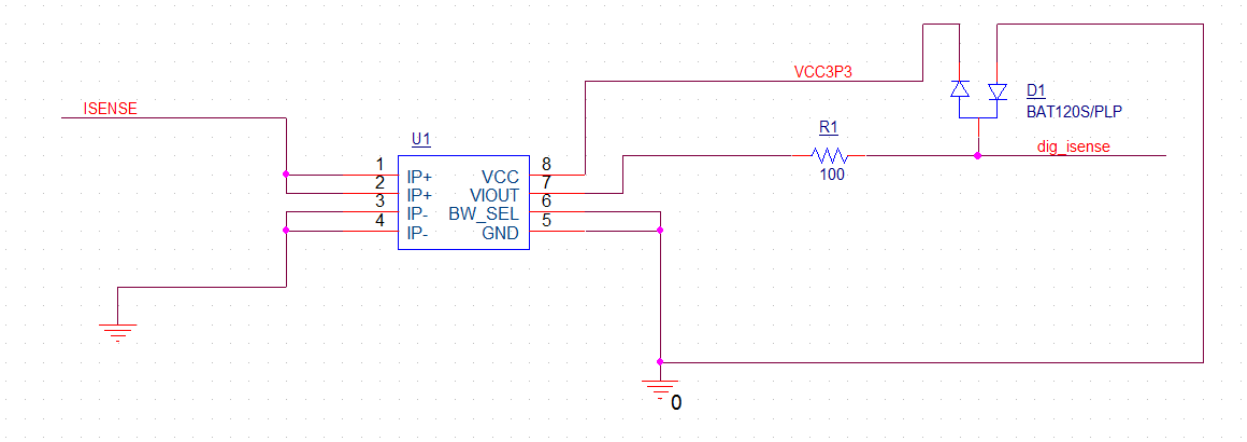


Figure 21. Current Sense Circuit Schematic

- C2 is a decoupling capacitor recommended by the data sheet application note.
- C3 is a filter capacitor recommended by the data sheet application note.
- C4 is an optional filter capacitor which may be needed depending on the signal integrity of the output voltage.
- R1 is a current limiting resistor, to protect the FPGA from sinking too much current.

The current sensing range is -20A to 20 A, centered around 1.65V and has a sensitivity of 66 mV/A.

Table 12 Current Sense Parameters

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Nominal Performance						
Current Sensing Range	I_{PR}		–20	–	20	A
Sensitivity	Sens	$I_{PR}(min) < I_P < I_{PR}(max)$	–	66	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional; I_P = 0 A	–	V_{CC} x 0.5	–	V
Accuracy Performance						
Sensitivity Error	E_{sens}	T_A = 25°C to 150°C; measured at $I_P = I_{PR}(max)$	–1.5	–	1.5	%
		T_A = –40°C to 25°C; ; measured at $I_P = I_{PR}(max)$	–	±2	–	%
Offset Voltage	V_{OE}	I_P = 0 A; T_A = 25°C to 150°C	–10	–	10	mV
		I_P = 0 A; T_A = -40°C to 25°C	–	±15	–	mV
Total Output Error*	E_{TOT}	$I_P = I_{PR}(max)$, T_A = 25°C to 150°C	–2	–	2	%
		$I_P = I_{PR}(max)$, T_A = –40°C to 25°C	–	±3	–	%
Lifetime Drift Characteristics						
Sensitivity Error Lifetime Drift	E_{sens_drift}		–	±2	–	%
Total Output Error Lifetime Drift	E_{tot_drift}		–	±2	–	%

*Percentage of I_P, with $I_P = I_{PR}(max)$

The current sensing circuitry was tested to verify its functionality. This was done by driving a known amount of current through the current sense IC ranging from 10A to -10A. The results of this test is shown in Table 13. A plot of the test results for the current IC are shown in Figure 22. This plot shows the applied current on the x-axis, with the measured output voltage on the y-axis. This test revealed that an offset voltage of 1.68V for the current IC with a sensitivity of 65.7 mV per A.

Table 13 Hardware Test Results for Current Sensor

Test Results	
Current (A)	**Voltage (V)**
10	**2.337**
5	**2.005**
2	**1.809**
1	**1.742**
0	**1.68**
-1	**1.614**
-2	**1.548**
-5	**1.351**
-10	**1.02**

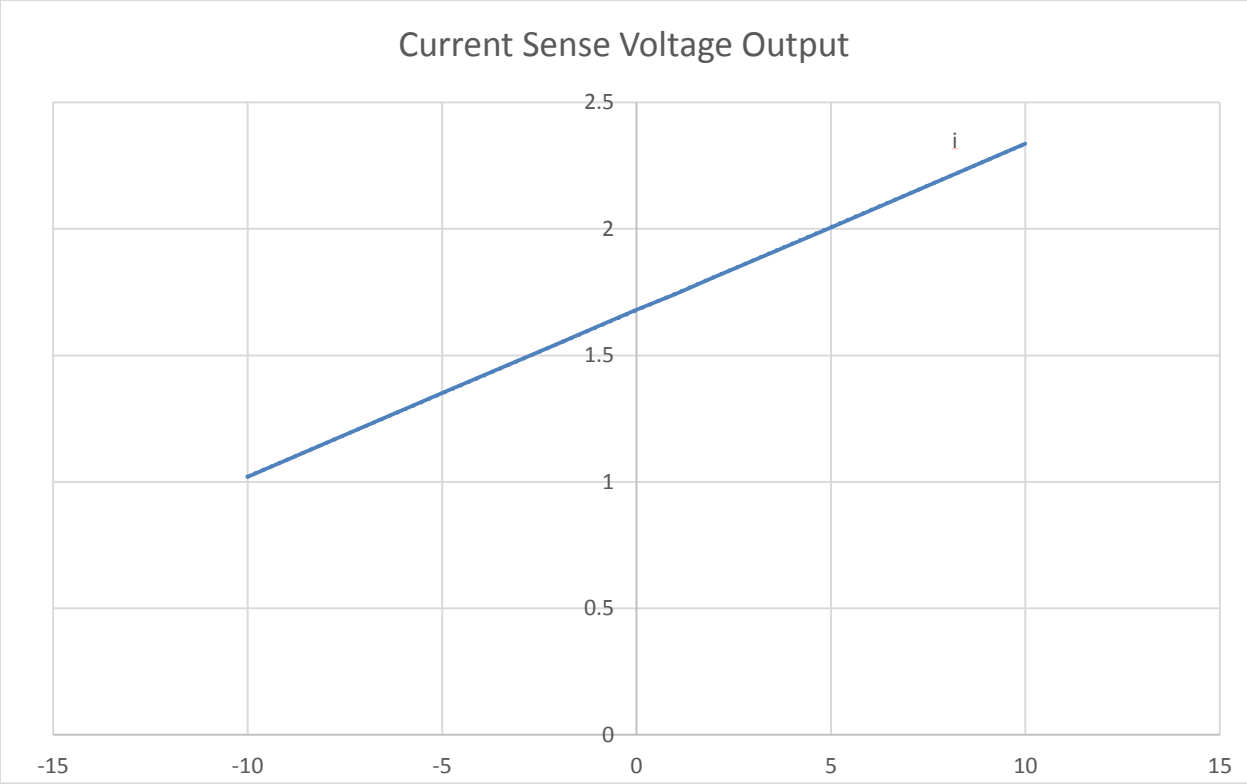


Figure 22 Plot of Hardware Test Results

The current sense circuit was further tested by applying a 120 ohm resistive load across the load terminal and enabling the load switch. Based on this load the expected current was a 60 Hz sine wave of 1.414A peak. The output voltage of the current IC for the 120 ohm load is shown in Figure 23. The measured value from the current IC was 1.4626A peak, which has a percent error of 3.44% assuming the resistance used was exactly 120 ohms and the line voltage was exactly 120 VRMS.

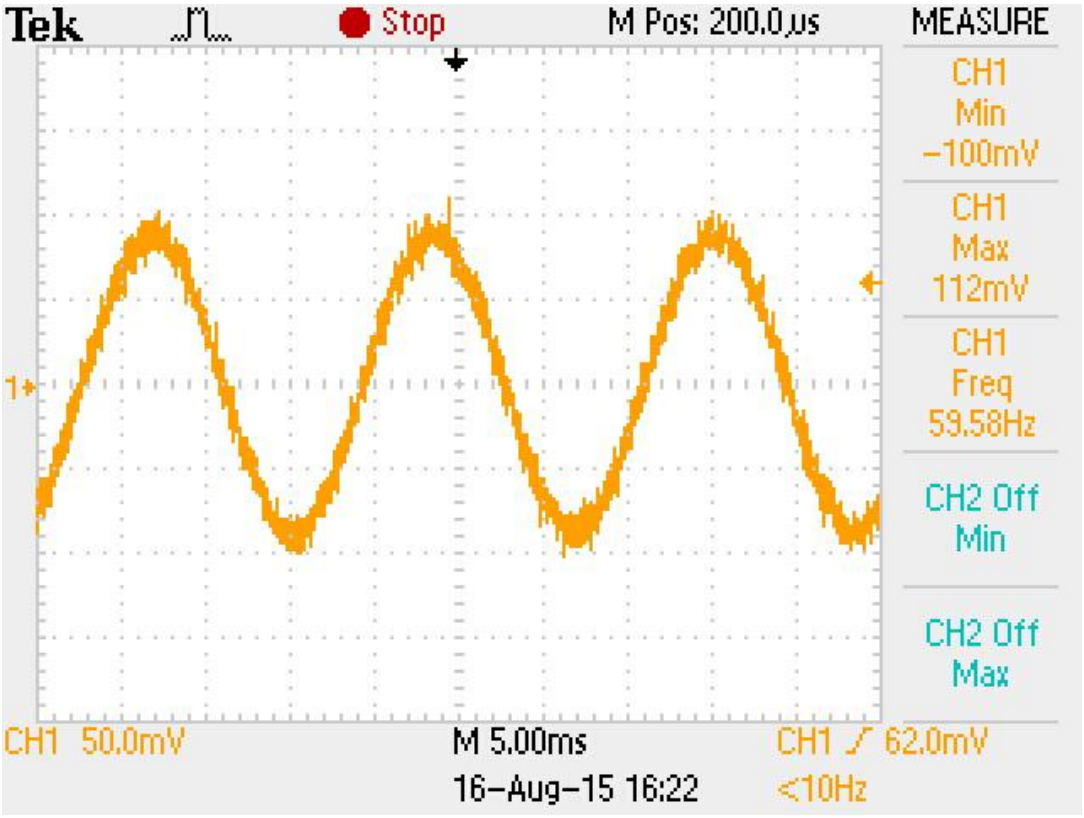


Figure 23 120 Ohm Resistive Load Current Sesne

4.2.5.2 Voltage sensing

This block provides a proportional analog signal to the ADC located on the DE-0 nano board which corresponds to the load voltage. The designed voltage sense circuit schematic is shown in Figure 25. A circuit was also needed to generate a 5VDC voltage referenced to neutral which could be used as power for the isolated amplifier. The schematic for the generation of this voltage generation is shown in Figure 26.

Design notes for Voltage sense:

- The ACPL-C87A refers to an integrated circuit which provides an optically isolated amplifier designed specifically for voltage sensing. It has a 2V input range and a high input impedance thus minimizing its loading effects. A differential output voltage that is proportional to the input voltage is created on the output side of the optical isolation barrier. The part uses sigma-delta modulation technology to transmit the signal information digitally across the isolation boundary. The functional block diagram for this part can be seen in Figure 24.

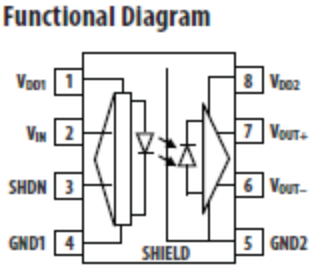


Figure 24. ACPL-C87A Functional Diagram

- The ACPL-C87A provides an isolated amplifier allowing the controller to sample the line voltage. The ACPL-C87A requires two isolated supply voltages: one for the digital side, and one for the line side. The digital voltage DIG_3V3 can be provided by the main power supply. The digital generated voltage DIG_3V3 CANNOT supply the line side supply voltage, as this would break the isolation barrier defeating the purpose of the chip. Therefore to provide a 5V reference to Neutral, a simple capacitively coupled power supply is generated which is capable of sourcing the 15mA required by the isolated amplifier input side circuitry.
- The voltage sense circuit senses the line voltage, feeds a part of this voltage into the isolation amplifier, which then allows the FPGA to determine the sensed voltage.
- R7, R8, R9 and R10 in Figure 25 function as a voltage divider such that the 120 VRMS line voltage is scaled down to 2V to be fed into the isolation amplifier. The maximum line voltage was assumed to be 160 VRMS, so this value was to correspond to 2V as seen by the isolation amplifier input. The chosen resistor values result in the following input voltage at 160 VRMS.

$$V_{in} = \frac{3.9k}{303.9k} * 160 = 2.05V$$

- The series connection of R7, R8, and R9 is the part of the voltage divider responsible for dropping most of the line voltage. Therefore a large value of 300k ohms was chosen to minimize power dissipation. (V^2/R). This resistor was also split up into three resistors, which is standard practice in this application as it allows for the power dissipation to be divided among three different resistors instead of having all of the power dissipated across one resistor. In this configuration, the maximum possible power dissipation of each R7, R8 and R9 is 27.738 mW.

$$P = \frac{V^2}{R} = \frac{\left(\frac{158\ V}{3}\right)^2}{100\ kohms} = 27.7\ mW$$

- 158 V is the voltage differential across the total series combination of R7, R8 and R9. Since all resistors are of equal value the voltage will be evenly split across each resistor.

- 100kohms is the chosen value of the resistors.
- The amplifier with resistors R12, R11, R13, and R16 is a balanced differential amplifier capable of performing signal conditioning and gain adjustment.
- C3 and C4 comprise a ow pass filter on the output voltage signal to remove high frequency noise.

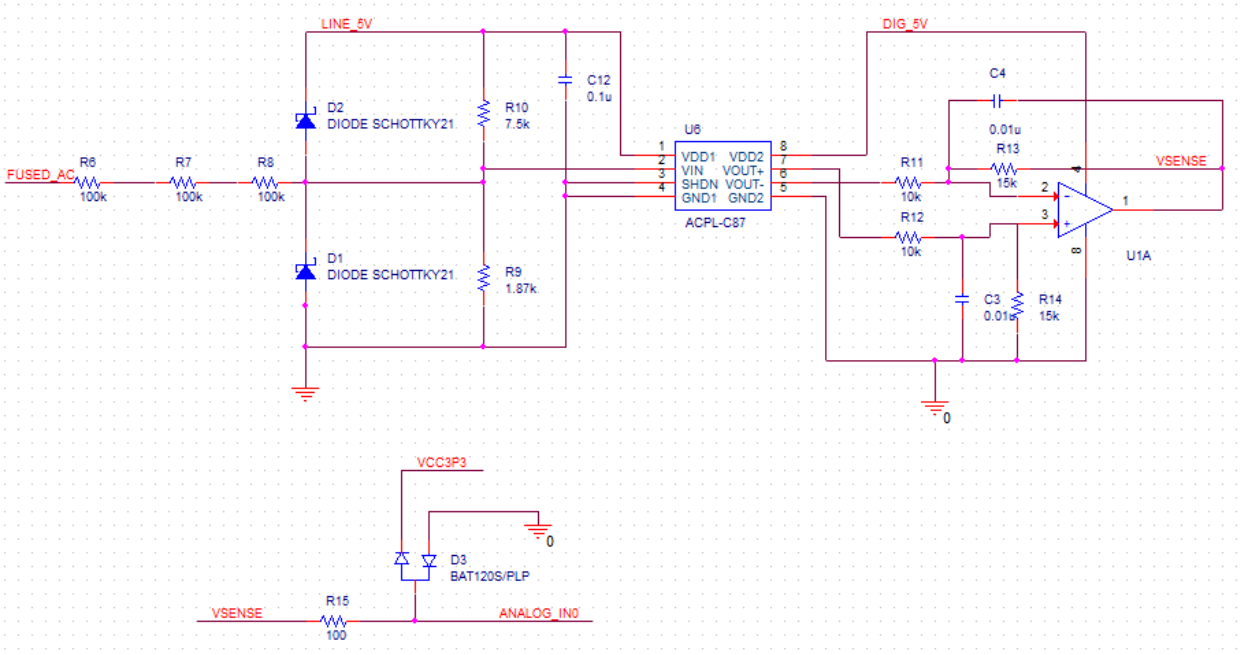


Figure 25. Voltage Sense Schematic

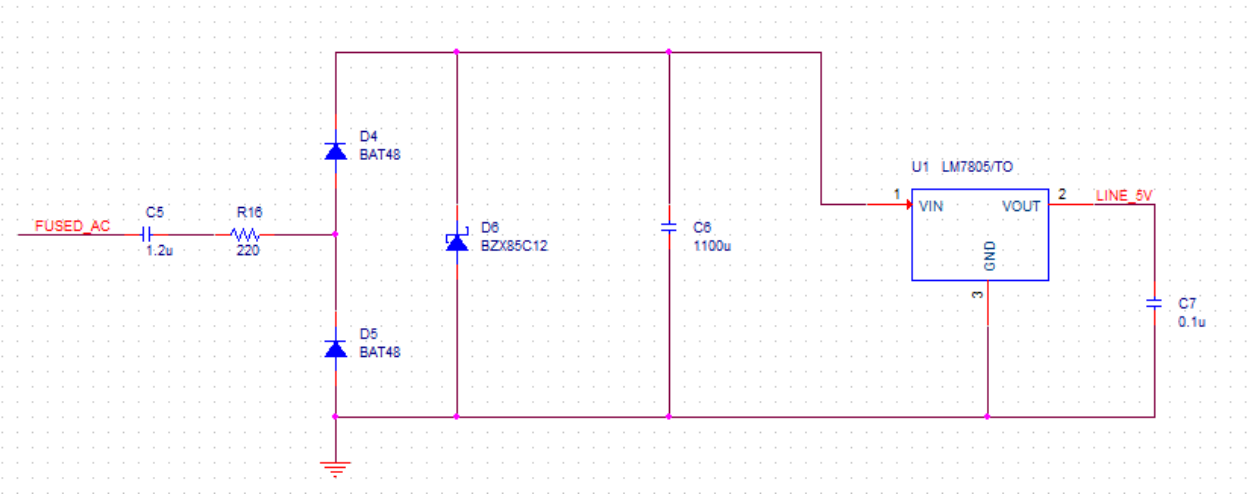
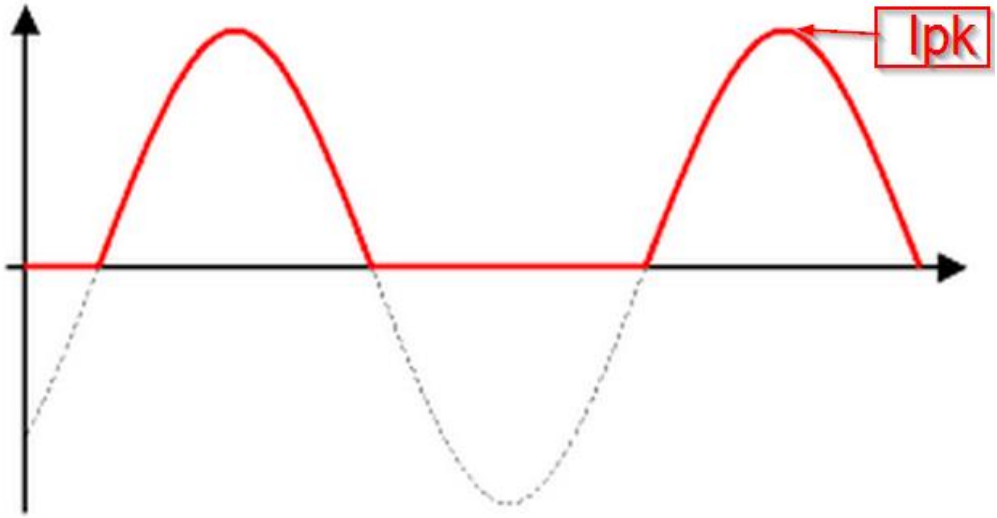


Figure 26 - Line 5 VDC Generation Referenced to Neutral

Line 5V Generation Detailed Design Description:

A 5VDC voltage referenced to neutral is needed for the voltage sense amplifier primary side. This 5V reference will be used to power the hot side of the isolation amplifier and also used to generate a reference to center the divided line voltage around 1V.

- The capacitively coupled power supply is shown in Figure 26. It takes the line (120 VRMS) with respect to Neutral and produces a 5V supply capable of providing 15 mA. The functionality of this capacitively coupled supply is the same as the capacitively coupled supply discussed in the generation 2 power supply design section.
- To step the line voltage down to a small fraction of the input means the impedance of C5 must be high with respect to R16 and C6
- Charging current to C6 is supplied via D4 - this is a half-wave circuit
- The average current (ID) thru C5 is given by



$$I_{Davg} = \frac{1}{T}\int_0^t I_{pk}\sin(wt)\,dt = \frac{I_{pk}}{2*\pi}\int_0^{\pi}\sin(wt) = -\frac{I_{pk}}{2\pi}\cos(wt)\Big|_{pi}^{0}$$

$$I_{Davg} = \frac{I_{pk}}{\pi}$$

- To supply a constant Load of Iload requires:

$$\frac{I_{pk}}{\pi} > I_{LOAD}$$

- Thus to size C1 to determine Impedance Required to Provide the Needed I Load

$$I_{pk} = \frac{V_{pk}}{X_{C5}}$$

$$X_{C5} < \frac{V_{pk}}{I_{pk}} = \frac{V_{pk}}{I_{load} * \pi}$$

$$C_5 > \frac{I_{load}}{V_{pk} * 2f}$$

- for Iload = 15 mA

$$C_5 = \frac{15mA}{160 * 2 * 60} = 0.78uF$$

- Assuming 20% Low Line:

$$C_5 = \frac{15mA}{0.8 * 160 * 2 * 60} = 0.975uF$$

- Assume 20% Tolerance Cap

$$C_5 = \frac{0.975uF}{0.8} = 1.21875\ uF \quad use\ 1.2\ uF$$

- Resistor R16 limits the in-rush current when the circuit starts up. In normal operation its impedance has small effect on circuit in comparison to C5 impedance

$$I_{surge} = \frac{V_{pk}}{R16} = \frac{160}{220} = 0.72A$$

- Power Dissipation of R16 determined by steady state current through which is governed by C5

$$X_{C5\min} = \frac{1}{2 * \pi * f * C_{min}} = \frac{1}{2 * \pi * 60 * 1.2uF * 0.8} = 2763\ ohms$$

$$I_{C5RMS\ MAX} = \frac{V_{lineRmsMax}}{X_{C1Min}} = 120 * \frac{1.1}{2763} = 0.048\ A$$

$$P_{R1MAX} = I^2 * R = 0.048^2 * 220(1.1) = 0.56\ W$$

USE A 2W Resistor

- Cap C6 determines the output ripple voltage and the time for the output voltage to initially rise as it charges up from the limited current supplied by C5. It does not affect the magnitude of the output voltage.

- Assuming a diode conduction time of 4ms

$$\Delta V = I_{load} * \frac{\Delta t}{C6} = 15mA * \frac{(16-4)ms}{1000uF} = 0.18V$$

- Output voltage magnitude is determined by the average current supplied from C5, the load current and the load resistance in steady state. These average currents are balanced. As the load resistance increases the output voltage increases which in turn delays the conduction angle of D1 as the line voltage must increase to a value greater than the output voltage. This results in current through C5 decreasing. The output voltage continues to increase until the load current required and the average C5 current supplied are balanced. In the worst case of no load the circuit would act as a voltage doubler and the load would increase until 2X the line voltage which would prevent and current flow through C5. To prevent this condition a minimum load should always be present.

- A Voltage regulator is used to provide a tight output voltage. This regulator has a maximum input voltage of 20Volts. To avoid exceeding the 20V a 12V zener diode is connected across its input terminals. The impedance R16 and C5 will limit the zener current

Worst Case Start up Surge

$$\frac{160 - 12}{220} = 0.672A$$

- The worst continous zener current would be no load, min tolerance C5 and max tolerance Vline

$$I_{zmax} = (160(1.1) - 1.2)\left(2 * \pi * 1.2uF(1.2)\right) = 89mA$$

- This current would be a half sine with peak value of Iz max pk so average current would be

$$I_{Zavg} = \frac{I_{Zmax}}{\pi} = \frac{89mA}{\pi} = 28.3\ mA$$

$$P_z = 12(28.3mA) = 340\ mW$$

BELOW 500 mW rating

The following circuit, shown in Figure 27 was simulated with LT SPICE to verify the operation of the voltage sense circuitry.

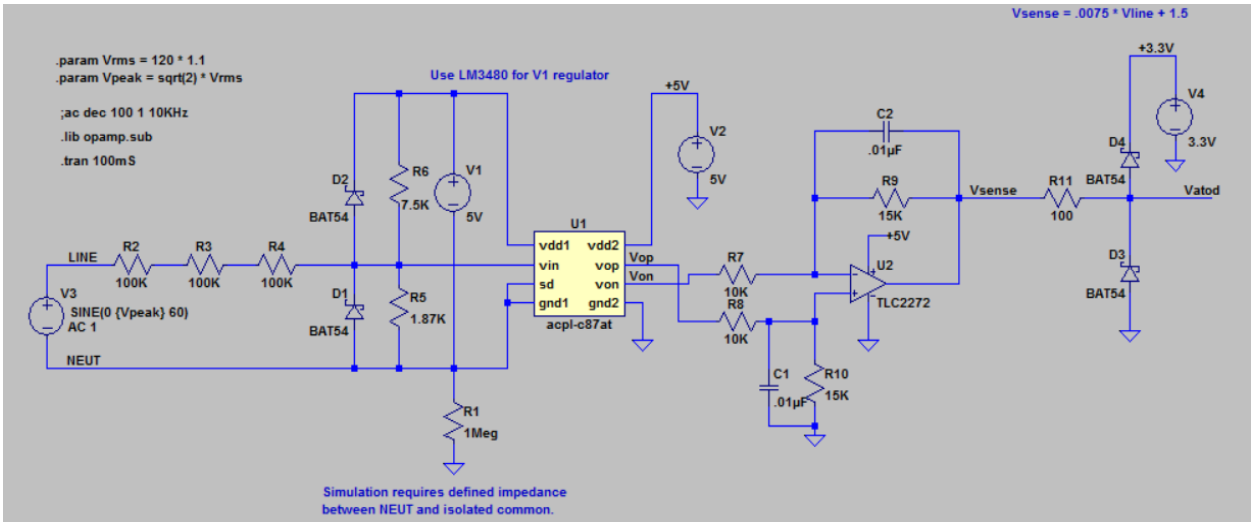


Figure 27 LT Spice Simulation of Voltage Sense

The simulation results from this simulation are shown in Figure 28. The top waveform is an AC waveform provided to the input of the circuit at 60 Hz ranging from 200 to -200 V. The bottom waveform shown the output waveform of the voltage sense circuitry. The output waveform ranges from 0 to 2V such that it can be sensed by the FPGA.

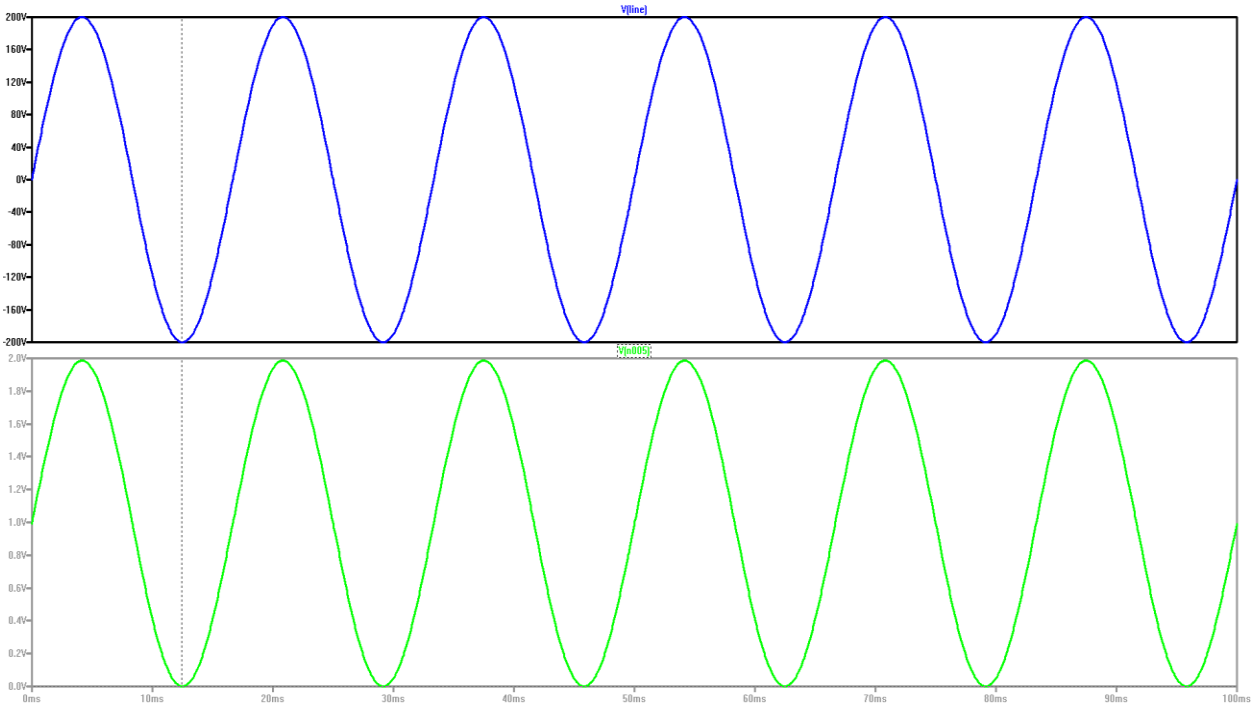


Figure 28 Output Waveforms from Simulation

The frequency response of the voltage sense circuitry was determined by sweeping the input voltage from 1Hz to 10 kHz. The results of this simulation are shown in Figure 29. The passband gain was seen to be -42.8 dB, with a phase shift of -3.306. The cutoff frequency was determined to be approximately 1 kHz.

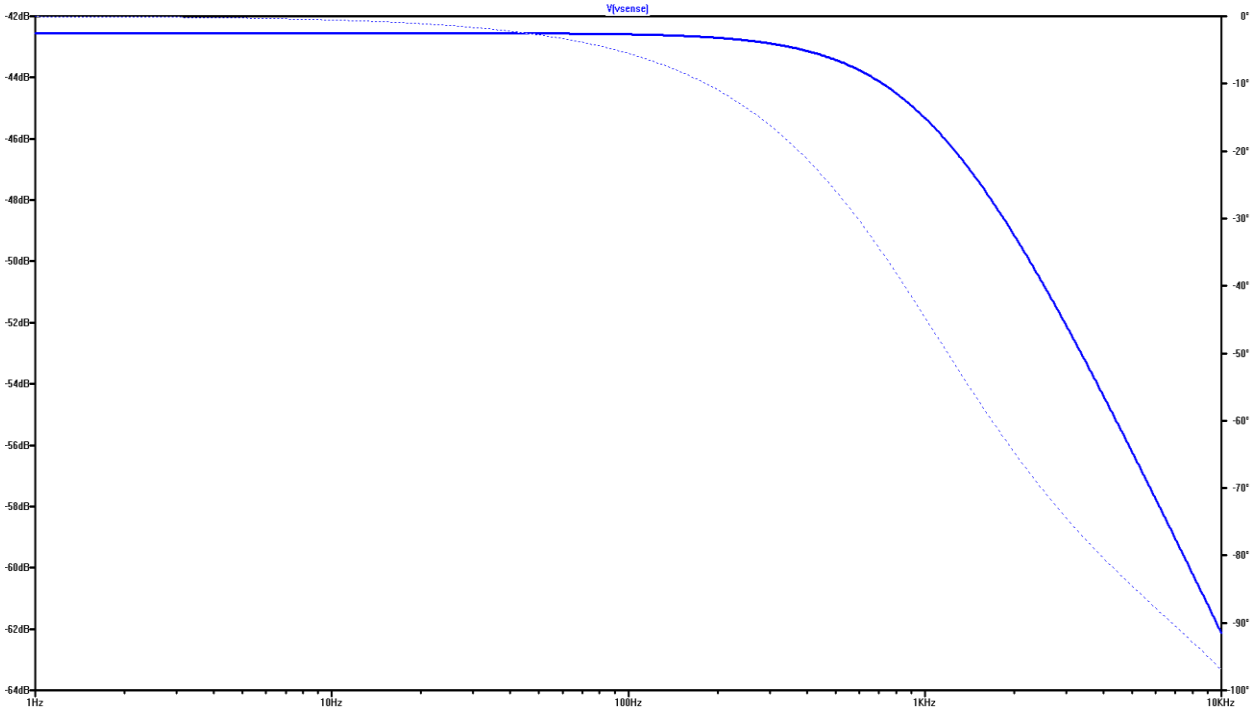


Figure 29 Frequency Response of Voltage Sense

Resistor Value Calculations for Amplifier:

Divided Down Offset Generation:

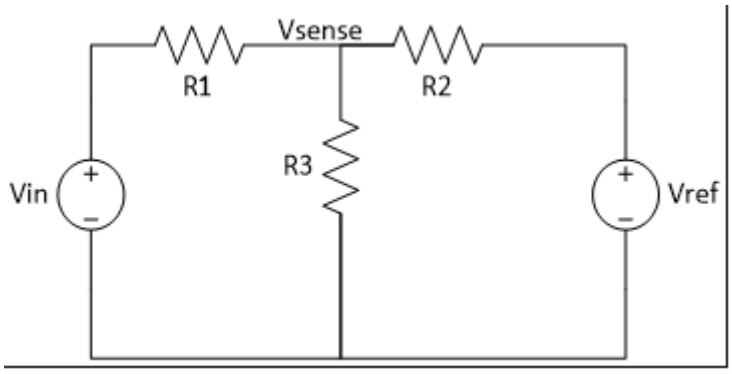


Figure 30 Voltage Offset Generation

$$V_{sense} = \frac{\frac{R2 * R3}{R2 + R3} * Vin}{R1 + \frac{R2 * R3}{R2 + R3}} + \frac{\frac{R1 * R3}{R1 + R3} * Vref}{R2 + \frac{R1 * R3}{R1 + R3}}$$

$$V_{sense} = \frac{R2 * R3 * Vin + R1 * R3 * Vref}{R1 * R2 + R2 * R3 + R1 * R3}$$

Want (Max input to ACPL-C87A is 2V)

Vsense = 2V at Vin = 200V

Vsense = 1V at Vin = 0V

Vsense = 0 at Vin = -200 V

Vref = 5V so:

$$(1)\ \ 1 = \frac{R1*R3*5}{R1*R2+R2*R3+R1*R3}$$

$$(2)\ \ 2 = \frac{R2*R3*200}{R1*R2+R2*R3+R1*R3} + \frac{R1*R3*5}{R1*R2+R2*R3+R1*R3}$$

Solving equation 1 and 2

$$R2 = \frac{R1}{40}$$

Pick R1 = 300k then R2 = 7.5k

$$R3 = \frac{R2}{Vref - 1 - \left(\frac{Vref}{Vin}\right)}$$

Detailed Design Notes:

- First stage before U1 op-amp shifts and scales line voltage such that 2V corresponds to 200V, 0V corresponds to 1V and -200V corresponds to 0V.
- U1 or ACPL provides isolation between the fused AC line voltage and the voltage to be transmitted to the ADC. This amplifier has a gain of 1.

Unless otherwise noted, I_A = -40° C to +105° C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3.3 V to 5.5 V, V_{IN} = 0 – 2 V, and V_{SD} = 0 V.

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Test Conditions/Notes	Fig.
DC CHARACTERISTICS							
Input Offset Voltage	V_{OS}	-9.9	-0.3	9.9	mV	T_A = 25° C	3, 4
Magnitude of Input Offset Change vs. Temperature	$\lvert dV_{OS}/dT_A \rvert$		2.1		µV/°C	T_A = –40° C to + 105° C ; Direct short across inputs.	5
Gain (ACPL-C87B, ±0.5%)	G0	0.995	1	1.005	V/V	T_A = 25° C; V_{DD2} = 5 V; Note 2.	6, 7
		0.994	0.999	1.004	V/V	T_A = 25° C; V_{DD2} = 3.3 V; Note 2.	6, 7
Gain (ACPL-C87A, ±1%)	G1	0.99	1	1.01	V/V	T_A = 25° C; Note 2.	6, 7
Gain (ACPL-C870, ±3%)	G3	0.97	1	1.03	V/V	T_A = 25° C; Note 2.	6, 7
Magnitude of Gain Change vs. Temperature	dG/dT_A		-35		ppm/°C	T_A = -40° C to + 105° C	8
Nonlinearity	NL		0.05	0.1	%	V_{IN} = 0 to 2 V, T_A = 25° C	9, 10
Magnitude of NL Change vs. Temperature	$\lvert dNL/dT_A \rvert$		0.0002		%/°C	T_A = -40° C to + 105° C	11

Figure 31 Voltage Sense Pramaters

- The signal then goes thru a differential amplifier which has a gain of 1.5 in the passband.

The equation for the output voltage based on the input voltage in the pass band range of the voltage amplifer is provided in the equation below. This first part of the gain (0.0049645VAC) is dependent on VAC and can be determined using super-position by shorting out the 5V reference supply. The second part (0.992) is the offset which can be determined using superposition and shorting out the VAC supply. The multiplication by 1.5 is due to the gain of the differential amplifier following the isolated amplifier.

$$V_{OT} = (0.0049645V_{AC} + 0.992) * 1.5$$

The voltage sense circuitry was tested at a voltage of 60 Hz at 120 V RMS. For this signal the measured output voltage was 2.78 (expected 2.715) and the minimum voltage was 220 mV (expected 224 mV). The results of this test are shown in Figure 32.

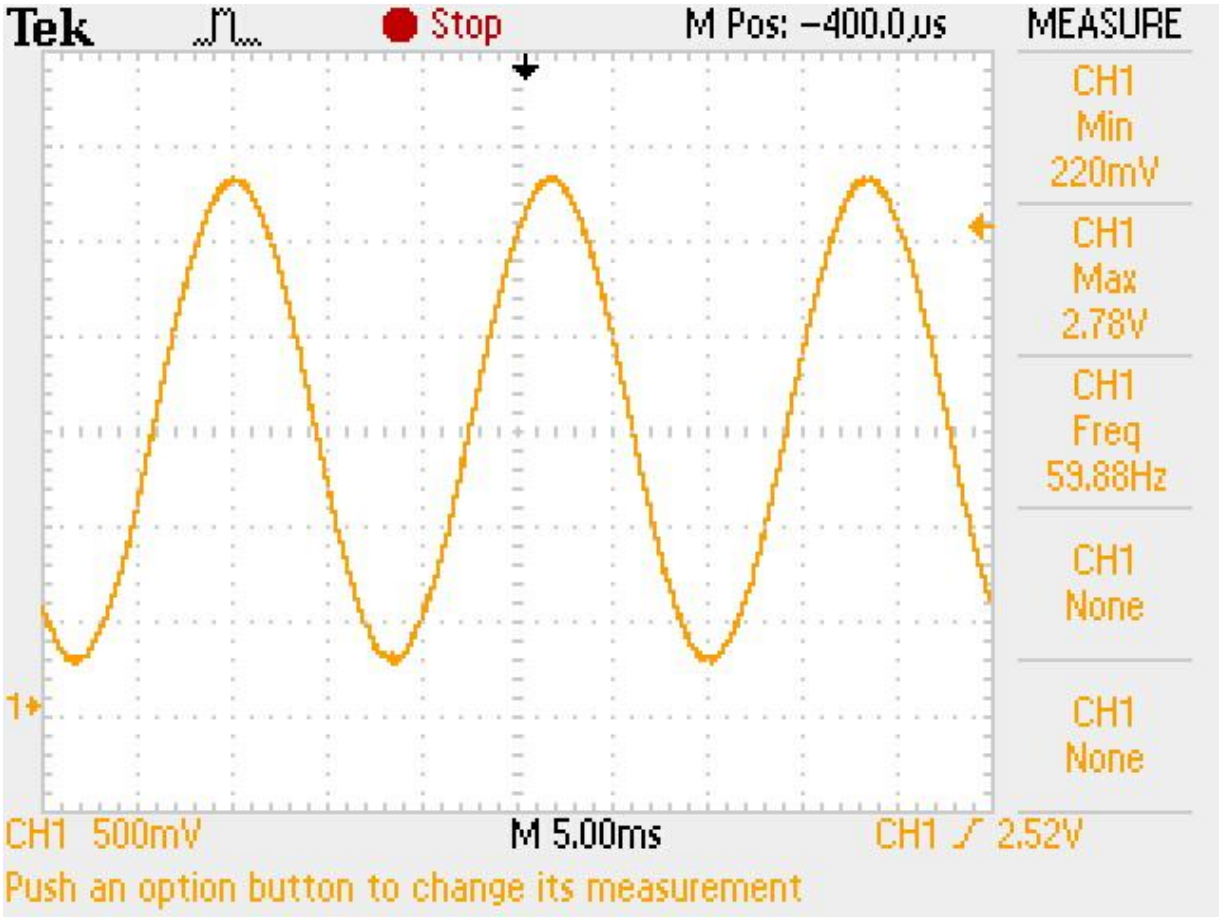


Figure 32 Voltage Sense Hardware Results

4.2.6 Surge Protection

The selected design consisted of a slow blow fuse and a MOV as shown in Figure 10. Both the fuse and the MOV will have no effect on the circuit during normal operation. In the event of a surge voltage transient, the MOV will dissipate any excess energy thus keeping the line voltage from exceeding 160V. In the event of the MOV failing as a short circuit the fuse will burn out thus breaking the path of current flow and protecting all circuit components.

4.2.7 Controller

The controller to be used is the DE-0 Nano development platform and is responsible for the tasks shown in Figure 34. Rectangular blocks within the controller correspond to firmware blocks, which will be developed, and oval block correspond to external hardware circuitry that the controller will interface with. The tasks, which are shown in Figure 34, are described as follows:

- Programming Interface – Provide an interface which can be used to program the Cyclone IV FPGA such that iterative development can take place. The DE-0 evaluation board contains an onboard JTAG port which will be used for this purpose.

- Current Monitoring – The current monitoring driver is responsible for handling the samples from the current sense hardware. The current sense hardware shall also decipher the results of the current sense hardware and produce a result usable for power calculations. The current is continuously monitored and compared against a desired current limit. If the sensed current exceeds the current limited value, the load switch will be turned off and a current fault will be latched.
- PLC Controller- Provides an interface to communicate off chip via the power line communication hardware. Tasks will include transmitting and receiving data between remote and main units. This will be achieved through the development of an I2C module which will allow the FPGA to communicate with the PLC evaluation boards via I2C. A finite state machine within the FPGA will also be developed which is capable of interacting with the PLC evaluation boards via the designed I2C interface. The FPGA will send a PLC message at a rate specified by the main module. The main module shall provide an interrupt to the FPGA which will notify it that it has a message to receive. The commands sent from the main module consist of a single byte of data (8 bits), with a 2 bit opcode and a 6 bit payload. The four supported op-codes are defined in Table 14. See the firmware appendix for a more detailed description of the command structure between the remote outlet module and the FPGA.

Table 14. Opcodes for FPGA / Main Module Communication

Opcode	Payload	Description
00	ON/OFF	Command to toggle load switch
01	Current limit value	Command to set current limit for load
10	Time between FPGA Transmissions	Command to Set variable TX rates
11	Dimming Value	Command to set level of dimming (not implemented in prototype model)

- Power Calculations – Provide power calculations based on current and voltage measurements. The FPGA will take instantaneous voltage and current samples every 200 us and use these value to determine the average power, the RMS voltage and the RMS current. Figure 33 shows the implementation of these calculations implemented within the FPGA. Everything within the FPGA block are calculations which are happening within the FPGA. Outside the FPGA block, represents that data processing which is occurring within the main module before the main module stores the results into the database. The FPGA exhibits a sliding window of 333 ms in which it performs all of these calculations. It is important to note that the FPGA makes no assumptions about the shape or frequency of the input waveforms and therefore the RMS calculations will return the expected values for any type of waveform. The waveform does not have to be sinusoidal. A limitation to the designed power algorithim is the fact that the window is not necessarily locked to the

frequency of the input waveform. Therefore the next step to improving algorithm accuracy would be to implement the ability to lock all calculations to the frequency of the input signal. But the sample time is a close multiple of 60 Hz so any error will be small

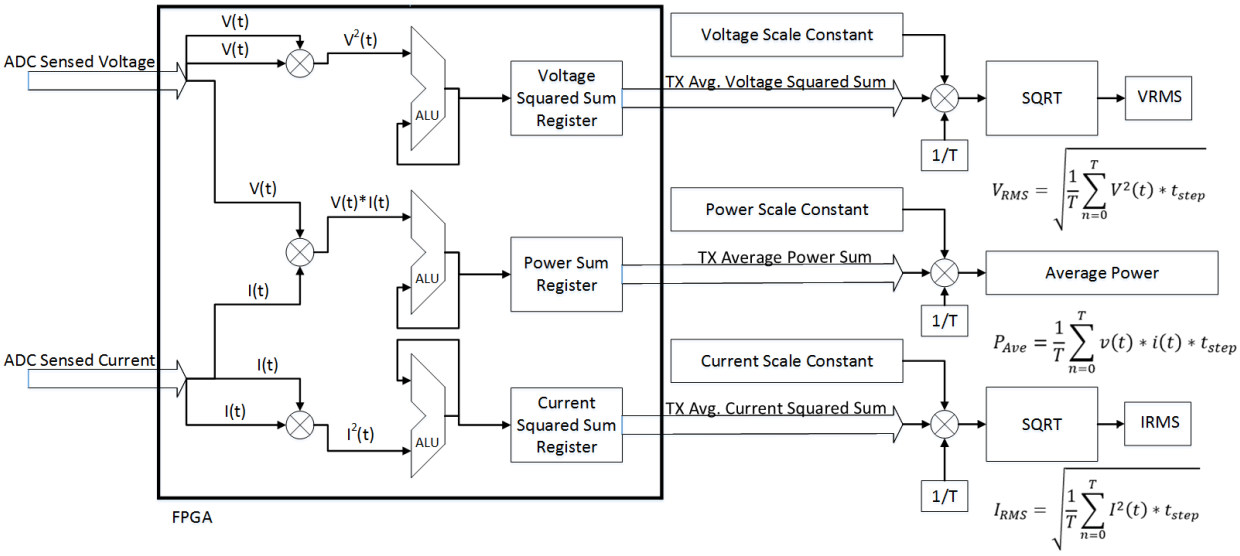


Figure 33 FPGA Calculations

- Load Switch Driver – Provides control of the load switch hardware, by commanding the load to the ON or OFF condition. This block will also be responsible for shutting the load switch off in the event of an over current/voltage fault.
- Voltage Monitoring Driver- The voltage-monitoring driver is responsible for handling the samples from the voltage sense hardware. The voltage sense hardware shall also decipher the results of the voltage sense hardware and produce a result usable for power calculations.

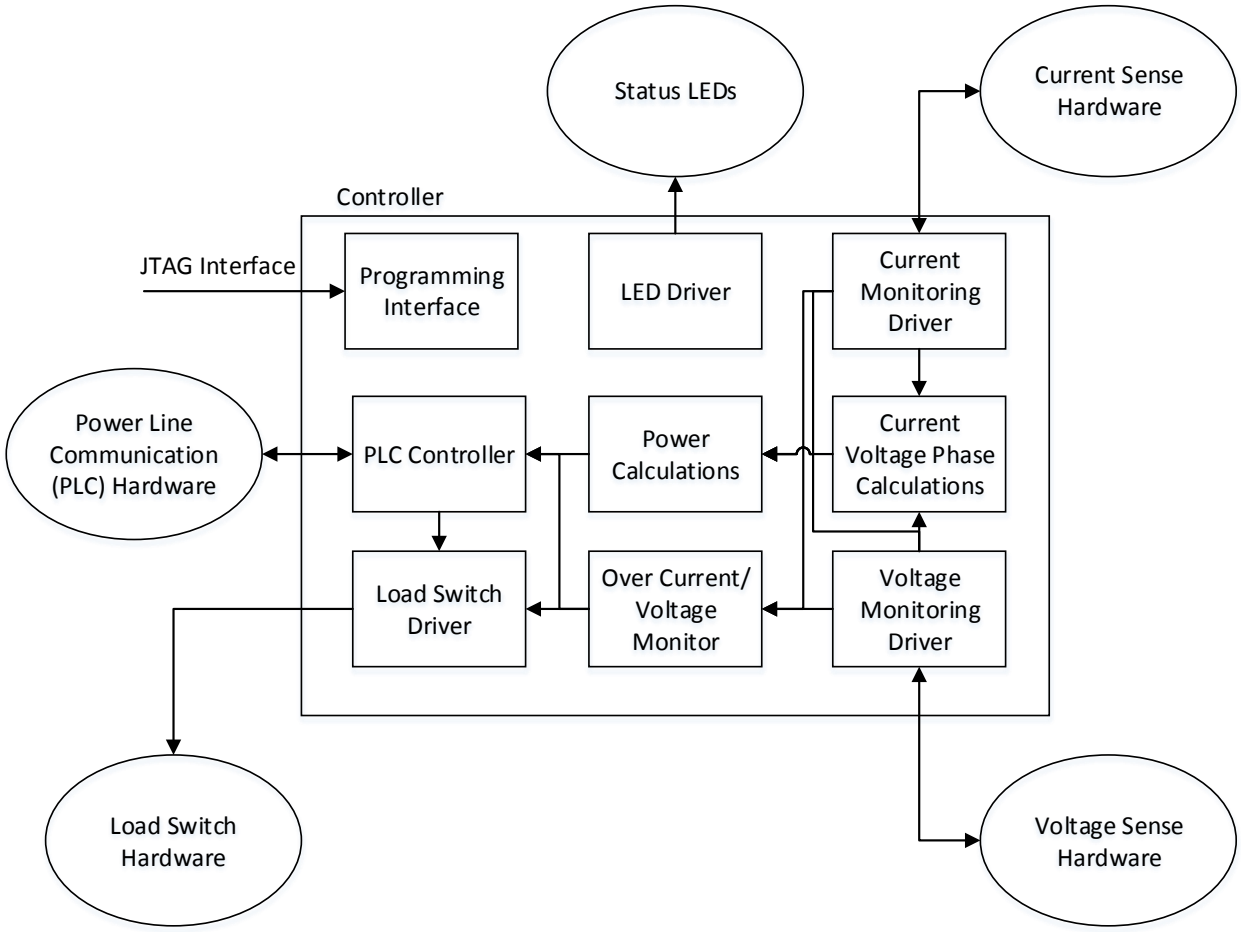


Figure 34. Controller Diagram

4.2.7.1 FPGA Controller Theory of Operation

4.2.7.1.1 FPGA Architecture and Design Process

The targeted device for the remote outlet FPGA is the Cyclone IV. The FPGA design uses VHDL to describe the parallel behavior of the systems hardware components. Since the FPGA VHDL code is targeted for an Altera device, Quartus II version 15.0 was used.

4.2.7.1.2 FPGA Design Hierarchy

The FPGA design is divided into different levels of hierarchy with a top level module and several lower level modules with additional levels of hierarchy found at each level. The top level module is wrapper_top.vhd. This module performs component instantiation of hierarchical blocks and implements assorted glue logic for the functionality of the inner modules.

In addition to the VHDL design files, pin planner was used to specify the I/O pin locations and drive strengths for the various inputs and output of the top level.

4.2.7.1.3 Design Modules

This section describes the design modules for each level of the design starting from the top and working down. Each module consists of an overview of the module, a description of the modules processes and component instantiations and also a table of the modules inputs and outputs.

4.2.7.1.3.1 top_wrapper.vhd

The top level of this design consists of all external input and output connections. The top level module instantiates the remote_outlet_module_top component and provides the necessary glue logic to allow it to function correctly.

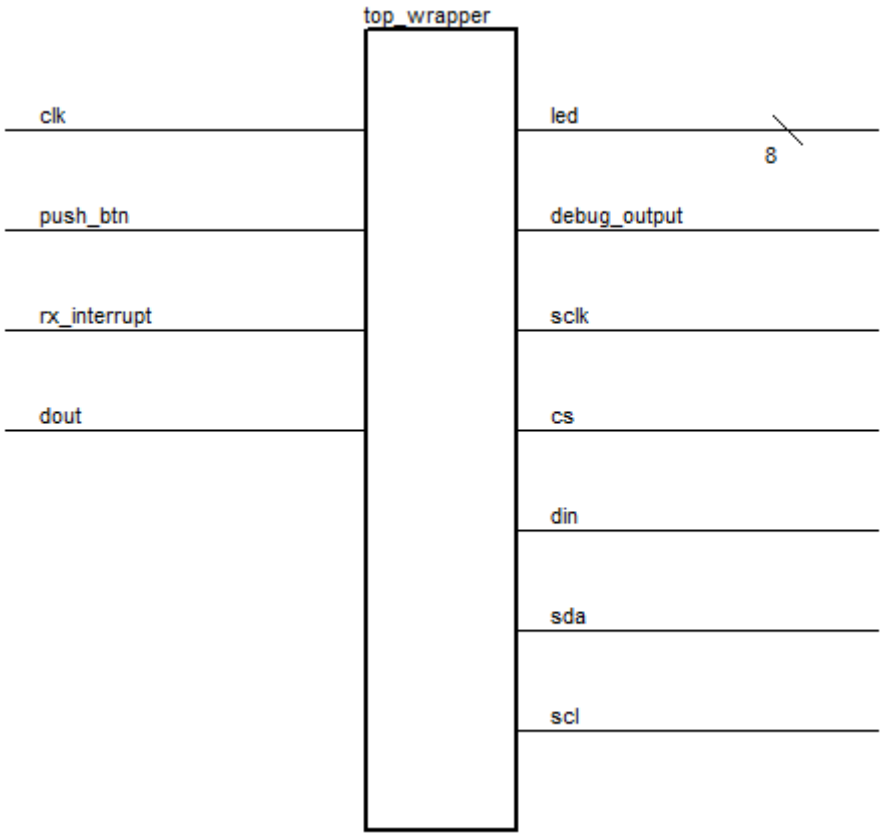


Figure 35 Entity Diagram for top_wrapper

4.2.7.1.3.1.1 Processes

None

4.2.7.1.3.1.2 Components

Remote_outlet_module_top.vhd : Top level component in which contains detailed implementation of the remote outlet design.

4.2.7.1.3.1.3 Input/Output

Signal	Direction	Signal Description
clk	Input	Input clock, 50MHz
push_btn[1:0]	Input	Push button input of DE-0 Nano Board, used for debugging purposes only
dip_switch[3:0]	Input	DIP Switch input to DE-0 Nano Board used for debugging purposes only
por	Input	Active high power on reset from hardware circuitry indicating status of remote outlet circuitry
rx_interrupt	Input	Active high pulse from PLC module indicating that a PLC message is avaliable for the FPGA to process
triac_drive	Output	Active high output to drive the ioslated triac drive.
led	Output	LED outputs used to display various status to the user
debug_output	Output	Debug output used for development purposes only. Allows internal signals to be viewed on oscilloscope
sclk	Output	ADC serial clock
cs	Output	ADC chip select
din	Output	ADC serial data input
dout	Input	ADC serial data output
sda	Bidirectional	Serial data line for I2C communication between FPGA and PLC
scl	Bidirectional	Serial clock line for I2C communication between FPGA and PLC

4.2.7.1.3.2 Remote_outlet_module_top.vhd

This module instantiates the block needed to control the analog to digital converter and the block which implements the PLC state machine controller.

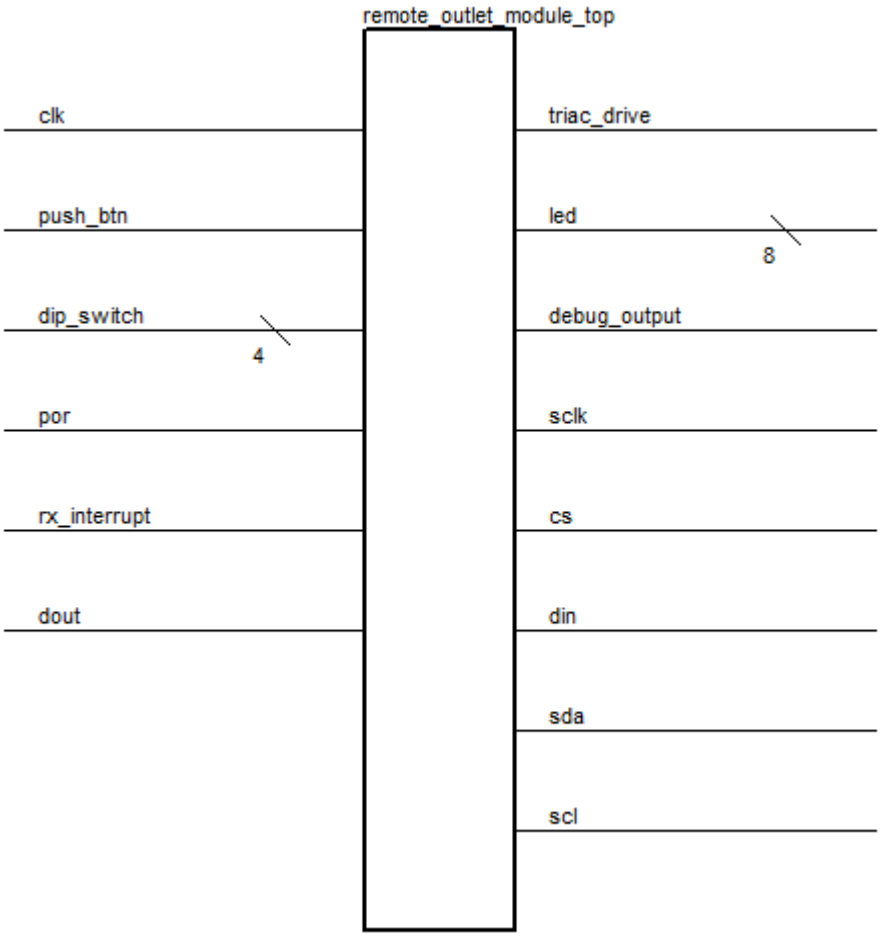


Figure 36 Entity for remote_outlet_module_top

4.2.7.1.3.2.1 Processes

Sample_rate_proc : Generate a 200us sample pulse signal to control the rate at which the ADC samples. This process synchronously generates a 200 us 5kHz pulse from the 50 MHZ clock.

Fsm_proc : Implements the finite state machine which gathers data from the ADC, (voltage and current data) and then performs the power calculation. The state machine is implemented as a single process synchronous state machine with an asynchronous reset.

Rst_gen_proc : Implements synchronization of the por asynchronous reset. This process also changes the rst logic such that the internals of the FPGA can use an active low reset instead of the active high reset which is implemented in hardware.

Set_state_proc : Implements logic to set the state logic for the load switch. Load switch state is synchronously updated with respect to the 50 MHz clock.

State_hand_proc : Implements logic to synchronously set output logic based on current load switch state. This state machine handles latching the load switch off if a current fault occurs.

4.2.7.1.3.2.2 Components

adc128s022_interface.vhd : ADC serial interface which communicates with Texas Instruments ADC.

plc_i2c_fsm.vhd : Implementation of plc state machine which handles all communications with main module via the Cypress PLC evaluation boards.

4.2.7.1.3.2.3 Input/Output

clk	Direction	Signal Description
clk	Input	Input clock, 50MHz
push_btn[1:0]	Input	Push button input of DE-0 Nano Board, used for debugging purposes only
dip_switch[3:0]	Input	DIP Switch input to DE-0 Nano Board used for debugging purposes only
por	Input	Active high power on reset from hardware circuitry indicating status of remote outlet circuitry
rx_interrupt	Input	Active high pulse from PLC module indicating that a PLC message is avaliable for the FPGA to process
triac_drive	Output	Active high output to drive the ioslated triac drive.
led	Output	LED outputs used to display various status to the user
debug_output	Output	Debug output used for development purposes only. Allows internal signals to be viewed on osilliscope
sclk	Output	ADC serial clock
cs	Output	ADC chip select
din	Output	ADC serial data input
dout	Input	ADC serial data output
sda	Bidirectional	Serial data line for I2C communication between FPGA and PLC
scl	Bidirectional	Serial clock line for I2C communication between FPGA and PLC

4.2.7.1.3.3 adc128s022_interface.vhd

This module instantiates the logic needed to communicate with the ADC converter. A finite state machine is implemented which is capable of sending commands to the ADC to specify conversion settings and then receive the requested conversion.

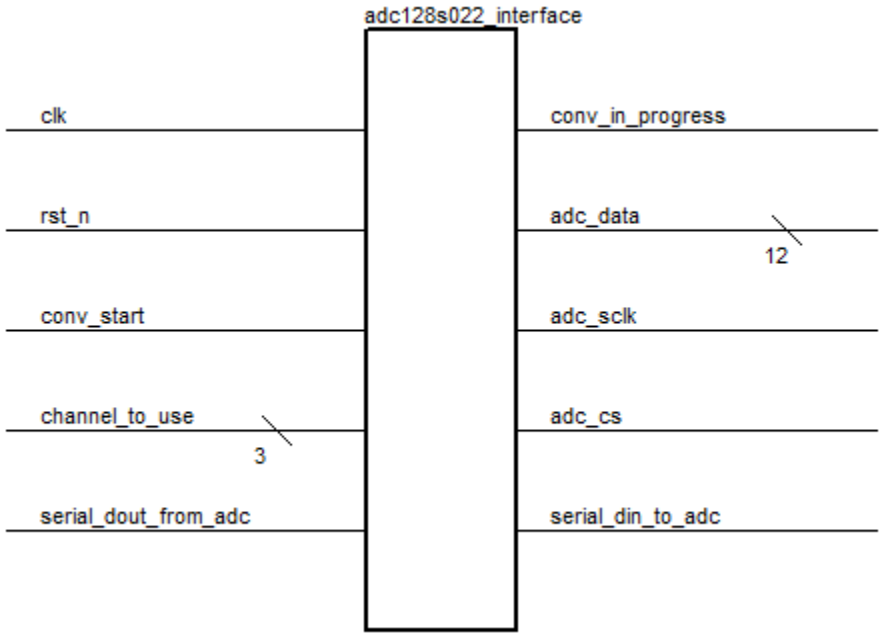


Figure 37 Entity for adc123s022_interface

4.2.7.1.3.3.1 Processes

gen_sclk_proc : Generate a 3.125 MHz clock needed for the ADC based of the 50 MHz clock.

fsm_sm_proc : Finite state machine to control inputs and outputs sent to the ADC. Finite state machine waits for a conversion to be requested, starts the conversion on the desired channel, and serially receives the data from the ADC converter. Upon conversion being done indicates that a conversion has been completed.

4.2.7.1.3.3.2 Components

edge_dect.vhd : Edge Detection which is used to detect the presence of a rising or falling edge on a given signal. Edge detection is done synchronous to the rising edge of the system clock (50 MHz). Any change in the signal faster than 50 MHz will not be captured.

4.2.7.1.3.3.3 Input/Output

clk	Direction	Signal Description
clk	Input	Input clock, 50MHz

rst_n	Input	Active low asynchronous reset
conv_start	Input	Input to request an ADC conversion. All conversion details are latched in on the rising edge of this input
channel_to_use[2:0]	Input	Select the channel of which to convert
conv_in_progress	Output	Indicate the status of the ADC. A '1' shall indicate that a conversion is in progress. On the falling edge of this signal, the requested conversion is complete and the data is valid.
adc_data	Output	12-data bits from the ADC converter representing the digital value of the sensed analog voltage
serial_dout_from_adc	Input	ADC serial output data
adc_sclk	Output	Serial clock provided to ADC, which governs speed at which samples can take place
adc_cs	Output	ADC chip select
serial_din_to_adc	Output	ADC serial input data

4.2.7.1.3.4 edge_dect.vhd

This module implements both rising and falling edge detection by clocking a signal and comparing the past value of the signal with the present value. The hardware implementation of this module is shown below.

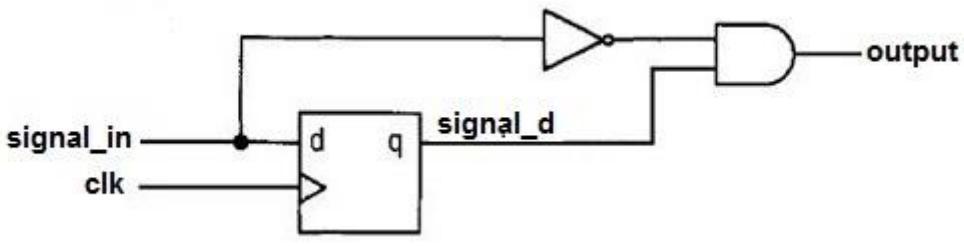


Figure 38 Edge Detector Hardware Implementation

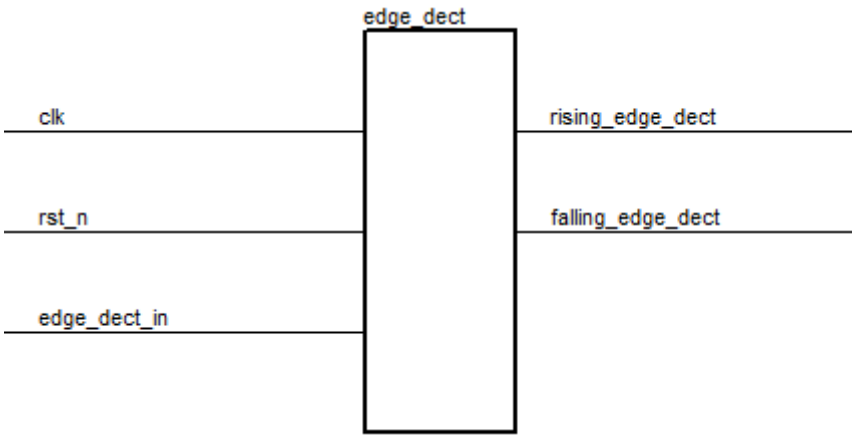


Figure 39 Entity for edge_dect

4.2.7.1.3.4.1 Processes

Input_shift_proc : Shifts in the input signal synchronously on the rising edge of the clock.

edge_dect_proc : Compares present signal value with previous signal value and determines if rising or falling edge has occurred. Output logic is registered synchronously to clock.

4.2.7.1.3.4.2 Components

None

4.2.7.1.3.4.3 Input/Output

clk	Direction	Signal Description
clk	Input	Input clock, 50MHz
rst_n	Input	Active low asynchronous reset
edge_dect_in	Input	Signal of which to perform edge detection on
rising_edge_dect	Output	Output indicating presence of rising edge on a signal. High iff a rising edge is detected
falling_edge_dect	Output	Output indicating presence of falling edge on a signal. High iff a falling edge is detected

4.2.7.1.3.5 plc_i2c_fsm.vhd

This module implements the state machine to handle interfacing with the Cypress interface PLC boards. Functionality includes TX and RX between main module and FPGA.

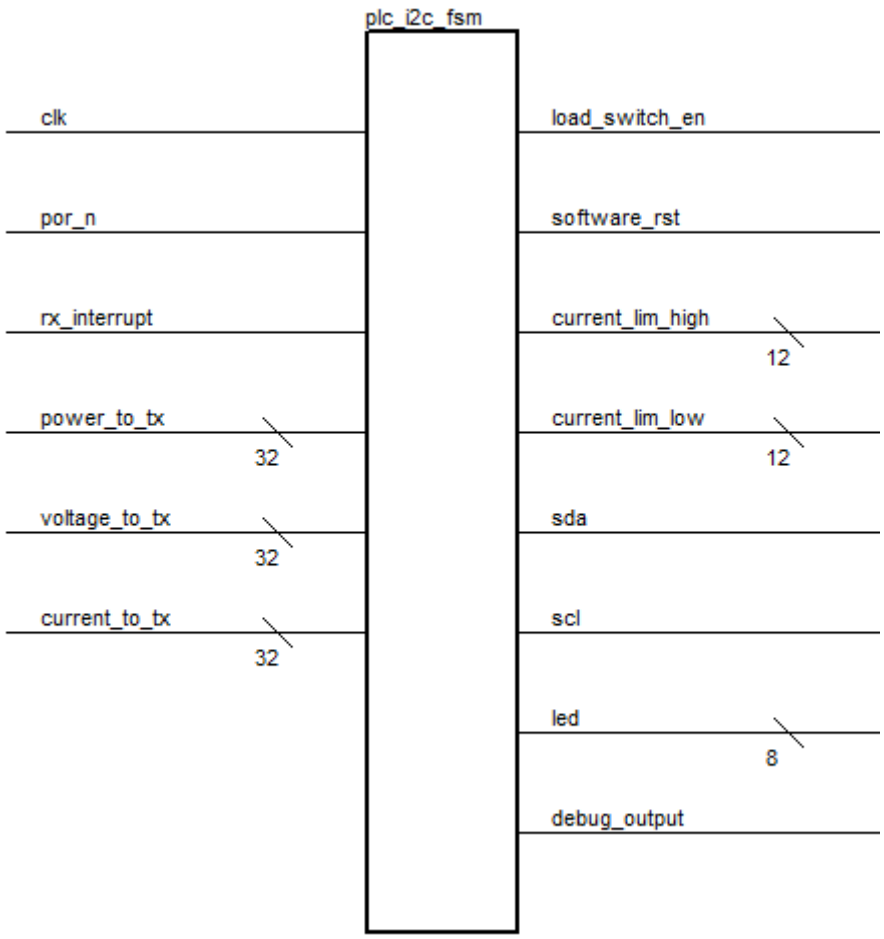


Figure 40 Entity for plc_12c_fsm

4.2.7.1.3.5.1 Processes

gen_1kHZ_clock : Generate 1 KHz clock based of 50 MHz system clock which is used for timing within the FPGA. This slow count is the basis for several counters within this module.

gen_tx_pulse : Generate a TX pulse which can range anywhere from 1 second to 16.75 second. This pulse is variable based on the message values received from the I2C interface. Value received from I2C shall be 6 bits long with a resolution of 250 ms per bit.

tx_interrupt_proc : Goes high on a rising edge of tx_pulse and goes low after interrupt is processed. When the generated RX pulse goes high the finite state machine in charge of TX and RX knows that a TX must be performed with the latched data.

rx_interrupt_proc : Generate a RX interrupt. This pulse goes high when the PLC rising edge interrupt is active. The PLC interrupt is active low. When the generated TX pulse goes high the finite state machine in charge of TX and RX knows that a RX must be performed and the new message must be processed.

plc_i2c_fsm : Finite State machine to handle RX and TX between FPGA and PLC boards. This module uses the I2C module to send and receive commands. State machine initially in idle, and waits until a tx or rx interrupt is generated. If interrupts for tx and rx occur at the same time, rx has priority since receiving commands is more important that sending data back to the main module. When RX interrupt handling is complete TX interrupt will then run.

If a tx interrupt occurs:

- Data to transmit is latched
- A PLC write is requested
- Data payload is serially shifted to the I2C module and I2C burst writes are enabled.
- Wait until I2C module indicates that it has completed the I2C write.
- After writing payload data write command to PLC module to request a PLC transmission.
- Send parameters of PLC write
- Wait until RX PLC write command is processed.
- Go back into the IDLE state

If an rx interrupt occurs:

- Write to I2C interface to indicate that FPGA wants to read data from PLC module.
- Wait until PLC module acknowledges FPGA request.
- Collect data which PLC module provides.
- After receiving data, process op-code to determine what message is from main module.
- Based on op-code, handle payload and update necessary status of the outlet module based on message.

4.2.7.1.3.5.2 Components

i2c_master_djm.vhd : I2C master component which is capabale of reading and writing to other I2C devices.

4.2.7.1.3.5.3 Input/output

clk	Direction	Signal Description
clk	Input	Input clock, 50MHz
por_n	Input	Active low asynchronous reset
rx_interrupt	Input	Interrupt signal form PLC which indicates that a PLC message is available for the FPGA

power_to_tx[31:0]	Input	32-bit value representing power to transmit to the main module
voltage_to_tx[31:0]	Input	32-bit value representing voltage to transmit to the main module
current_to_tx[31:0]	Input	32-bit value representing current to transmit to the main module
load_switch_en	Output	Status of load switch to be set by above level module based on commands from main module
software_rst	Output	Debug rst signal which provides the ability for main module to reset firmware
current_lim_high[11:0]	Output	Current Limit high value based on current limit requested from main module
current_lim_low[11:0]	Output	Current Limit low value based on current limit requested from main module
sda	Bidirectional	Serial data line for I2C communication between FPGA and PLC
scl	Bidirectional	Serial clock line for I2C communication between FPGA and PLC
led	Output	LED output used to display FPGA status
debug_output	Output	Debug Output used to allow for internal signal visibility during debug

4.2.7.1.3.6 I2c_master_djm.vhd

This module implements the I2C bus protocol allowing the FPGA to function as a master for I2C transactions. This module was obtained from the following location: https://eewiki.net/pages/viewpage.action?pageId=10125324#I2CMaster(VHDL)-AdditionalInformation. Slight modifications were made to ensure desired synthesis functionality would be met with Cyclone IV FPGA. Since this core was obtained, no further design description is provided. Refer to the aforementioned link for a detailed summary of implementation.

4.2.7.2 FPGA Simulation Verification

Prior to synthesizing the FPGA design, a detailed simulation environment was created. This allowed many issues to be discovered in simulation and also provided a means of re-creating issues that would occur in hardware such that they could be adequately debugged and corrected.

In order to create a simulation environment for the VHDL all of the inputs to the FPGA and the components that the FPGA interfaced with had to be modeled. By modeling all of the system components in VHDL all of the synthesizable code was able to be tested thru simulation.

4.2.7.2.1 ADC Bus Functional Model

In order to simulate transactions with the ADC converter a bus functional model of the ADC was developed. This bus functional model mimicked the behavior that was seen from the hardware ADC. This allowed the developed serial interface to be tested in simulation. The entity for the bus functional ADC is shown below.

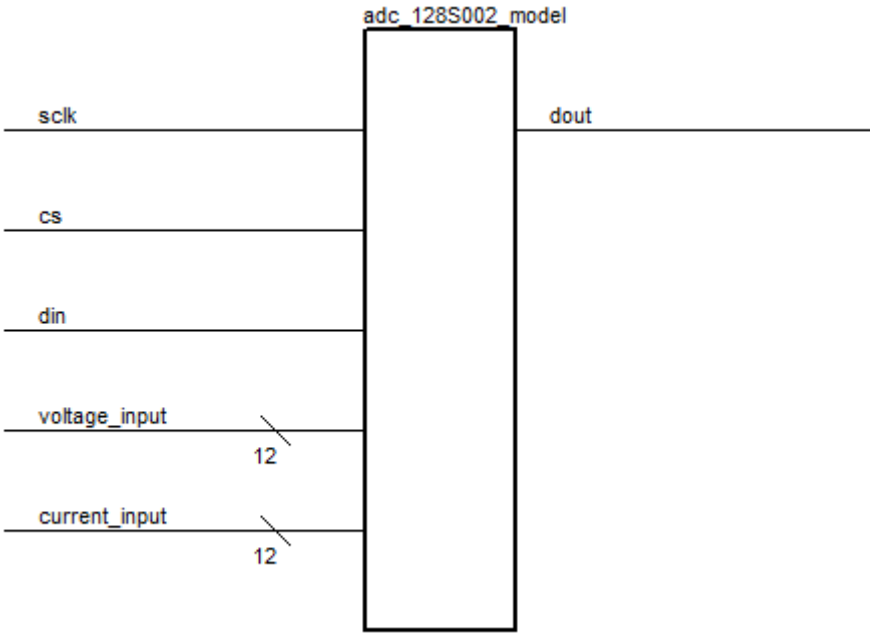


Figure 41 entity for adc_128s002_model

4.2.7.2.2 System Testbench – sys_tb.vhd

The complete system testbench instantiated the remote outlet top level VHDL code, and the bus functional model of the ADC. The testbench then generated analog waveforms corresponding to the sensed voltage and current. These current and voltage waveforms were easily adjustable allowing the design to be tested at various load conditions. This process greatly accelerated the design process as the increased visibility into the complex design allowed for problems to be easily debugged and corrected.

4.2.7.2.2.1 Processes

time_gen_proc : Generate time step. This process determines the step to generate the “analog” voltage.

Voltage_sense_proc : Generate voltage sense signal and corresponding digital value. This value is then used by bus functional model of ADC and serially shifted into design.

Current_sense_proc : Generate current sense signal and corresponding digital value. This value is then used by bus functional model of ADC and serially shifted into design.

clk_gen : Generate 50 MHz clock signal for system clock.

por_gen : Generate POR rst signal to simulate how hardware will handle POR signal upon power up.

rx_proc : Generate rx_interrupt signal to simulate interrupts received from the PLC module

4.2.7.2.2.2 Components

remote_outlet_module_top.vhd : Top level of the design. This was the unit under test.

adc_128S002_model.vhd : Bus functional model of the ADC.

4.2.8 FPGA Communication Interface Circuits

The I/O of the FPGA operated at logic levels of 3.3V. The I/O of the PLC module operated at logic levels of 5V. Since these two modules needed to communicate interface circuitry was needed to allow for level-shifting between the two modules.

4.2.8.1 I2C Level Shifting

A bi-directional I2C level shifter was used so both the FPGA and the PLC module operated at their native voltages. This was done using two NMOS transistors, as shown in the schematic of Figure 42.

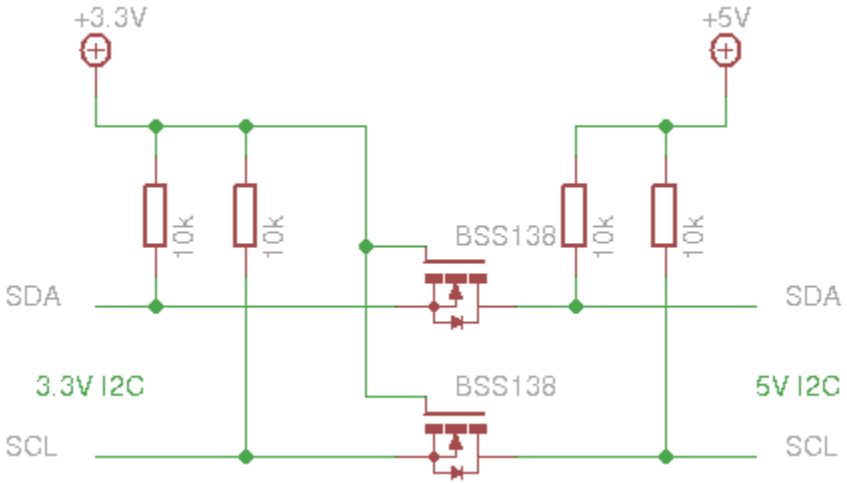


Figure 42 I2C Level Shifter

To understand how the aforementioned circuit works, it is important to have an understanding of how I2C communication works. When an I2C device is sending data it sends a '0' by driving the bus low. However, when it wants to send a '1,' the bus is "let go" (set to a state of high 'Z') and the pull up resistor pulls the bus to the supply voltage. When the 3.3V master drives the

SDA signal low there is a positive gate to source voltage across the pass transistor which allows the low logic level to pass to the 5V slave. When the 3.3V master lets go of the bus (to indicate a logic '1') the pull up resistor pulls the source of the pass transistor to the same potential as the gate. This turns of the pass NMOS transistor. Therefore on both the master and slave side the output voltage will be determined by the voltage which is connected to the pull-up resistor. This allows two I2C devices operating at different potentials to both determine a logic '1' at the same time. When selecting pull-up resistors it is important to not select resistors that are too large as large resistors limit the amount of current when switching from low to high, which slows down the switching speeds.

4.2.8.2 RX Interrupt Level Shifting

To prevent the FPGA from having to poll the PLC module, the PLC module was set up to interrupt the FPGA whenever it received a message. Since the GPIO available on the PLC module operated at 5V an interface circuit was needed to convert this value to logic levels compatible with the FPGA. A simple resistive voltage divider was initially used but was deemed to be a poor design choice as the 5V GPIO was seen to fluctuate anywhere from 5V to 6.2V, which could cause either an overvoltage on the pins of the FPGA, or an voltage that was in the unknown region of the FPGA. To remedy this the circuit of Figure 43 was used to convert from 5V interrupt levels of the PLC to 3.3V levels of the FPGA.

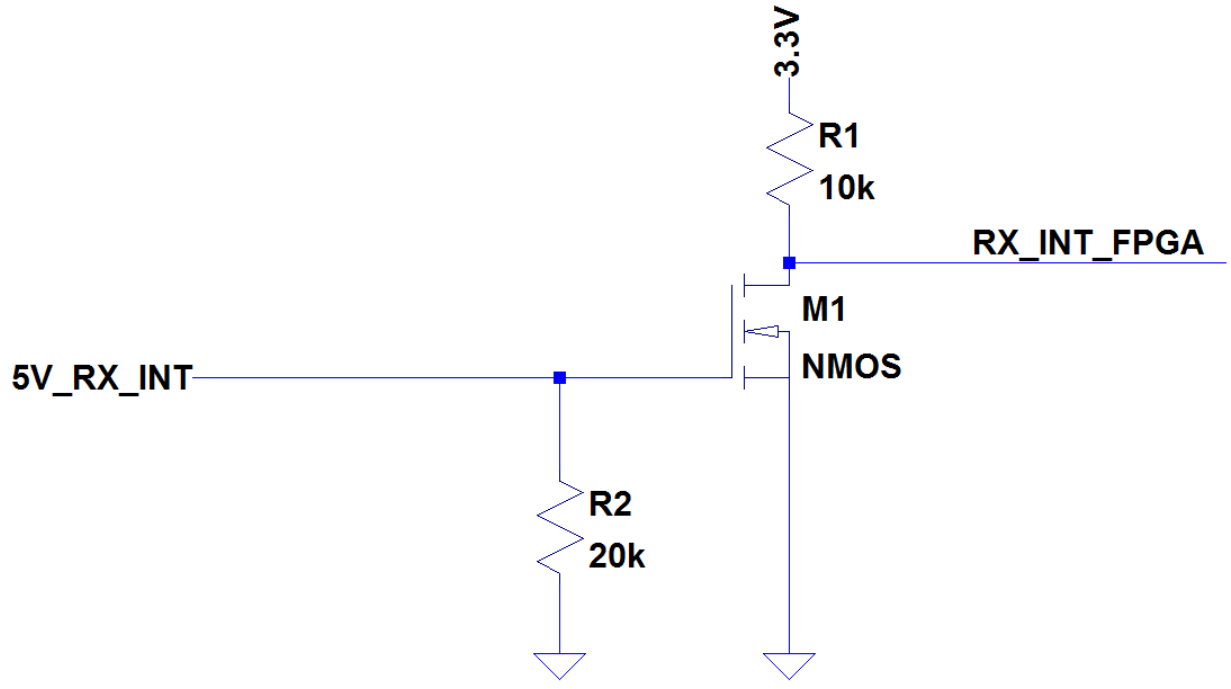


Figure 43 RX Interrupt Circuit

When the 5V_RX_INT is not active (GND) the NMOS transistor M1 will be OFF as it will have agate to source of 0V. Therefore there will be no current flow through R1 which will pull the RX_INT_FPGA line to 3.3V. When the 5V_RX_INT is asserted (5V) the NMOS transistor

NMOS will turn ON. This will allow a current flow through the R1 resistor to GND. Since there is no voltage drop across the NMOS (ideally) all of the 3.3V is dropped across R1 and the RX_INT_FPGA pin goes low. It is important to note that this circuit provides a signal inversion of the interrupt. This is easily handled within the FPGA by making the RX interrupt active low.

4.2.8.3 Remote Outlet Hardware Prototype

The remote outlet module hardware was prototyped by breadboarding the critical power line interface components. Figure 44 shows the prototyped analog outlet hardware along with identifying all important blocks in the hardware design.

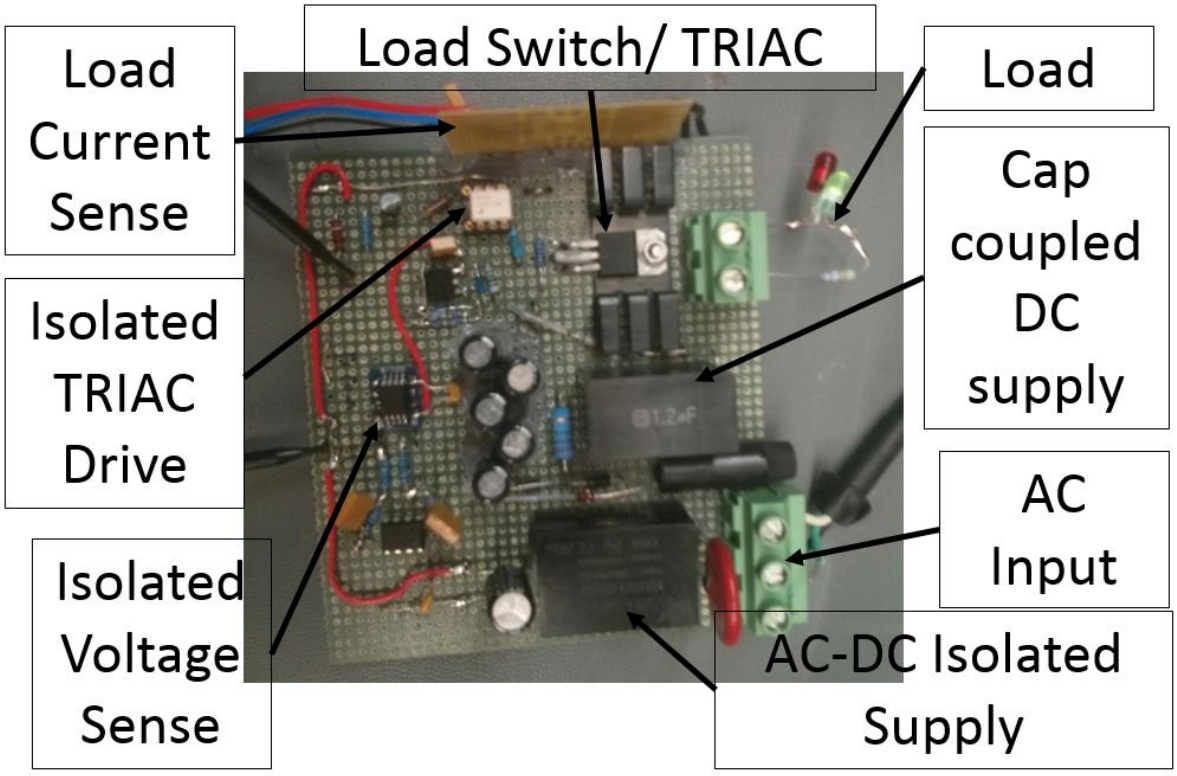


Figure 44 - Prototype Hardware for Remote Outlet Modules

4.3 POWER LINE COMMUNICATION

Because of concerns about achieving the minimum data rate, it was determined that power would be measured and transmitted for single gangs (2 outlets – not for each single outlet). This makes it so the system could support roughly twice the number of outlets for a given data rate. There are many formats and contents of data that could be transmitted to convey power usage. The two primary choices for power usage transmission are either transmit only power or transmit three components – as current, voltage, and power. While the three component transmission would utilize more data, it would allow for users to view data relating to voltage levels, which is a unique

feature that could help users identify issues with wiring and connections. For this reason, three component power was selected for the values to be sent back to the main module via the PLC. For transmission of three components, many of the components could be reduced to save on the number of transmitted bits. While these reductions were not implemented in the prototype, they would be implemented to optimize the production devices. Voltage could be transmitted as a difference from 100 V (or a similar number) utilizing a 5-bit number to range between 100 & 131 volts. Current could be specified with an accuracy of about 16.5 mA using a 10-bit resolution, and the power could likewise be reduced, which would greatly reduce the number of transmitted bits compared to three component power with no reduction (12 Bytes in the prototype implementation).

In the design, the remote module's PLC was configured to transmit its physical address in its packet header to the main module, in order to provide a unique identification of the outlet to the main module. Each PLC is preconfigured with the logical address of the main module (a hardcoded value from the factory) so they can immediately begin transmission without handshakes to the main module when installed. It is critical that the remote module transmits its physical address in order for the main module to realize that there is a newly installed outlet, and to identify it.

The physical address of the transmitting device can be obtained from the packet header when using the Cypress PLC chip, which means it does not need to be transmitted redundantly within the packet payload. For the chosen chip, the packet header is 13 Bytes when transmitting the device's physical address instead of its logical address. Provided the number of outlet gangs M=50, packet header P=13 Bytes, the three component power is represented in 12 Bytes, and the measurement transmission frequency is F_S=once every 15 seconds, the required minimum data transmission rate would be 667 bps which is well below our specified 2400 bps according to Equation 2. This does not include any form of the compression techniques aforementioned.

$$B > M * (P + V + I + P) * (F_S) \quad \textbf{(2)}$$

To allow for near real-time viewing of data, it would be practical to have the ability for the main module to request a non-default transmit rate (default of 1 transmission every 15 seconds). For example, all modules could transmit once every 15 seconds, but the main module could request a certain gang (or group of gangs) send at a rate ranging between once every 1 second to once every 15 seconds. Assuming the default frequency is F_D, and the real-time (fastest) viewing frequency is F_R, and the maximum number of items in a real-time viewing group is M_R (And also assuming all other outlets are default time), then Equations 2 can be modified as shown in Equation 3.

$$B > (MF_D + M_R F_R - M_R F_D) * (P + V + I + P) \quad \textbf{(3)}$$

Assuming the prior assumptions, and that the biggest real-time group with a frequency of one transmission per second is 5 modules, the minimum bandwidth for a perfect transmission, no collision model would be 1600 for a 3 component power transmission model. Further, if the data rate is slightly too high during implementation, the data being transmitted may be compressed, which should drastically reduce the required data rate.

The pinout of the CY8CPLC20 28-pin SSOP is shown in Figure 45.

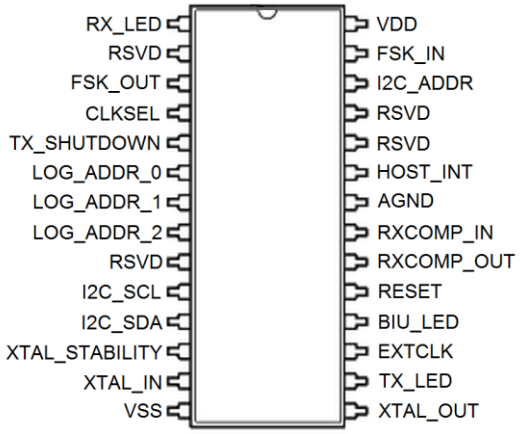


Figure 45. CY8CPLC10 Pinout

Because PLC is a mature technology, the operation of the PLC chip is relatively straightforward. The chip is connected to the FPGA using I^2C to communicate to the PLC chip. Each module will be equipped with the chosen PLC chip, which will simply act as a black box system to pass information from the outlet modules to the main module, and vice versa. A simplified view of the system is shown below, in Figure 46.

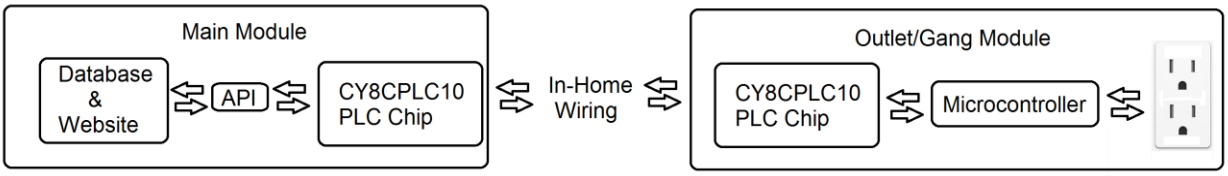


Figure 46. PLC System Overview

Figure 46 shows that each module is equipped with one of the selected PLC chips, and uses it as an interface with other modules. In the case of the Main Module, it interacts with each of the outlet modules via the PLC chip. Each outlet module need directly interact only with the main module however. Each outlet module consists of a "gang" (2 outlets) equipped with a single FPGA, a single PLC chip, coupling, control, and measurement hardware. At the interval specified by the Main Module, the Outlet modules' FPGA will average the power consumption and send the data to the Main Module via the PLC chip. The transmission frequency will be variable, so that the Main Module may request real-time data from individual modules. The Main module will constantly receive data from remote modules and update its database, but will also be able to issue commands to turn the remote outlets on and off. Figure 47 summarizes the interactions that are necessary with the PLC connection.

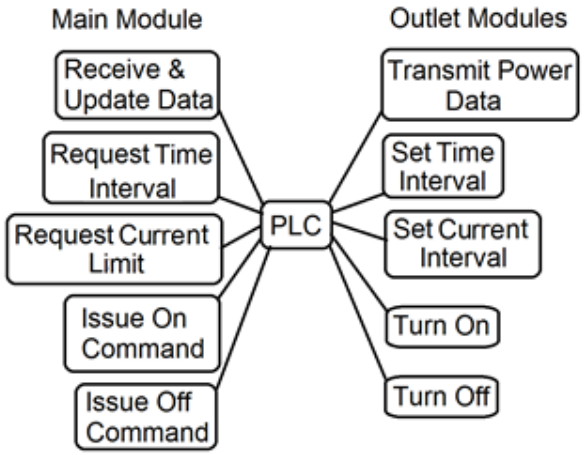


Figure 47. Commands & Updates Facilitated by PLC

The opcodes utilized to transmit these messages are of no concern to the actual PLC device itself, since it only needs to forward received messages as directed. The table of opcodes used can be found in Table 14. Receiving and transmitting data on the power line requires that the PLC be coupled with the mains wiring. For the production units, these will not automatically be integrated as part of the PLC development board. There are two main coupling types under consideration for the production unit, which will be chosen based on the other choices in the design. Utilization of transformers will isolate the PLC while coupling it with the main wiring, and will be utilized if the FPGA is isolated as well. If the FPGA is not isolated, then the PLC will be coupled capacitively. Such couplings are already widely available in application notes for many of the discussed chips. Utilization of transformers throughout the design would isolate the design at the expense of space, but would help to protect the system from damage. However, if the FPGA's supply is not isolated, then the space used at the transformer coupling of the PLC chip would be wasted as it would not be isolated anyways, which is why the selection is dependent on the FPGA's coupling. For the Main Module, it is expected to be coupled with a transformer, as the data center should definitely be isolated and protected from the power line. For the prototype modules designed, a Cypress PLC development board was utilized, eliminating the need to design the coupling, although this information is valuable for production devices.

4.4 Main Module

4.4.1 Communication Interface

Similarly to the FGPA, the Pi communicates with the PLC module via I2C communication. The logic level of the Pi operates at 3.3V, while the PLC module operates at 5V. The same level shifter design used between the FPGA and the PLC module of the remote outlet module side is used between the Pi and the PLC module of the main module side.

In addition to the I2C level shifter, another level shifting circuit was used for the RX interrupt signal, generated by the PLC module.

4.4.2 Measurement Recording

As with the FPGA on the remote outlet module side, the Pi does not poll for a new message received on the PLC module. Instead, a GPIO interrupt is setup on pin 21 of the Pi. When the PLC module receives a new message (measurement), the interrupt on the Pi is then triggered. Upon trigger, a callback function is called which performs the following steps:

1. Read the source address of the received message
    a. If the source address equals 0x0, then a blank message has occurred. This typically happens when the PLC module is turned on after the Pi.
2. Check the database to see if a remote outlet module with that address already exists
3. If the source address is not in the database, perform the next steps:
    a. Read the source address again.
    b. If the two source addresses are not equal, then an I2C read error has occurred and the measurement should not be entered.
    c. If the two source addresses are equal, a new outlet module entry should be created in the database with the read source address.
4. Read the 12-Byte measurement sent by the remote outlet module.
5. Perform the calculations necessary to determine the measurement values to be stored.
6. Store the measurements in the database, with the respective outlet ID for the remote outlet module.
7. Clear the New_RX_Msg bit in the PLC memory table.

The PLC module on the main module side is configured to accept a new message and store it only if the New_RX_Msg bit in the memory table is ‘0.’ If the bit is ‘1,’ then any messages send to the PLC module are discarded. Therefore, the Pi must manually clear that bit, in order to receive new messages from the remote outlet modules.

4.4.3 Command Sending

Commands from the main module to the remote outlet modules are sent via the web application. Depending on the command to be sent, an 8-bit message will be sent from the main module to the remote outlet module(s). The opcode table, seen in Table 14, contains the 2-bit opcode at the start of the message. The remaining 6 bits are either hardcoded values for the on/off commands, or the payload value for the current limit/time interval commands.

4.5 WEB APPLICATION

4.5.1 Overview

The application will be constructed using the standard web application layer design where each part of the application is separated into layers that interact with each other. This reduces coupling

within the application and allows for easy maintainability and upgradability. Figure 48 shows an example of this layering from Microsoft.

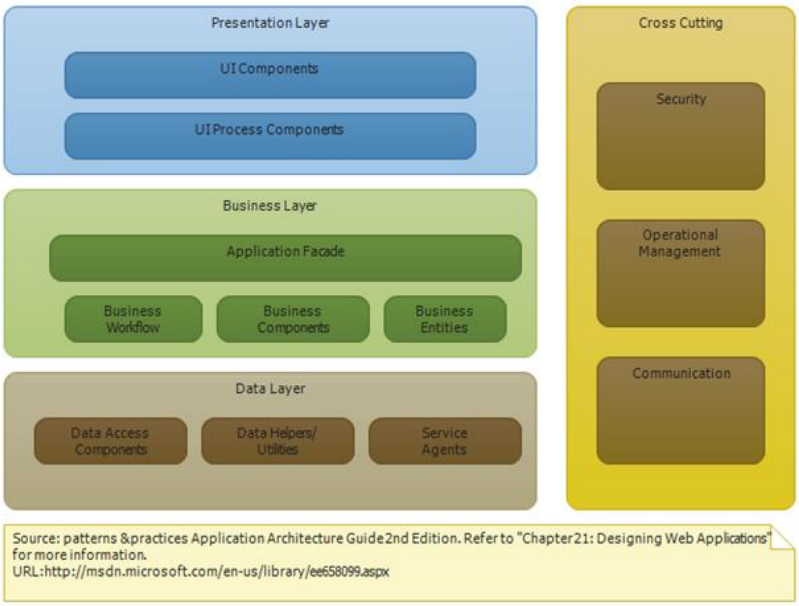


Figure 48. Web Application Layering

Figure 48 shows that there are three main layers and other components that interact with all of the layers. This is the typical design of a web application that is used by most in industry. The presentation layer (or UI layer) is where the user interface is implemented. This layer will include everything the user will see and interact with. So all the power consumption charts, the naming and grouping interface, and the scheduling or control interface will be implemented in this layer. The business layer (or service layer) is where the UI will communicate to get information or perform tasks the user requested. In this layer the user's requests from the UI layer will be processed and requests will be made to the data layer if needed. This layer also handles anything that needs to be displayed from the data layer. The service layer will process this information and pass it up to the UI layer. In the data layer is where the actual requests, and queries to the database are performed. There is usually a request from the service layer that requires data to be fetched or modified. The data layer handles parsing these requests into queries, running the queries against the database, and returning the results. The right-hand box shows some components that integrate with each layer such as security and communication. This design makes the application as loosely coupled as possible, which is beneficial. A loosely coupled design is easier to maintain, upgrade, and allows for the development work to be divided easily. This design will also ensure the user interface is as simple as it can be because the UI will not be coupled to the data in any way.

4.5.2 User Interface

The user interface is a crucial part of the design of the web application. The interface is the sole interaction between the user and the system and therefore must be simple and intuitive. Figures 49-52 show an overview of the design of the web application.

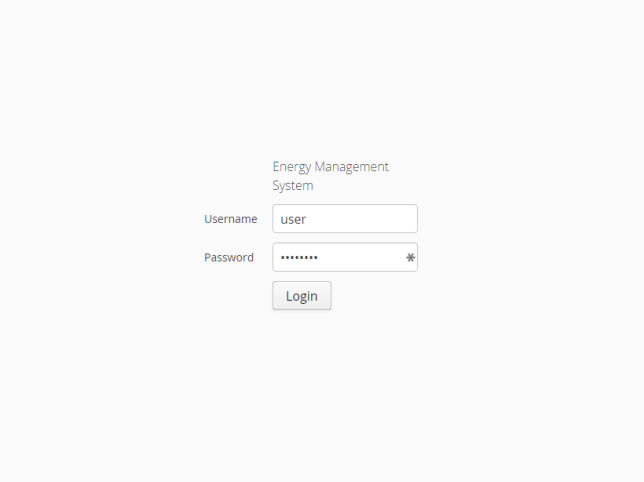


Figure 49. Login Page

Figure 49 shows the login page for the web application. This is a very simple page that allows the user to log into the web application. After entering the correct username and password, the home tab of the web application will load. If the user enters an incorrect username and password, a message will appear on the screen that tells them the entry was invalid.

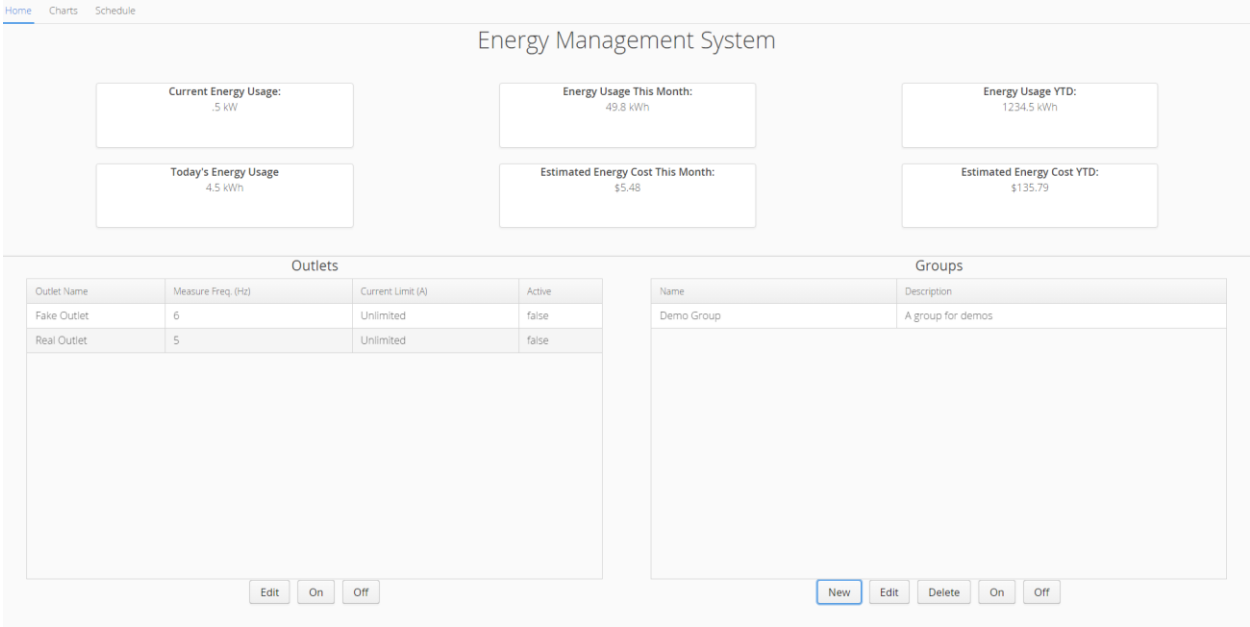


Figure 50. Home Tab

Figure 50 shows the home tab of the application. The user sees this screen after they successfully log in. The home tab shows most of the information about the system. On the top half of the screen, the user can see some basic statistics about their current system. These measurements will always be the same metrics and are intended to give the user a quick idea of their daily, monthly, and year-to-date usage. The bottom half of the screen shows two tables where the user can configure both the outlets and groups in the system. The outlet table (on left) allows the user to configure outlet settings, such as name, refresh rate, and current limit. The user can also toggle the on/off state of the outlet from here. The group table (on right) allows the users to create, edit, and delete groups. From here, outlets can be added or taken away from groups. In addition, the user can toggle the on/off state of all outlets within a group at once.

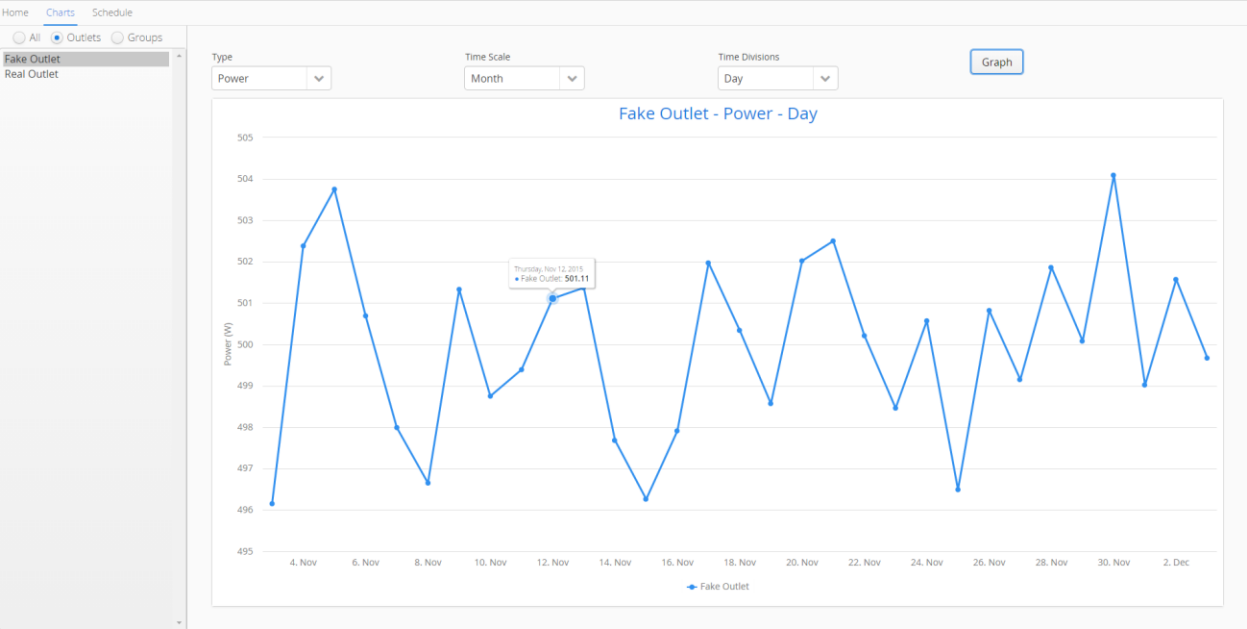


Figure 51. Chart Tab

Figure 51 shows the Chart Tab of the web application. The chart tab is where the user can graph all of their usage data from each of their outlets. The panel on the left is where the user can select whether they want to graph by outlet, group, or simply all outlets. This panel is then used to select the outlets or groups that the user wants to see data for. The three drop-down menus can then be used to select what type of the graph the user desires (voltage, current, or power), the time scale (ranges from 5 minutes to year), and the time divisions (varies based on time scale). Once the user selects all these components, the user can click the 'graph' button to create the desired graph. The outlet selection panel supports multiple selection. If multiple outlets (or groups) are selected each one will be plotted as a separate line on the graph.

The charts are built using a combination of MySQL queries and Java code to format the data into the particular format that the chart library requires. All the measurements from each of the outlets is queried from the database. Then, based on the time divisions, the data are averaged together for

each division and a single point is made on the graph for each point. If there is only one measurement in the database for a particular division, the chart will only reflect that measurement.

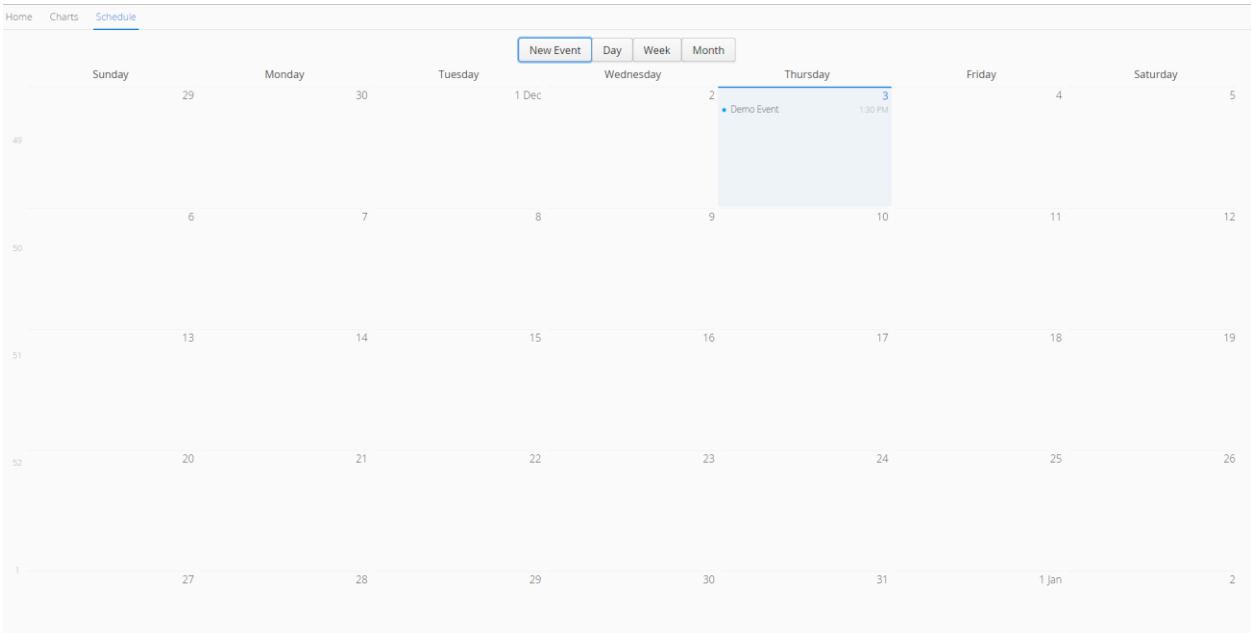


Figure 52. Schedule Tab

The final tab (shown in Figure 52) is the schedule tab. This is the place where the user can create a schedule for their outlets. The schedule interface was made to have the basic look and feel of other calendar interfaces, such as Google Calendar. The user can create events that have a specific start date and time, an end date and time, a list of outlets that are involved, and whether to keep these outlets on or off. Every minute a Java routine runs in the background to update all of the outlets currently associated with an active event.

4.5.3 Communication with Outlets

The web application needed a way to communicate with the outlets. This communication needs to occur when a user toggles an outlet (or group) on or off and when the user changes the current limit or the measurement frequency. From the web application, the communication is straightforward. The web application simply calls a python script that handles sending the command to the outlet over PLC. There is a different python script for each of the commands the web application may need to send. One of the arguments of each of the scripts is the PLC address that is stored in the database. This instructs the Python script where to send the command over the PLC.

4.6 DATA STORAGE

4.6.1 Database Model

The MySQL database management system stores the various components of the system in separate tables. Figure 53, below, shows the overall components of the database. The Users table holds any relevant usernames that are used with the system.

The Outlet table contains information data for all of the remote outlet modules, which are the major components of the Energy Management System. The outlet ID is primarily used for querying the outlets, and will remain internal to the database and web application. The user identifies the outlets by name, which can be customized. The outlet module's address is stored as a 64-bit binary value, and is used to communicate with the remote outlet module. The frequency and current limit columns are for the update frequency and current limit, respectively. The active column stores whether or not the outlet module is active.

The Measurement table holds all of the outlet module measurement readings that are sent to the main unit, from the individual outlet modules. The measurement ID is an internal primary key for the table, and is used to identify the reading within the database. The table stores the outlet ID, voltage reading, current reading, and power reading from the associated outlet module. A timestamp is inserted at the time the reading is created, which allows the user to view a range of readings through the web application.

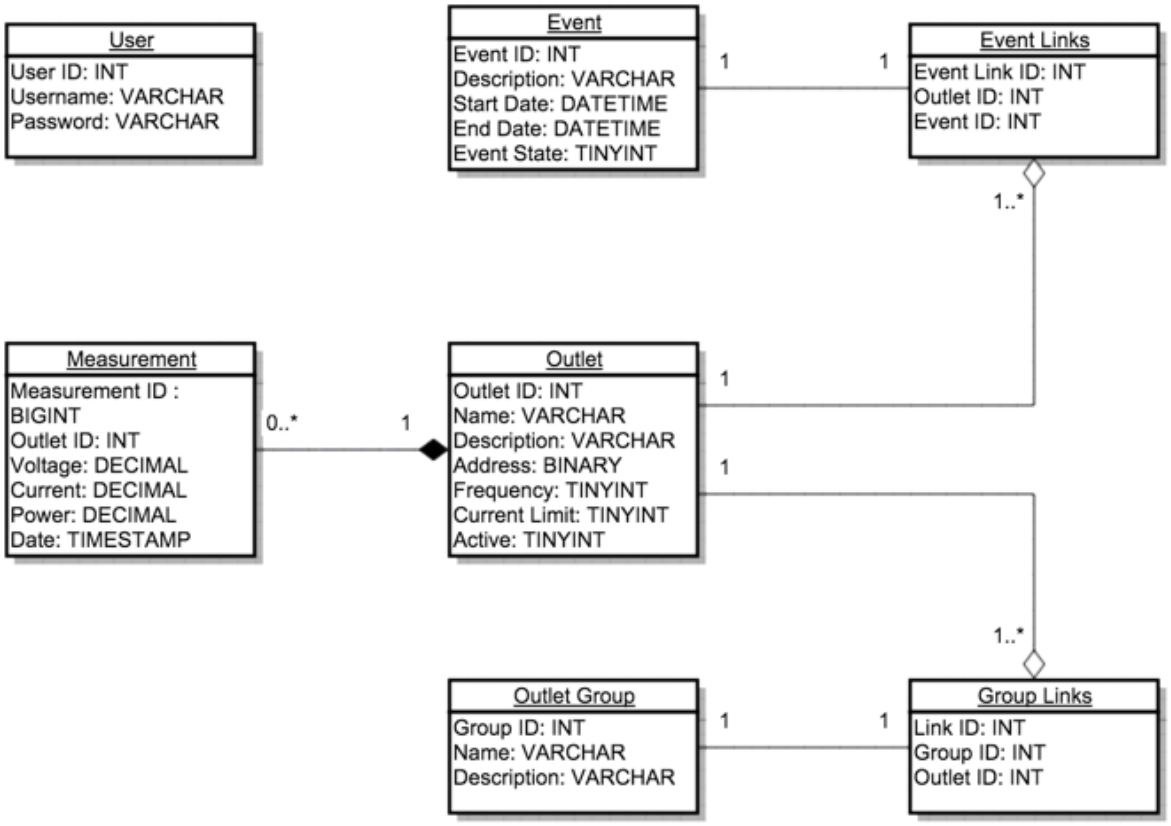


Figure 53. Database UML Diagram

The Event table holds any user-defined schedules for individual outlet modules. The event ID column is an internal ID for the table, as well as an identifier for the Event Links table. The start and end date columns are user-defined for the schedule created. The event state column determines whether or not the outlet should be on or off.

The remaining two tables, Group Links and Event Links, are used to correlate any outlet modules with its respective group or event. The tables are internal to the application, and are not seen by the user.

4.6.2 Data Compression

It is unlikely that users will need to see the 15-second resolution of outlet readings after a period of time. Because of this, the data is “compressed," by averaging a certain number of readings into one. To accomplish this, every day at midnight, the main unit queries all of the readings that are 1 to 2 days old, and then averages all readings for each hour into one hour measurements, for all outlets. The voltage, current, and power are averaged and stored into a new row. The other rows associated with the averaging are then deleted.

4.7 ENGINEERING STANDARDS

There are many engineering standards associated with the design of the EMS project. First and foremost, the system interfaces with the 120 V_{RMS}, 60-Hz AC power line to provide the main functionality of the system. The I^2C standard was utilized to interface between the controllers and the power line communication chips. The production modules must meet the form factor of a standard household electrical outlet box. For the FPGA, Quartus II was used for development. NetBeans was used for development of the Raspberry Pi 2 web application, which was deployed on Apache Tomcat. The SQL standard was used for database development.

4.8 MULTIDISCIPLINARY ASPECTS

This project involves aspects pertaining to computer, electrical, mechanical, and software engineering. Table 15 provides a brief description of the tasks involved for the various disciplines.

Table 15. Multi-Disciplinary Aspects

Multi-Disciplinary Aspects	Relevance to Project
Computer Engineering	Interface between hardware components and processor. Development of firmware to drive device hardware.
Electrical Engineering	Circuit design, PCB layout
Mechanical Engineering	Design of enclosure for various modules
Software Engineering	Development of a web-app to display data and remotely configure outlets

4.9 BACKGROUND

Completion of the Energy Management System required the utilization of a multitude of skills. Some of the most important skills associated with the project included hardware and software interfacing, circuit design, web application design, database construction, communication, and signal integrity analysis. Core computer and electrical engineering classes taken by group members, such as Software Engineering, Interface and Digital Electronics, Circuits I and II, Electronics I and II, Linear Systems, Communications Systems, and Data Communication provided the necessary background in these skills. Outside of these classes, personal experience in Wireless Networks has been extremely valuable for communication design.

Donald MacIntyre has had experience with PCB design, layout, signal integrity, VHDL firmware design and high voltage power design from multiple co-op blocks at Moog Inc. Andrew Cope has had experience with database construction in personal projects, as well as for professional websites. Jacob Lauzon has had considerable experience designing Java web applications through The Echo Group.

4.10 OUTSIDE CONTRIBUTORS

Dr. Andres Kwasinski offered direction and advice in regards to the utilization of power line communication, and will act as a primary contact with communication concerns.

Dr. Becker-Gomez also helped the team in obtaining PLC evaluation boards from Cypress.

5 CONSTRAINTS AND CONSIDERATIONS

5.1 EXTENSIBILITY

The current focus of the project is for residential buildings and possibly small businesses; however, the design could be extended to large businesses and large buildings. This would only include an addition of outlet modules and, depending on the size of the install, possibly higher performance PLC chips. The main concern with larger systems would be the fact that large buildings use three-phase power directly. Some adaptations would need to be made to measure the three different phases. In addition to larger systems, smaller systems could also be created. For instance, single, network connected outlet modules that can be purchased separately.

5.2 MANUFACTURABILITY

The system will be scalable and ultimately mass-producible. Both the outlet modules and the main unit will be assembled on a Printed Circuit Board (PCB) that can be easily mass-produced. As the component parts will be bulk-ordered, the overall cost of the system per unit will be reduced.

5.3 RELIABILITY

The system will need to be very reliable, as it will need to be powered on and measuring data 24/7. The system will also need to be able to recover from a power outage without human interaction. The design allows for a reliable system because the user will not have to manually restart the system components.

Before attempting to mass-produce the Energy Management System, Highly Accelerated Life Testing (HALT) will be performed to attempt to quantify the Mean Time Between Failure (MTBF) of the Energy Management System. Tools such as Sherlock, which is a software tool providing automated design analysis, could be used to model failure rates and determine the complete product life curve. Based on the results of Sherlock's Automated Design Analysis tools, MTBF issues can be addressed early in the design cycle. Due to the high cost of the Sherlock software, it is not feasible to perform this analysis as part of this project. An electrical stress analysis can be performed using standard circuit analysis techniques to verify that components have sufficient deratings.

5.4 HEALTH AND SAFETY ISSUES

The system will need to have surge protection, to prevent any connected devices or outlet modules from being damaged. The system components will also need to be Underwriters Laboratory (UL) recognized, to ensure that potential risks are limited and safety standards are met. In order to commercially sell the Energy Management System, it will be necessary in the United States to obtain approval from UL and other safety agencies in foreign countries which could be expensive. UL recognized components were chosen for all components no isolated from the power line.

5.5 INTELLECTUAL PROPERTY

The system's web application software will be proprietary.

With the smart grid industry on the rise there are many provided resources such as example code and application notes. For example, companies such as Texas Instruments, in an effort to encourage design engineers to choose their products, make available at no cost application notes and sample code. Therefore, the programming effort for this design will most likely heavily leverage available code. Also, there are many open source projects that have been developed in the past, which can be referenced. Additionally, energy-metering algorithms are provided by multiple vendors. These public domain algorithms will serve as a basis for the embedded development.

5.6 ENVIRONMENTAL

The EMS will monitor and control outlet power consumption, allowing users to reduce their power consumption. Lowering power consumption is an integral part of sustainability. Similarly, the outlet modules and main module will be designed such that they consume minimal amounts of power. It is important the system does not utilize more power than it can save the user. While the project would still be useful for automation, low power consumption is required for high efficiency.

Saving power is a significant feature, since society's heavy reliance on fossil fuels increasingly makes global warming a concern. Unsustainable power consumption must be curbed to halt global warming.

5.7 SUSTAINABILITY

Minimizing power consumption promotes energy conservation which results in environmental sustainability. The EMS provides a green technology via its monitoring and control capabilities intended to provide a tool for consumers to consume power as efficiently as possible. To the maximum extent possible the EMS hardware will be designed and fabricated with environmentally friendly materials, such as lead free solders. The ability to programmatically schedule turning off loads automatically ensures power minimization.

6 COST

Table 16 and 17 show the cost estimates of each part of the outlet modules and main unit respectively. Part selection was limited to components that were in stock at DigiKey a well-known national electronics distributor. Table 16 and 17 also provide hyperlinks to component datasheets by selecting the part number. The final column in the tables indicate in what functional block of the design the particular component is used. The cost per unit listed is the low quantity DigiKey cost. It is also anticipated that a printed circuit board will be designed and fabricated using an online prototype shop such as Sunstone. The cost for fabricating a couple of blank PCBs is estimated to be $250. A full cost estimate is shown in Table 18 for 3 outlet modules and 1 main unit. The costs specified in this report are representative of the cost of a prototype system. If the EMS system was taken to production, the system would be mass produced which would allow for parts to be purchased in bulk at discounted prices. In the prototype system, multiple expensive development boards were used to decrease design time. In production a single fully featured PCB containing only the necessary components would be implemented. In production all of the PLC intelligence would be moved into the FPGA, eliminating the expensive PLC module cost. In production the team would also consider moving from an isolated electrical design to an electrically coupled design which would eliminate the need for expensive components capable of providing isolation. It is estimated that in production remote outlet units could be produced at a unit cost of $45. This estimate induces the cost for all parts, fabrication of a PCB, and also the cost of assembly and testing of the final project.

Table 16. Outlet Module Cost

Part Number	Description	Vendor	Cost per Unit	Qty	Ext Cost	Lead Time	Functional Block
RAC01-05SC	AC/DC switching power supply	Recom	$ 12.34	1	$ 12.34	stock	Power Supply
V150ZA05P	Varistor	Littelfuse	$ 0.56	1	$ 0.56	stock	
MOC3063M	Optoisolator	Fairchild Semi	$ 0.95	1	$ 0.95	stock	Load Switch
MMBT3904	NPN Transistor	Fairchild Semi	$ 0.15	1	$ 0.15	stock	
BTA20-600CWRG	TRIAC	STMicroelectronics	$ 1.97	1	$ 1.97	stock	
ACS722	Hall Effect Current IC	Allegro	$ 5.27	1	$ 5.27	stock	Current Sense
ACPL-C87A	Isolated Voltage Sense	Avago	$ 6.42	1	$ 6.42	stock	Voltage Sense
TLC272A	dual op-amp	TI	$ 1.35	1	$ 1.35	stock	
MMBT3904	NPN Transistor	Fairchild Semi	$ 0.15	1	$ 0.15	stock	
BZX84C5V6	5.6 Zener Diode	Fairchild Semi	$ 0.19	1	$ 0.19	stock	
MRA4006	1A, 800V diode	On semi	$ 0.31	2	$ 0.62	stock	
EP4CE6E22C8N	Field Programmable Gate Array	Altera	$ 11.95	1	$ 11.95	stock	Controller
Cost					$ 41.92		

Table 17. Main Unit Cost

Part Number	Description	Vendor	Cost per Unit	Qty	Ext Cost	Lead Time	Functional Block
CY8CPLC10	PLC Chip	Cypress	$ 9.04	1	$ 9.04	stock	Power Line Communication
Pi 2	Raspberry Pi 2	Amazon	$ 35.00	1	$ 35.00	stock	Main Unit
SDSDQUAN-032G-G4A	32 GB MicroSD Card	Amazon	$ 16.19	1	$ 16.19	stock	Main Unit
EW-7811Un	USB Wireless Adapter	Amazon	$ 9.23	1	$ 9.23	stock	Main Unit
Cost					$ 69.46		

Table 18. Complete Cost of Selected Number of Modules

Module Type	Number of Modules	Cumulative Cost of Module Type
Main Module	1	$69.46
Outlet Module	3	$125.76
Full Cost		$195.22

7 TESTING

7.1 TESTING SCHEDULE

The initial testing schedule is provided in Table 19. Minor adjustments to the schedule were made throughout the project. Unit testing were done first, to ensure that individual components of the Energy Management System are working correctly. The integration testing followed the unit testing, and was responsible for ensuring that the components worked together with one another. Finally, acceptance testing was performed to ensure the system as a whole was working correctly to meet the engineering and marketing requirements. Final testing was completed the first week in December of 2015.

Table 19. Preliminary Testing Schedule

Unit Testing	June 2015
Integration Testing	September - October 2015
Acceptance Testing	October - November 2015

7.2 UNIT TESTS

Unit tests verify that individual components are operating as expected. Unit tests are critical to properly debugging a project, as they significantly reduce the scope of variables to be tested. Unit tests validate individual components, ensuring that higher level tests will not fail due to unexpected operation of the subcomponents. The complete unit tests for this project are shown in section 12.1 of Appendix B.

7.3 INTEGRATION TESTS

Once the Unit tests have been passed, it is critical that the boundary between the subsystems are thoroughly tested. This boundary is known as the interface between components, and is the primary location for errors when endeavoring to utilize integration tests. In addition, it is only upon integration that some components can be tested, as they lack a usable interface for reasonable tests. Thus the complete Integration tests for the EMS is shown in section 12.2 of Appendix B.

7.4 ACCEPTANCE TESTS

Acceptance tests are the tests conducted to verify that the requirements of a project have been met. Acceptance tests validate the product, and verify that it works as expected upon completion. As such, the acceptance tests of the EMS are closely coupled to the engineering requirements. Passing all acceptance tests will guarantee that all marketing and engineering requirements have been satisfied. In order to release a finished product fulfilling the engineering specifications, the project must pass the following tests. The complete acceptance tests for the EMS are shown in section 12.3 of Appendix B.

7.5 TEST COVERAGE MATRIX

The test coverage matrix verifies that all engineering requirements are fully tested. The requirement number corresponds to requirements listed in section 3, whereas the test number corresponds to the tests listed in Appendix B. The test coverage matrix is shown in section 12.4 of Appendix B.

7.6 TEST RESULTS

Section 12, Appendix B covers the basic test results for each of the tests as they were completed. When testing, there were a number of notable results obtained. The EMS project met all of its accuracy goals: 4% error in power at 55W loads, 1% error in voltage for a 29W load, and error from 9.5% at 29W to 0% at 55W for the current. The reason current ranged so much was because there is a small current at such a small load, which is difficult to measure, however larger loads were measured more accurately. In addition, the power efficiency was calculated to be 96.4% efficient at a load of 77.4W, which will only increase with the load. The control electronics were seen to draw approximately 2W which was fixed independent of the load. Beyond performance metrics, the manual entry of outlets was abandoned, in favor of outlets automatically being added to the database and web application, which is a far more reliable, pleasant user experience.

The project success also came with minor shortcomings. The project did not implement a number of features in the web application: default charts on outlet selection, scheduling recurrent events, settings, and real time measurements. Many of these features were abandoned due to time constraints or performance concerns, but others, such as the real time measurements merely evolved into different features. In that case, while real time was abandoned, the same 1 second transmission interval is attainable by the user, now in addition to a range of transmission rates from once per second to once every 15 seconds, which is ultimately a feature gain.

There were a number of requirements that were not fully verified, although they are expected to pass in a production environment. The prototype hardware tests have revealed that high current loads should not be run for extended times on the outlet module. In the prototype system the current sense circuitry was dissipating too much power for high load currents. This was due to the small leads used to connect the current sensor in the breadboarded setup of the project which did not allow for proper heat sinking. In the production design the current IC would be connected directly to power planes (as specified by current IC datasheet) which would allow for the conduction of heat away from the IC. The outlet and main modules were not produced for less than $50 and $200 respectively. However these cost estimates were evaluated at a single run pricing and evaluation boards used often had extra hardware that was not needed. It is estimated that the outlet and main modules would meet the cost goal in a production environment. For more information on this, see the cost section of this document. Likewise, the completed outlet module prototype would not fit within a standard electrical box or be easy for an electrician to install. However production units will consist of only a single PCB which will make use of all surface mount parts. This will allow for a drastic size reduction as the current implementation

uses many different evaluation boards and uses through hole parts exclusively. Assembly size estimates for a production unit would be 2.5in. wide by 4in. tall by 0.5 in deep, which would fit in a standard electrical outlet.

8 RISKS

8.1 SYSTEM ELECTRONICS

8.1.1 Power Supply

At this time the load on the power supply is not completely known but expected to be around 2 Watts for an optimized design.

8.1.2 Controller

The remaining uncertainties for the controller are the requirements of the power line communication interface, which will be required. Uncertainties include number of I/O needed, communication protocols with PLC chip, data transmission speeds, power calculations needed, and the sampling rate. These factors will be strongly impacted by the web UI design and which parameters are chosen to be tracked.

8.2 WEB APPLICATION

There are few major uncertainties with this design. The first, and biggest, uncertainty is whether or not the Raspberry Pi 2 will be able to handle serving the web application and the database. The Django framework was chosen to reduce memory usage; however the usage is definitely not small. The application's usage along with the Linux distribution and hosting the database may be too much for the Pi. More extensive testing may need to be done to ensure that the memory usage will not be an issue. In addition to the memory usage, the processing power is a concern. There is some uncertainty as to whether the processor on the Pi will be able to handle all of the requests from the database, the hardware, and the application. If there is too much going on, the performance of the system could be affected.

8.3 DATA STORAGE

8.3.1 Disk Space

Although MySQL puts some overhead data in the database, it is miniscule against the amount of data needed for the outlet modules and outlet readings. Similarly, the User, Outlet Group, Event, Group Links, and Event Links tables take up a small amount of disk space. There are two major considerations, when it comes to disk space: the Outlet and Measurement tables. Table 20 below shows the estimated size for different numbers of outlet modules.

Table 20. Outlet Table Size for Various Quantities of Outlet Modules

Number of Outlet Modules	Maximum Size for Outlet Module Table row:	Total Estimated Size
1	1,068 B	1,068 B
10	1,068 B	10.43 KB
50	1,068 B	52.15 KB
100	1,068 B	104.29 KB
300	1,068 B	312.89 KB
1,000	1,068 B	1.018 MB
10,000	1,068 B	10.19 MB

As seen in the table above, the size for even a large number (10,000) of outlet modules results in a relatively small table size. However, the larger consideration is the Outlet Reading table. Table 21 below shows several quantities of outlet modules, as well as two different updating frequencies.

Table 21. Measurement Table Size for Multiple Outlet Modules

Number of Outlet Modules	Update Interval	Max Bytes Per Reading	Table Size Per Day	Table Size Per Year	Table Size Per 5 Years
10	1s	29 Bytes	23.89 MB	8.515 GB	42.56 GB
50	1s	29 Bytes	119.48 MB	42.59 GB	212.9 GB
100	1s	29 Bytes	238.95 MB	85.17 GB	425.8 GB
500	1s	29 Bytes	1,195 MB	425.9 GB	2.079 TB
10	15s	29 Bytes	163.13 KB	58.14 MB	290.7 MB
50	15s	29 Bytes	815.63 KB	290.7 MB	1.419 GB
100	15s	29 Bytes	1.59 MB	580.4 MB	2.834 GB
500	15s	29 Bytes	7.96 MB	2.837 GB	14.19 GB

Given enough outlet modules, there is a considerable amount of space that needs to be used in order to store the outlet module readings. The table size assumes that no readings are deleted over the lifetime of the product. If the data were not compressed, 11 GB of available storage on the main unit would be able to last a maximum of roughly 19.4 years (with 100 outlets in a home).

8.3.2 Data Types / Values

Since the Outlet Reading table uses the TIMESTAMP data type, the time is represented in 32 bits. The TIMESTAMP data type represents the number of seconds since 1970. As it is a 32-bit integer, it has a maximum value of 4,294,967,296. This results in the TIMESTAMP maxing out in the year 2038. If the system were to be used past that date, it would be advisable to switch to the DATETIME data type, which is 64 bits long. This would allow for ease of use, at the cost of adding 4 more bytes to the reading row. This is a 13.7% size increase, but should be mitigated by the data compression.

9 SCHEDULE

Table 22. Project Schedule

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Critical Component Breakout Boards	8/24/2015	RM, DM	9/28/2015	COMPLETE: Critical component breakout boards have been completed for all functions. Messages have successfully been sent through the power line using the provided evaluation boards.
User Interface Implementation	8/24/2015	JL, AC	11/28/2015	COMPLETE: Web application has been completed and has been successfully been loaded onto the Raspberry Pi.
Web App Database Communication	8/24/2015	AC, JL	9/13/2015	COMPLETE: The web application is able to communicate with the database using Hibernate (An Object-Relational Mapping library for Java)
Order Parts	8/24/2015	All	9/20/2015	COMPLETE: Cypress has provided a new PLC evaluation kit which functions correctly.
Initial PCB Design	8/31/2015	DM	9/6/2015	COMPLETE: Focusing efforts on vero-boarding initial hardware design instead of PCB design. Breadboard has been constructed. PCB may still be constructed if time permits, but

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
				based on summer slippage time for spinning PCB my not be available. Completion of breadboard has met the intent of this task.
Obtain and Verify Parts	9/7/2015	All	9/20/2015	COMPLETE: All parts except PLC have been received and verified. Completion date has been pushed back as received evaluation PLC boards are not functioning properly.
Verification of Power Supply Circuitry	9/14/2015	DM	9/14/2015	COMPLETE: Power Supply circuitry has been verified.
Verification of Breadboard Load Switch	9/14/2015	DM	9/14/2015	COMPLETE: Load Switch is operational, and a load is able to be switched ON and OFF via an external voltage (provided from FPGA or other embedded system).
Verification of Breadboard Current Sense	9/21/2015	DM	9/21/2015	COMPLETE: Current sense circuitry is operational.
Verification of Breadboard Voltage Sense	9/21/2015	DM	9/21/2015	COMPLETE: Voltage sense circuitry is operational

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Outlet Communication with PLC	9/28/2015	RM	9/25/2015	COMPLETE: Messages have been successfully sent via the power line.
Interface PLC with Pi	9/28/2015	RM, JL	10/7/2015	COMPLETE: Team has decided to acquire PLC evaluation boards. PLC communication is occurring with the PI but communications does not work consistently. Communication has improved from last status report, and various issues have been discovered and solved. Team successfully sent messages from Pi to FPGA.
Verification of Breadboard Processor	10/5/2015	All	10/9/2015	COMPLETE: FPGA has been selected to perform necessary embedded processing. Necessary power calculation is working properly within Modelsim simulation using a bus functional model of the ADC. FPGA I2C interface necessary for PLC communication has also been simulated. Team is working on determining final communication protocol between FPGA and Pi. All VHDL has been synthesized successfully. Messages have successfully been sent from FPGA to PLC to Pi (Both ways

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
				have been tested and are working)
Final PCB Design	10/19/2015	All	10/18/2015	COMPLETE: Based on team progress to this point, the decision has been made not to have a PCB manufactured. Completion of veroboard has met the intent of this task and shall be used for verifying functionality of the project.
Finalized Database Structure	10/19/2015	AC, JL	11/28/2015	COMPLETE: Finalized database structure is a result of completion of the web application.
PI PLC API	10/26/2015	RM, AC, JL	10/26/2015	COMPLETE – A python module has been written to act as the API for the Pi communication with the PLC chip. Additionally several python scripts have been written to handle commands to be sent from the Pi to the remote outlet modules.
System recognizes new outlets automatically	11/2/2015	All	11/12/2015	COMPLETE – The Pi's I2C will rarely read incorrect bits for the outlet module's address (e.g. 1000 instead of 1010). This results in a new, different address being stored in the

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
				database. However, it happens about 1% of the time, so the incorrect outlets (which would have much less readings than the correct outlets) could be deleted from the database. Another option is to read the address twice from I2C and compare the two values. If they are unequal, then the measurement may not be stored. Other solutions are being considered.
Send Hardware Measurement over PLC	11/9/2015	RM, JL, DM	11/15/2015	COMPLETE – Hardware Measurements have been sent over PLC. Team is working on tweaking accuracy of measurements.
Receive and store measured data	11/9/2015	AC, JL, RM	11/9/2015	COMPLETE – Measured data has been received and can be stored in the database.
View measured data	11/9/2015	JL, AC	11/9/2015	COMPLETE – Team currently has downloaded current version of web application onto the Raspberry Pi and has demonstrated capability to view data on web application.

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Toggle state of single outlet from web interface	11/16/2015	All	11/28/2015	COMPLETE – Load is able to be switched ON and OFF by toggling of the web application.
Toggle state of a group of outlets	11/16/2015	All	11/28/2015	COMPLETE – This task is seen to work. Multiple outlets can be added to a group and toggled ON and OFF.
Outlets and groups follow schedule	11/16/2015	All	11/28/2015	COMPLETE – Events are able to be scheduled from within the web application. These events then effect the status of the remote outlet module.
Data Compression Verification	11/16/2015	AC	11/16/2015	COMPLETE – Compression script runs every night at midnight, taking the measurements from two days ago, and compressing them into averaged hour measurements.
Full system test passed	11/25/2015	All		COMPLETE – All tests defined in the test plan have been run.

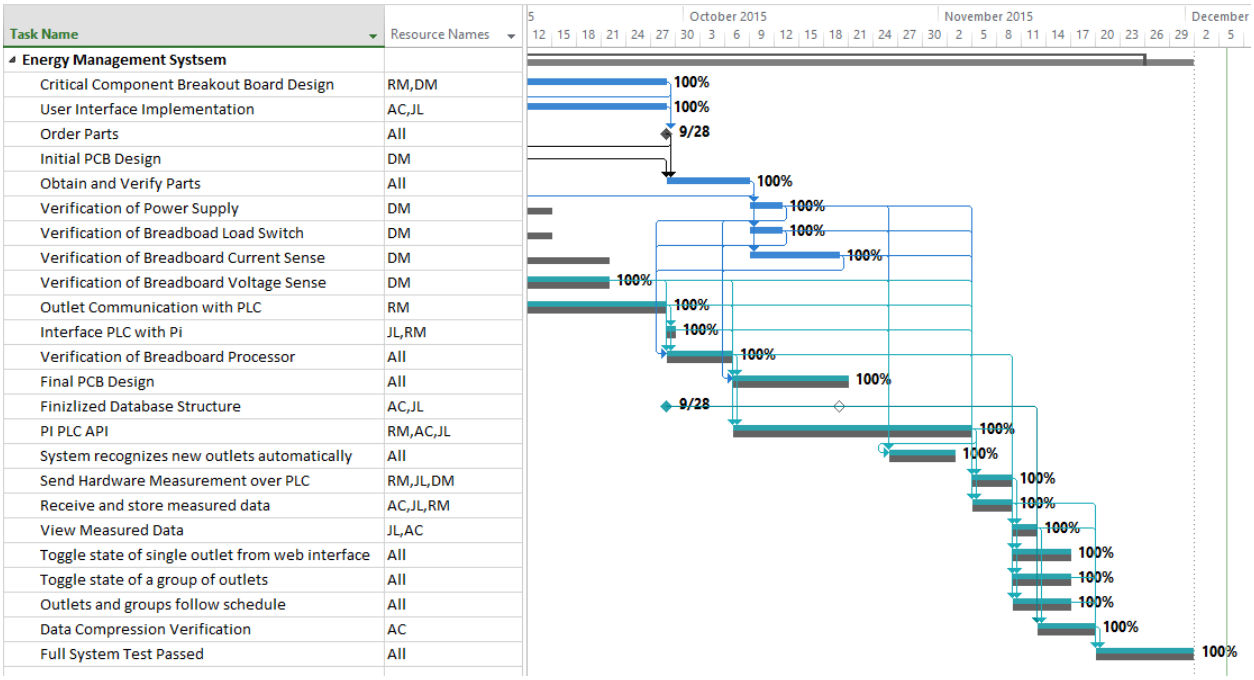


Figure 54 - EMS Gantt Chart

10 PERSPECTIVE

10.1 DIFFICULTIES

There were many difficulties encountered during the development of this project. The biggest of which was having all separate components that were much larger than we anticipated. This prevented us from being able to design a PCB and create a design that fit into a standard outlet box. Another difficulty was working with the PLC modules that were provided to us. The documentation did not adequately reflect the capability of the system-on-chip (SoC) on the PLC. Initially, the SoC was going to be used to do more than just PLC communication; however, the processor was not powerful enough to handle much beyond the PLC communication. This caused us to have to find another computing device for the outlet module and implement I2C communication between our two systems. Further limitations of the PLC modules hindered reliability of the system.

The decision to not develop a PCB for the remote outlet hardware prevented high load testing from occurring until very late in the project. This is because while individual components were set to meet the necessary design requirements but the nature of the breadboarded setup provided limitations which would have not been present if a PCB design had been performed

10.2 RETROSPECTIVE

Considering the initial design of the Energy Management System, we feel that the outcome of the project met our initial design goals fairly well with some exceptions. The size and cost of the modules were both greater than we had initially planned; however, this was due to our system being more of a proof-of-concept prototype and we believe that in a production model the size and cost requirements could be met. In addition, the outlet module included an FPGA, which was different from the initially planned microcontroller. Also, the web application was written in Java rather Python, as we had initially planned. This, however, did not hurt our final design and we believe it was a good design choice to make.

10.3 FUTURE

If we were to continue work on the Energy Management System there are few things we would focus on. We would want to implement our own PLC network stack and communication protocol in the FPGA. This would allow us to have a lot more control over the hardware and hopefully implement a more powerful and reliable system. In addition, we would be able to reduce the hardware needed to reduce the size of our module and design a PCB. We would also move the MySQL database and the hosting of the web application to a central server. This would reduce the load on the Raspberry Pi significantly and increase reliability. The central server would also provide a way to maintain and manage the web application, push updates to all users, and increase security of the application.

11 APPENDIX A

11.1 COMPETITIVE PRODUCTS

Lutron - http://www.lutron.com/en-US/Residential-Commercial-Solutions/Pages/Residential-Solutions/ResidentialEnergySavings.aspx
P3 Kill-a-watt - http://www.p3international.com/brochures/p4400.pdf
REC Green Energy Solutions - http://rec-gt.com/en/solutions/detail/7/
Belkin WeMo - http://www.belkin.com/us/Products/home-automation/c/wemo-home-automation/
Insteon - http://www.insteon.com/

11.2 SYSTEM ELECTRONICS

Fundamentals of AC Power Measurements
Energy Meter Code Library for 1-Phase to 3-Phase Using MPS430 Family
Current Sensing In Metering Applications Using A Pulse Current Sensor
Isolation Amplifier for Voltage Sensing in Electric and Hybrid Vehicles
STPM01 Programmable Single Phase Energy Metering IC with Tamper Detection
OnSemi Transient Overvoltage Protection Guide
STPM Smart Metering ICs Overview
STPM01 Energy Metering IC External Circuits Application Note
A Low Cost Single Phase Electricity Meter Using the MSP430C11x
Texas Instruments Smart Grid & Energy Products Overview
PLC Motherboard with AC Mains Line Coupling Reference Board
Three Outlet Smart Power Strip Reference Design
Low Cost Two Phase Electric Meter
Single Phase Electric Meter with Isolated Energy Measurement
MSP430 Energy Library
TI Electric Metering Overview (Including Reference Designs)
EVM430-F6779 Evaluation Module
AN954 Transformerless Power Supplies: Resistive and Capacitive
RECOM Power Supply Application Notes 2015

11.3 POWER LINE COMMUNICATION

Datasheets

http://www.cypress.com/?docID=45757
http://www.cypress.com/?docID=50840
http://www.st.com/web/en/resource/technical/document/datasheet/CD00096923.pdf
http://www.st.com/web/en/resource/technical/document/datasheet/CD00274120.pdf
http://www.st.com/st-web-ui/static/active/en/resource/technical/document/datasheet/CD00294970.pdf
http://www.atmel.com/Images/doc43051H.pdf
http://www.nxp.com/documents/data_sheet/TDA5051A.pdf

Application Notes
http://www.cypress.com/?docID=46702
http://www.st.com/web/en/resource/technical/document/application_note/CD00143379.pdf
http://www.st.com/web/en/resource/technical/document/application_note/CD00271738.pdf
http://www.st.com/st-web-ui/static/active/jp/resource/technical/document/application_note/DM00037363.pdf
A Low Cost Home Automation System Base On Power Line Communication Links
Smart Street Lighting Remote Control Protocol over Power Line Communication

11.4 WEB APPLICATION

BeagleBone Black
Product Page - http://beagleboard.org/BLACK
Processor Data Sheet - http://www.ti.com/lit/ds/symlink/am3358.pdf
Adafruit Page - http://www.adafruit.com/product/1876

Raspberry Pi 2 Model B
Product Page - http://www.raspberrypi.org/products/raspberry-pi-2-model-b/
Datasheet - http://www.adafruit.com/pdfs/raspberrypi2modelb.pdf

Django
Homepage - https://www.djangoproject.com/
Install Guide - https://docs.djangoproject.com/en/1.8/intro/install/
Django on Pi - http://www.hackedexistence.com/project/raspi/django-on-raspberry-pi.html
Django on Pi - http://www.hackedexistence.com/project/raspi/django-on-raspberry-pi.html

Apache Web Server
Homepage - http://httpd.apache.org/
Apache on Pi - http://www.raspberrypi.org/documentation/remote-access/web-server/apache.md

11.5 DATA STORAGE

MySQL
Documentation - http://dev.mysql.com/doc/refman/5.6/en/index.html
Storage Engines - http://dev.mysql.com/doc/refman/5.1/en/storage-engines.html
Data Storage Requirements - http://dev.mysql.com/doc/refman/5.1/en/storage-requirements.html

12 APPENDIX B

12.1 UNIT TESTS

Test Name:	Electrical - Power Supply DC Output Voltage – Test 1			
Setup:	Apply 120 VAC to terminals 1 and 2 of Recom power supply module			
Steps	Action	Expected Results	Passed	Comments
1	Measure the output voltage at pin 3 with respect to pin 4	DC voltage of 3.3V is measured +/- 5%	✓	3.3V Measured
2	Apply load resistors ranging from 1k to 4.8k across pins 3 and 4	Verify DC voltage of 3.3V is measured +/- 5%	✓	Added 1 mF capacitor to minimize ripple

Test Name:	Electrical - Voltage Sense Output Voltage – Test 2			
Setup:	Apply voltage of 0V to the input of the voltage sense circuitry			
Steps	Action	Expected Results	Passed	Comments
1	Measure the output voltage	The measured output voltage should correspond to the scale factor * input +/- 10%	✓	
2	Increase input voltage by steps of 5V until 170V (120V RMS) is achieved and repeat step 1	The measured output voltage should correspond to the scale factor * input +/- 10%	✓	Average error of 2.08% at 120V AC

Test Name:	Electrical - Voltage Sense Output Voltage Frequency Response – Test 3			
Setup:	Set a function generator to a sinusoidal signal of a fixed amplitude at a frequency of 10 Hz			
Steps	Action	Expected Results	Passed	Comments
1	Measure the output amplitude Voltage	Results should match DC test.	✓	
2	Repeat step 1 at frequencies of 100, 200, 500, 1000 Hz	As frequency increases the output amplitude will decrease with frequency	✓	
3	Plot the output voltage amplitude vs frequency		✓	
4	Verify that output frequency response is acceptable for application	3dB bandwidth of at least 1000 Hz	✓	Spectrum analyzer obtained passband gain of -42 dB with cutoff frequency of roughly 1Hz, which is well above 60 Hz operational limit

Test Name:	Electrical - Voltage Sense Circuit Power Supply Draw – Test 4			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Apply varying amounts of current ranging between -20A and 20A		✓	
2	Measure the output voltage for each current input	Output voltage corresponding to current input	✓	Average error of 3.44% at 120Ω load

Test Name:	Electrical - Load Switch - Switching Control – Test 5			
Setup:	Connect a power rheostat between the high side TRIAC output and the ac neutral. Connect an ammeter in series with the load.			
Steps	Action	Expected Results	Passed	Comments
1	Set the TRIAC to the OFF position	Verify no current flow through the load	✓	Current flow stops at next zero crossing
2	Set the TRIAC to the ON position and adjust the rheostat for 5 amps load current.	5 amp current flow through the load	✓	5 amp current observed through load
3	Repeat steps 1 and 2 with the rheostat adjusted for 10, 15 and 20 amps.	10, 15 and 20 amps current flow through the load	✓	Respective currents observed through load

Test Name:	Electrical - Load Switch - Switching Control – Test 6			
Setup:	Modify TRIAC load circuit to monitor load voltage with an oscilloscope.			
Steps	Action	Expected Results	Passed	Comments
1	Set the TRIAC to the OFF position	No current flow through the load	✓	
2	Set the TRIAC to the ON position	Current flow through the load	✓	
3	Turn TRIAC to the OFF position	Verify with oscilloscope that TRIAC shuts off at next zero crossing of ac waveform	✓	Current ends flow at next zero crossing of AC line

Test Name:	Electrical - Load Switch - Temperature Measurements – Test 7			
Setup:	Same setup as for TRIAC Load Switching			
Steps	Action	Expected Results	Passed	Comments
1	Apply loads ranging from 0A to 20A (maximum)		✓	
2	Measure temperature for all applied currents	Allow sufficient time for temperature to stabilize	✓	
3	Generate a temperature vs current plot	Temperature will increase with load current	✓	
4	Verify if measured temperatures are acceptable for application	A maximum temperature rise of 20 C.	✓	Prototype hardware reveals high current loads should not be run for extended periods

Test Name:	Electrical – Controller – Firmware – Test 8			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	2-Way I2C communication		✓	Logic analyzer used to verify
2	Turn load switch on/off	Current will/will not flow	✓	
3	Calculate average power compared to measured average	Within required 10%	✓	10% error at 29W, 4% error at 55W

Test Name:	Web App - Signing In – Test 9			
Setup:	The web application is running			
Steps	Action	Expected Results	Passed	Comments
1	Load into the web application		✓	Working
2	Enter Invalid username/password	Invalid username/password message	✓	
3	Enter valid username/password	Application loads	✓	

Test Name:	Web App - Viewing Charts – Test 10			
Setup:	Logged into web application			
Steps	Action	Expected Results	Passed	Comments
1	Go to the 'charts' tab	Chart interface appears	✓	
2	Select a single outlet	Default' chart appears for that outlet	**X**	Not Implemented
3	Cycle through all time divisions for all measurement types for all time scales	Chart should display the appropriate time divisions for the appropriate measurement type, for the appropriate time scale	✓	
4	Select a group of outlets	Default' chart appears for that outlet	**X**	Group selection, but no default chart
5	Cycle through all time divisions for all measurement types for all time scales	Chart should display the appropriate time divisions for the appropriate measurement type, for the appropriate time scale	✓	

Test Name:	Web App - Naming Outlets – Test 11			
Setup:	Logged into web application			
Steps	Action	Expected Results	Passed	Comments
1	Select an outlet in the table		✓	
2	Click edit/double click	Naming window appears	✓	
3	Enter a new name	Screen reflects entry	✓	
4	Save the name	Window closes and table updates, reflecting the new name	✓	

Test Name:	Web App - Grouping Outlets – Test 12			
Setup:	Logged into web application			
Steps	Action	Expected Results	Passed	Comments
1	Navigate to the 'home' tab		✓	
2	Click “New” under groups section	Grouping interface appears	✓	
3	Enter name/description	Screen reflects entry	✓	
4	Select outlet(s), then press “>”	Selected outlets are in the right box	✓	
5	Press save	Window closes, new group appears in groups section	✓	

Test Name:	Web App - Scheduling Interface – Test 13			
Setup:	Logged into web application			
Steps	Action	Expected Results	Passed	Comments
1	Navigate to the 'scheduling' tab	The scheduling interface appears	✓	Recurring events not implemented, otherwise working
2	Create a single (one-time) event	The event appears on the calendar	✓	
3	Edit the event	The event changes on the calendar	✓	
4	Create another event		✓	
5	Set this event to recurring on Wednesdays	The same event appears on every Wednesday	X	
6	Delete a single instance of this event	That one instance is removed	✓	
7	Create multiple events of different types	The schedule handles all of the events	X	
8	Multiple events on a single day		✓	

Test Name:	Web App - Scheduling Job – Test 14			
Setup:	The web application is running (this is a background process)			
Steps	Action	Expected Results	Passed	Comments
1	Create a simple schedule using the web interface		✓	Maximum error of 1 minute off
2	Close the application		✓	
3	Using text output in a log file, verify that events are happening at scheduled times	The scheduled events are being fired on time	✓	

Test Name:	Web App - Toggle outlet state – Test 15			
Setup:	Logged into web application			
Steps	Action	Expected Results	Passed	Comments
1	Navigate to the 'Home' tab		✓	
2	Select an outlet in the table	Outlet highlighted	✓	
3	Observe active state	Should either be true or false	✓	
4	Press “On” button	Table is updated and outlet active is true	✓	
5	Press “Off” button	Table is updated and outlet active is false	✓	

Test Name:	Web App – Settings – Test 16			
Setup:	Logged into web application			
Steps	Action	Expected Results	Passed	Comments
1	Navigate to the 'settings' tab	Settings interface appears	✓	Not Implemented
2	Change each setting	Verify the settings update on screen	**X**	
3		Verify settings are reflected in other locations	**X**	
4		Verify settings are reflected in database	**X**	

Test Name:	Database - Load Test – Test 17			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Insert 1000 rows per second for 10 seconds	10,000 rows are in the database	✓	No performance impact detected
2	Read all of the rows from the database	All 10,000 rows are correctly read from the database	✓	

Test Name:	Database - Insert Outlet Module Data – Test 18			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Insert data for one outlet module	1 outlet module has been added to the database	✓	
2	Read the data for the inserted outlet module	The correct data is read from the database	✓	Automatic entry to database is accurate

Test Name:	Database – Insert Outlet Reading Data – Test 19			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Insert data for one outlet reading	One outlet reading has been added to the database	✓	
2	Read the data for the inserted outlet reading	The correct data is read from the database	✓	

Test Name:	Database – Compression of Data – Test 20			
Setup:	Outlet readings that are 2 days old			
Steps	Action	Expected Results	Passed	Comments
1	Set (or wait for) data to be 2+ days old.	Data from 1 days ago is now 2+ days ago	✓	
2	Validate averaged data	The averaged data should be correct from averaging outlet readings into 1 hour segments	✓	

12.2 INTEGRATION TESTS

Test Name:	Electrical - Voltage Sense with Controller – Test 21			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Read a static voltage from the voltage sense circuitry	Valid voltage measurement computed in processor	✓	
2	Read in a dynamic voltage at frequencies up to 10kHz	Valid voltage measurement computed in processor	✓	
3	Verify processor average voltage calculation	Valid average voltage calculated	✓	Error within 1% for 29W load
4	Calculate frequency of voltage waveform	Valid voltage waveform frequency determined	X	Feature Removed

Test Name:	Electrical - Current Sense with Controller – Test 22			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Read a static current from the current sense circuitry	Valid current measurement computed in processor	✓	
2	Read in a dynamic current at frequencies up to 10kHz	Valid current measurement computed in processor	✓	
3	Verify processor average current calculation	Valid average current calculated	✓	9.5% error at 29W, ~0% error at 55W

Test Name:	Electrical - Load Switch with Controller – Test 23			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Processor Request to turn load switch ON	Verify load switch is in ON state	✓	
2	Processor Request to turn load switch OFF	Verify load switch is in OFF state	✓	

Test Name:	Web App - Receive Database Information – Test 24			
Setup:	Logged into web application and database is running and connected			
Steps	Action	Expected Results	Passed	Comments
1	View the list of outlets	All current outlets should be displayed	✓	
2	View the list of groups	All groups are shown with appropriate outlets	✓	
3	View many charts	Calculate and verify that the charts are displaying the correct information	✓	
4	View the settings	Verify settings match database settings	**X**	Not Implemented
5	Manually add outlet to database and refresh data	Outlet should appear in list	✓	Handled automatically
6	Manually change settings and refresh	New settings should appear in app	**X**	Not Implemented

Test Name:	Web App - Send Database Information – Test 25			
Setup:	Logged into web application and database is running and connected			
Steps	Action	Expected Results	Passed	Comments
1	Rename an outlet	Verify data in database	✓	
2	Create/edit groups	Verify data in database	✓	
3	Change settings	Verify data in database	**X**	Not Implemented
4	Create new user account	Verify data in database	**X**	Not Implemented
5	Toggle status of outlet or group	Verify data in database	✓	

Test Name:	Web App / Database – Requesting Real-time Readings – Test 26			
Setup:	Logged into web application and database is running and connected			
Steps	Action	Expected Results	Passed	Comments
1	Go to the 'charts' tab	Chart interface appears	✓	Feature Abandoned, feature replaced with 5 minute time scale with 1 second interval
2	Select a single outlet	Default' chart appears for that outlet	✓	
3	Select real-time update	Chart displays real-time information, readings in database have real-time flag set to 1	**X**	
4	End user session	User session ends, real-time readings are removed from the database	**X**	

12.3 ACCEPTANCE TESTS

Test Name:	Module Costs – Test 27			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Calculate component, shipping, and fabrication costs for Outlet Module	Cost should not exceed $50	**X**	Expected to pass within production
2	Calculate component, shipping, and fabrication costs for Main Module	Cost should not exceed $200	**X**	

Test Name:	Short Installation Time – Test 28			
Setup:	Obtain Main Module, Outlet Module(s)			
Steps	Action	Expected Results	Passed	Comments
1	Have certified Electrician Replace/Install each Outlet Module	Installation of each module should not exceed 30 minutes	**X**	Expected to pass within production
2	Have certified Electrician Replace/Install the Main Module	Installation and configuration of main module should not exceed 2 hours	**X**	

Test Name:	Power Measurement Accuracy Test – Test 29			
Setup:	Apply AC mains to system, provide various resistances			
Steps	Action	Expected Results	Passed	Comments
1	Apply various resistors (fixing the current), and obtain the power consumption results	For each resistor, verify that the measured power is within 10% of the fixed power usage	✓	

Test Name:	Usability Test – Test 30			
Setup:	Professionally installed modules, Provided an hour of familiarization with application			
Steps	Action	Expected Results	Passed	Comments
1	User navigates to application or web interface	Page opens to login screen, unless otherwise configured	✓	
2	User enters login credentials (existing user or default credentials)	Success within 3 minutes	✓	
3	Name an outlet module	Success within 5 minutes	✓	
4	View usage statistics of a single module	Success within 5 minutes	✓	
5	Turn an outlet module on/off	Success within 5 minutes	✓	
6	remove an outlet module	Success within 5 minutes	**X**	Abandoned, as not applicable
7	reach and configure schedule	Success within 5 minutes	✓	

Test Name:	Outlet Module Sizing – Test 31			
Setup:	Outlet Module is fabricated and constructed			
Steps	Action	Expected Results	Passed	Comments
1	Place outlet module in (at the maximum size) a 22 cubic inch electrical box.	Should sit flat with faceplate, without bulging out of the box	**X**	Expected to pass in production
2	Wire the electrical box and module with mains cabling	Should sit flat with faceplate, without bulging out of the box	**X**	

Test Name:	Load Testing – Test 32			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Connect a single module, with default communication rate	Data communication sufficiently low that data is received without issue	✓	
2	Connect a single module, with real-time communication rate	Data communication sufficiently low that data is received without issue	✓	
3	Connect up to 10 modules, with real-time communication rate	Data communication sufficiently low that data is received without issue	**X**	Could not test without multiple outlets
4	Connect 100 Modules, with default communication rate	Data communication sufficiently low that data is received without issue	**X**	
5	Connect 100 Modules, with 5 in real-time communication mode	Data communication sufficiently low that data is received without issue	**X**	

Test Name:	Schedule testing – Test 33			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Navigate to the 'scheduling' tab	The scheduling interface appears	✓	
2	Create a single (one-time) event	The event appears on the calendar	✓	
3	Observe outlet before/after scheduled time	Outlet should turn On/Off according to schedule	✓	
4	Create another event		✓	
5	Set this event to recurring on Wednesdays	The same event appears on every Wednesday	X	Feature not implemented
6	Observe outlet before/after scheduled time multiple days	Outlet should turn On/Off according to the schedule	X	
7	Delete a single instance of this event	That one instance is removed	✓	
8	Observe outlet before/after the previous scheduled time	The outlet should no longer be controlled by this scheduled event	✓	

Test Name:	Remote Tests – Test 34			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Navigate to the 'Home' tab	Outlets pane is shown	✓	
2	Select a target outlet		✓	
3	Turn outlet on	The outlet should now be on, without affecting other outlets	✓	
4	Turn outlet off	The outlet should now be off, without affecting other outlets	✓	

Test Name:	High Pot Testing – Test 35			
Setup:	Short all control terminals together and all power terminals together			
Steps	Action	Expected Results	Passed	Comments
1	Apply a 1500VAC using a high pot tester between the control and power circuits	No indication of breakdown	✓	Verified via analysis

Test Name:	Power Line Transient Survival – Test 36			
Setup:	Connect a transient pulse generator to the power line input			
Steps	Action	Expected Results	Passed	Comments
1	Apply a impulse voltage per IEC-60664-1	No indication of component failure	✓	Verified via analysis
2	Perform a functional test of the unit, post-impulse test	Functional test results as expected	**X**	N/A
NOTE	If an impulse tester is not available this test will be verified through analysis.			

Test Name:	Efficiency – Test 37			
Setup:				
Steps	Action	Expected Results	Passed	Comments
1	Measure power of non full load with kill-a-watt going into remote module		✓	74.6 W
2	Measure power usage of remote module + the same load attached to the module, calculate efficiency	Efficiency must be greater than 95%	✓	77.4 W without Main module, 96.4% Efficient. Maximum load would be around 2.5kW, which would yield a far better efficiency

12.4 TEST COVERAGE MATRIX

	Engineering Requirement												
Test Number	A	B	C	D	E	F	G	H	I	J	K	L	M
1					X	X							
2						X			X				
3						X			X				
4											X		
5						X					X		
6					X								
7					X								
8					X	X	X					X	X
9							X	X					
10							X	X				X	
11							X	X				X	
12							X	X					
13							X	X					
14							X	X				X	
15					X		X	X				X	
16							X	X					
17							X						
18												X	
19							X					X	
20							X	X					
21						X							
22						X							
23					X								
24							X					X	
25							X						
26							X						
27	X												
28		X								X			
29						X							
30					X	X	X	X				X	
31		X								X			
32					X								X
33							X	X					
34					X		X	X					
35				X									
36			X										
37											X		

12.5 FIRMWARE APPENDIX

12.5.1 FPGA RX Command Structure

The FPGA RX command structure is as follows:

OPCODE	PAYLOAD

12.5.1.1 Load Switch Command (Opcode – 00)

This command is used by the main module to toggle the load ON or OFF. The operation of this command is shown below:

OP		Payload						
7	6	5	4	3	2	1	0	
0	0	1	0	1	0	1	0	ON
0	0	X	X	X	X	X	X	OFF

12.5.1.2 Current Limit Command (Opcode – 01)

This command is used by the main module to set the current limit of the FPGA. This command allows current limits to be set with a resolution of 0.5A. Payload value represents magnitude of current limit. Only values ranging from 0-26 A can be set. Setting a value of 5A means that the current will be limited to +- 5A. The operation of this command is shown below:

OP		Payload					
7	6	5	4	3	2	1	0
0	1	X	X	X	X	X	X

A detailed table which relates the payload, current limits, and digital ranges is provided below:

	0A Votlage	1.6784					
Payload	Current Limits	Low Range Voltage Limit	High Range Voltage Limit	Low Range Digital Limit	High Range Analog Limit	Low Range Hex	High Range Hex
0	0	1.6784	1.6784	2083	2084	823	824
1	0.5	1.64555	1.71125	2042	2125	7FA	84D
2	1	1.6127	1.7441	2001	2165	7D1	875
3	1.5	1.57985	1.77695	1960	2206	7A8	89E

4	2	1.547	1.8098	1920	2247	780	8C7
5	2.5	1.51415	1.84265	1879	2288	757	8F0
6	3	1.4813	1.8755	1838	2328	72E	918
7	3.5	1.44845	1.90835	1797	2369	705	941
8	4	1.4156	1.9412	1757	2410	6DD	96A
9	4.5	1.38275	1.97405	1716	2451	6B4	993
10	5	1.3499	2.0069	1675	2491	68B	9BB
11	5.5	1.31705	2.03975	1634	2532	662	9E4
12	6	1.2842	2.0726	1593	2573	639	A0D
13	6.5	1.25135	2.10545	1553	2614	611	A36
14	7	1.2185	2.1383	1512	2655	5E8	A5F
15	7.5	1.18565	2.17115	1471	2695	5BF	A87
16	8	1.1528	2.204	1430	2736	596	AB0
17	8.5	1.11995	2.23685	1390	2777	56E	AD9
18	9	1.0871	2.2697	1349	2818	545	B02
19	9.5	1.05425	2.30255	1308	2858	51C	B2A
20	10	1.0214	2.3354	1267	2899	4F3	B53
21	10.5	0.98855	2.36825	1227	2940	4CB	B7C
22	11	0.9557	2.4011	1186	2981	4A2	BA5
23	11.5	0.92285	2.43395	1145	3022	479	BCE
24	12	0.89	2.4668	1104	3062	450	BF6
25	12.5	0.85715	2.49965	1063	3103	427	C1F
26	13	0.8243	2.5325	1023	3144	3FF	C48
27	13.5	0.79145	2.56535	982	3185	3D6	C71
28	14	0.7586	2.5982	941	3225	3AD	C99
29	14.5	0.72575	2.63105	900	3266	384	CC2
30	15	0.6929	2.6639	860	3307	35C	CEB
31	15.5	0.66005	2.69675	819	3348	333	D14
32	16	0.6272	2.7296	778	3389	30A	D3D
33	16.5	0.59435	2.76245	737	3429	2E1	D65
34	17	0.5615	2.7953	696	3470	2B8	D8E
35	17.5	0.52865	2.82815	656	3511	290	DB7
36	18	0.4958	2.861	615	3552	267	DE0
37	18.5	0.46295	2.89385	574	3592	23E	E08
38	19	0.4301	2.9267	533	3633	215	E31
39	19.5	0.39725	2.95955	493	3674	1ED	E5A
40	20	0.3644	2.9924	452	3715	1C4	E83
41	20.5	0.33155	3.02525	411	3755	19B	EAB
42	21	0.2987	3.0581	370	3796	172	ED4
43	21.5	0.26585	3.09095	329	3837	149	EFD
44	22	0.233	3.1238	289	3878	121	F26

45	22.5	0.20015	3.15665	248	3919	F8	F4F
46	23	0.1673	3.1895	207	3959	CF	F77
47	23.5	0.13445	3.22235	166	4000	A6	FA0
48	24	0.1016	3.2552	126	4041	7E	FC9
49	24.5	0.06875	3.28805	85	4082	55	FF2
50	25	0.0359	3.3209	44	4122	2C	FFF
51	25.5	0.00305	3.35375	3	4163	3	FFF
52	26	-0.0298	3.3866	-37	4204	0	FFF
53	26.5	-0.06265	3.41945	-78	4245	0	FFF
54	27	-0.0955	3.4523	-119	4286	0	FFF
55	27.5	-0.12835	3.48515	-160	4326	0	FFF
56	28	-0.1612	3.518	-201	4367	0	FFF
57	28.5	-0.19405	3.55085	-241	4408	0	FFF
58	29	-0.2269	3.5837	-282	4449	0	FFF
59	29.5	-0.25975	3.61655	-323	4489	0	FFF
60	30	-0.2926	3.6494	-364	4530	0	FFF
61	30.5	-0.32545	3.68225	-404	4571	0	FFF
62	31	-0.3583	3.7151	-445	4612	0	FFF
63	31.5	-0.39115	3.74795	-486	4653	0	FFF

12.5.1.3 Transmit Time Set – (Opcode – 10)

This command is used by the main module to specify the time between transmissions from the FPGA to the main module. The payload value represents offsets from 1 second (the minimum transmission speed). Each bit has a resolution of 250 ms. The operation of this command is shown below:

OP		Payload					
7	6	5	4	3	2	1	0
1	0	X	X	X	X	X	X

A detailed table which relates the payload, offset time, and digital count values used within the FPGA to obtain these delays is provided below:

Payload	Offset Time	FPGA Count
0	1	
1	1.25	250
2	1.5	500
3	1.75	750
4	2	1000
5	2.25	1250

6	2.5	1500
7	2.75	1750
8	3	2000
9	3.25	2250
10	3.5	2500
11	3.75	2750
12	4	3000
13	4.25	3250
14	4.5	3500
15	4.75	3750
16	5	4000
17	5.25	4250
18	5.5	4500
19	5.75	4750
20	6	5000
21	6.25	5250
22	6.5	5500
23	6.75	5750
24	7	6000
25	7.25	6250
26	7.5	6500
27	7.75	6750
28	8	7000
29	8.25	7250
30	8.5	7500
31	8.75	7750
32	9	8000
33	9.25	8250
34	9.5	8500
35	9.75	8750
36	10	9000
37	10.25	9250
38	10.5	9500
39	10.75	9750
40	11	10000
41	11.25	10250
42	11.5	10500
43	11.75	10750
44	12	11000
45	12.25	11250
46	12.5	11500

47	12.75	11750
48	13	12000
49	13.25	12250
50	13.5	12500
51	13.75	12750
52	14	13000
53	14.25	13250
54	14.5	13500
55	14.75	13750
56	15	14000
57	15.25	14250
58	15.5	14500
59	15.75	14750
60	16	15000
61	16.25	15250
62	16.5	15500
63	16.75	15750

12.5.1.4Dimming Command (Opcode – 11)

This command was not implemented in the prototype system. In production this command would be used to set the desired dimming value as specified by the main module.

12.5.2 Power Calculations

The following embedded spreadsheet documents the complete power calculation which takes place within the FPGA.