Weekly Progress Report

Project Name: Energy Management System (EMS)
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Collaborators:

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Project URL: https://edge.rit.edu/edge/C15505/public/index.html

Updated Milestone Chart:

Updates from previous revisions are italicized for clarity.

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Critical Component Breakout Boards	8/24/2015	RM, DM	9/28/2015	Critical component breakout boards have been completed for all functions. Messages have successfully been sent through the power line using the provided evaluation boards.
User Interface Implementation	8/24/2015	JL, AC	11/02/2015	Rest of system does not heavily depend on webapp so completion delay is not a large factor. This milestone has slipped again from its previous date of 10/12
Web App Database Communication	8/24/2015	AC, JL	9/13/2015	The web application is able to communicate with the database using Hibernate (An Object-Relational Mapping library for Java)

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Order Parts	8/24/2015	All	9/20/2015	Cypress has provided a new PLC evaluation kit which functions correctly.
Initial PCB Design	8/31/2015	DM	9/6/2015	Focusing efforts on vero-boarding initial hardware design instead of PCB design. Breadboard has been constructed. PCB may still be constructed if time permits, but based on summer slippage time for spinning PCB my not be available. Completion of breadboard has met the intent of this task.
Obtain and Verify Parts	9/7/2015	All	9/20/2015	All parts except PLC have been received and verified. Completion date has been pushed back as received evaluation PLC boards are not functioning properly.
Verification of Power Supply Circuitry	9/14/2015	DM	9/14/2015	Power Supply circuitry has been verified.
Verification of Breadboard Load Switch	9/14/2015	DM	9/14/2015	Load Switch is operational, and a load is able to be switched ON and OFF via an external voltage (provided from FPGA or other embedded system).
Verification of Breadboard Current Sense	9/21/2015	DM	9/21/2015	Current sense circuitry is operational.
Verification of Breadboard Voltage Sense	9/21/2015	DM	9/21/2015	Voltage sense circuitry is operational
Outlet Communication	9/28/2015	RM	9/25/2015	Messages have been successfully sent via the power line.

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
with PLC				
Interface PLC with Pi	9/28/2015	RM, JL	10/7/2015	Team has decided to acquire PLC evaluation boards. PLC communication is occurring with the PI but communications does not work consistently. Communication has improved from last status report, and various issues have been discovered and solved. Team successfully sent messages from Pi to FPGA.
Verification of Breadboard Processor	10/5/2015	All	10/9/2015	FPGA has been selected to perform necessary embedded processing. Necessary power calculation is working properly within Modelsim simulation using a bus functional model of the ADC. FPGA I2C interface necessary for PLC communication has also been simulated. Team is working on determining final communication protocol between FPGA and Pi. All VHDL has been synthesized successfully. Messages have successfully been sent from FPGA to PLC to Pi (Both ways have been tested and are working)
Final PCB Design	10/19/2015	All	10/18/2015	*Based on team progress to this point, the decision has been made not to have a PCB manufactured. Completion of veroboard has met the intent of this task and shall be used for verifying functionality of the project.*
Finalized Database Structure	10/19/2015	AC, JL	11/02/2015	This will be a result of the webapp completion.

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
PI PLC API	10/26/2015	RM, AC, JL		
System recognizes new outlets automatically	11/2/2015	All		
Send Hardware Measurement over PLC	11/9/2015	RM, JL, DM		
Receive and store measured data	11/9/2015	AC, JL, RM		
View measured data	11/9/2015	JL, AC		
Toggle state of single outlet from web interface	11/16/2015	All		
Toggle state of a group of outlets	11/16/2015	All		
Outlets and groups follow schedule	11/16/2015	All		
Data Compression Verification	11/16/2015	AC		
Full system test passed	11/25/2015	All		

Current Milestones:

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Final PCB Design	10/19/2015	All	10/18/2015	*Based on team progress to this point, the decision has been made not to have a PCB manufactured. Completion of veroboard has met the intent of this task and shall be used for verifying functionality of the project.*
User Interface Implementation	8/24/2015	JL, AC	11/02/2015	Rest of system does not heavily depend on webapp so completion delay is not a large factor. This milestone has slipped again from its previous date of 9/28.
PI PLC API	10/26/2015	RM, AC, JL		

Next Milestones:

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
System recognizes new outlets automatically	11/2/2015	All		
Send Hardware	11/9/2015	RM, JL, DM		

Task Description	Original Scheduled Completion Date	Responsible Team Member	Modified Completion Date	Comments
Measurement over PLC				
Receive and store measured data	11/9/2015	AC, JL, RM		

Status

Difficulties:

Currently experiencing intermittent PLC to Raspberry Pi communication. Team is currently working on debugging issues. Over the course of the last week team has discovered and resolved several issues.

Team is also working to establish a method which will allow for the PLC hardware to interrupt Pi/FPGA when an update is received instead of the Pi/FPGAs having to poll PLC status registers.

Surprises

PLC PSoC can only perform PLC functions and cannot perform any calculations on voltage current data. Therefore an additional embedded platform will be needed to perform controller functionality.

Successes:

Team has officially decided to use an FPGA to perform necessary embedded platform calculations, and I2C communications. Necessary VHDL has been developed to perform power calculations. A detailed simulation environment was then created to verify the VHDL firmware. ADC was modeled with bus functional model such that they are able to receive an analog value

and serially shift out a digital value representing the analog voltage processed. VHDL has been seen to work properly within simulation. VHDL has also been synthesized and downloaded to hardware. I2C VHDL code has also been generated such that the FPGA is able to send and receive I2C messages. This has been tested through simulation and is seen to be working. I2C code has also been synthesized and is correctly working in hardware. This week team was able to successfully send a message throughout the system in both directions (FPGA to PLC to Pi).

The “Home Tab” of the web application is complete. This means that outlets can be modified and groups can be created/updated/deleted successfully. The next major step, the “Charts” tab, is being implemented now.

Questions/problems for consideration:

We have decided not to make an overall PCB but to develop a working hardware prototype on vero-board which can be used to demonstrate the functionality of the system, and if time/budget permits then complete a PCB design.

Determine if the Raspberry Pi (main module), will be able to process I2C messages via interrupts or if polling will have to be used.

Team is considering moving proposal document from a word document to a LaTeX document to avoid Figure number issues etc.

We are making a design change within the web application. We are switching from using the Python based Django framework to the Java based Vaadin framework. This is being done because the team is more familiar with Java and the Vaadin framework and also because Java is a more powerful platform for development. This means we will need a way for the Java app to talk to native Python scripts running on the Raspberry Pi (possibly Jython) and that the web application will use significantly more system memory. Some additional tests will be run in the near future to ensure the memory usage is not too high.

Gantt Chart:

Task Mode	Task Name	Resource Names
	Energy Management Systsem	
	Critical Component Breakout Board Design	RM,DM
	User Interface Implementation	AC,JL
	Order Parts	All
	Initial PCB Design	DM
	Obtain and Verify Parts	All
	Verification of Power Supply	DM
	Verification of Breadboad Load Switch	DM
	Verification of Breadboard Current Sense	DM
	Verification of Breadboard Voltage Sense	DM
	Outlet Communication with PLC	RM
	Interface PLC with Pi	JL,RM
	Verification of Breadboard Processor	All
	Final PCB Design	All
	Finizlized Database Structure	AC,JL
	PI PLC API	RM,AC,JL
	System recognizes new outlets automatically	All
	Send Hardware Measurement over PLC	RM,JL,DM
	Receive and store measured data	AC,JL,RM
	View Measured Data	JL,AC
	Toggle state of single outlet from web interface	All
	Toggle state of a group of outlets	All
	Outlets and groups follow schedule	All
	Data Compression Verification	AC
	Full System Test Passed	All