Energy Management System

A modular solution for power monitoring and management for homes and small businesses

High-Risk Assessment: Power Line Communication

An efficient, robust power line communication module is necessary to ensure the successful operation of the EMS.

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Overview

The Power Management System operates utilizing a central module in conjunction with numerous remote outlet modules. In order to collect data from remote modules, as well as issue commands to those modules, the central module must be able to both transmit and receive data via power line communication. The remote modules must in turn be able to transmit the usage data, as well as receive commands from the central module. Thus a reliable communication is necessary to guarantee the safe and useful operation of the system. In addition, inclusion of advanced features, such as error checking and collision avoidance within the PLC module are beneficial as they could significantly simplify the design of the remote modules (which are meant to be low cost).

Risk Specification

Marketing Requirements

1. The system shall allow for control of individual outlets.
2. The system shall be safe.
3. The system shall have low cost in comparison to competitive products.
4. The system shall be of reasonable size in comparison to existing systems.
5. The system shall communicate usage data and commands between outlets and the main module.

Engineering Specifications

Marketing requirements	Engineering Requirements	Justification
3	A. Production cost should not exceed $200 for the main unit and $30 for the outlet modules.	This is based upon analysis of a competitive market and current design requirements.
2	B. Control circuits shall be isolated from power line by 1250V RMS minimum.	Electrical isolation is required by safety agencies for equipment connected to the AC power line.
2	C. The system shall use only UL recognized components.	Safety agency approvals will be required to sell product commercially.
4	D. The system shall be able to fit into current standard electrical outlets.	To be fully integrated and competitive, the system must be able to replace current outlets.
1,5	E. Wall units shall be identifiable.	This allows the system to know what information is coming from what wall unit and to provide individual control.
1,5	F. All modules should be able to transmit at a BPS rate sufficient to relay commands and usage data at the chosen sampling frequency.	In order to have reliable communication, the modules must have an adequate minimum communication rate.

Risk Investigation

The main concerns of a Power Line Communication module relate to the robustness of the communication. An ideal chip must include collision avoidance/detection and a method to resend, as well as a communication rate high enough to support the "maximum" supported modules connected to the system. Another topic of interest is the interface shared with the chip, as it should be easily controllable by a microcontroller for implementation.

As the communication rate for many modules in specified in a bps format, including the package's header and other transmission information (CRC error detection/repair bits, etc), the necessary transmission rate will depend on the chosen chip. As an estimate, the transmission rate, in bits/sec must at least meet this requirement:

$$B > M * (P[bits] + D[bits]) * (F_s) \quad (1)$$

Where B, M, P, D, and F_s are respectively: the minimum supported bitrate of an adequate chip [bits/second], the number of outlet modules, any non-data transmission information (such as packet headers, CRC bits, etc), the number of actual data bits per transmission, and the sampling frequency of a single module. Note that this is merely a minimum requirement – sending commands from the main module will add further data requirements but will be considerably less frequent, and so was not included here. Additionally, resending of data may also impact the necessary transmission rate, but is chip dependent.

Because of concerns as to achieving the minimum data rate, it was determined that power would be measured and transmitted for single gangs (2 outlets – not for each single outlet) while each outlet would remain individually controllable. This makes it so the system could support roughly twice the number of outlets for a given data rate. There are many formats and contents of data that could be transmitted to convey power usage. The two primary choices for power usage transmission are either: transmit only power, or transmit three components – as current, voltage, and power factor – that allow for calculation of power. While the three component transmission would utilize more data, it would allow for users to view data relating to voltage levels, which is a unique feature that could help users identify issues with wiring and connections. For transmission of three components, many of the components could be reduced so save on the number of transmitted bits. Voltage could be transmitted as a distance from 100 V (or a similar number) utilizing a 5 bit number to range between 100 & 131 volts. Current could be specified with an accuracy of about 16.5 mA using a 10 bit resolution, and the power factor ranges from 1 to -1, which could be specified in 8 bits which would give an accuracy of 0.008.

All of these considerations impact the rough estimate shown in Equation 1, and create two different equations based on the chosen power transmission scheme. Another factor is that if the address bits of the packet header are not easily accessible, or if they change dynamically, then each transmission will be required to transmit an ID. The number of ID bits will be dependent on the number of supported outlet modules (M) which have two outlets per gang. As their data will be combined, this is not a concern for

the sending of usage data, but an additional ID bit will be required to send commands to individual outlets, and not the entire module. The number of ID bits for transmissions from gangs will be the ceiling function of $\log_2(M)$, in order to provide just enough bits for unique identifiers. Equation 2 shows the estimation equation for transmissions sending only power data, while Equation 3 shows the estimation equation for transmissions sending power factor, voltage, and current data. Please note that this assumes data is transmitted in a single packet, and requires modification to estimate multi-packet transmissions. The square brackets surrounding the ID section indicate that it may or may not be necessary depending on the chosen chip.

$$B > M * (P + [[log_2(M)]] + Power) * (F_s) \quad (2)$$

$$B > M * (P + [[log_2(M)]] + V + I + PF) * (F_s) \quad (3)$$

Respective minimum data requirements were then calculated using Equations 2 & 3, along with the assumptions of 0 packet headers with only ID (true minimum packet header size in reality), a single component power indicated with 11 bits, a voltage indicated with 5 bits, a current with 10 bits, and a power factor resolution with 8 bits. Additionally, the M (modules) was chosen as 50, with a transmission frequency of once every 15 seconds. Utilizing these values, the minimum required bandwidth for single component power was estimated at 57 bps, with a 3 component power requirement of 97 bps.

To allow for near real time viewing of data, it would be practical to have the ability for the main module to request a non-default transmit rate. For example, all modules could transmit once every 15 seconds, but the main module could request a certain light (or group of lights) send at a rate of once per second, for real time viewing. Assuming the default frequency is F_D, and the real time viewing frequency is F_R, and the maximum number of items in a real time viewing group is M_R, then Equations 2 and 3 can be modified as shown in Equations 4 and 5 respectively.

$$B > (MF_D + M_R F_R - M_R F_D) * (P + [[log_2(M)]] + Power) \quad (4)$$

$$B > (MF_D + M_R F_R - M_R F_D) * (P + [[log_2(M)]] + V + I + PF) \quad (5)$$

Assuming the prior assumptions, and that the biggest real time group with a frequency of one transmission per second is 5 modules, the minimum bandwidth for a perfect transmission, no collision model would be 136 bps for a single power component transmission, or 232 bps for a 3 component power transmission model.

Part	Packet Bits	Required Data Rate (x1 Component)	Required Data Rate (x3 Component)	Provided Data Rate	Collision Provisions	Interface	Programmable MC?
CY8CPLC10	56	536	632	2400	Yes	I2C	No
CY8CPLC20	56	536	632	2400	Yes	I2C, UART	Maybe

ST7540	0			4800	No	UART/SPI	No
ST7570	112-336	984-2688	1080-2688	2400	Yes	UART	No
ST7590				128000	Yes	UART/SPI	Maybe
MAX2992				300000	Yes	UART/SPI	Maybe
ATSAM4CP16B				128000	Yes	UART/SPI	Yes
TDA5051A	0			1200	no	Digital	no

At this point, further analysis is required. Smaller, less complex chips provide a smaller bandwidth as well as require the implementation of a MAC layer to handle collisions in general. Many of these smaller chips have a high enough data rate to be expected to work with the rough estimate values utilized, but won't expand far beyond that rate. The advantage of the less complex chips is that although they may be physically larger, they have relatively simple functionality and few pins to route. On the same token, the more complex chips have a larger bit rate, smaller area (but larger routing concerns), more complex operation, and come with MAC layers to handle collisions. The more complex chips were also difficult to obtain packet data for – They have a high enough data rate that is not a real concern, but it would be convenient to know. Additionally, the more complex chips are expected to cost more, so less complex alternatives that fit the requirements may be better. Ultimately, if the routing area of the complex chips is difficult to contain within a standard electrical box, then the simple chips may be a cheaper and better option, even if it requires reducing the number of modules supported if there are unforeseen issues. The more complex chips provide for much better performance (real time data), while also leaving a larger error margin to overcome unforeseen data requirements. The most likely candidates for simple chips would be the Cypress CY8CPLC family, or the ST7540 (which would require manual implementation of a MAC layer, but have a higher data rate). The more complex chips were difficult to obtain meaningful data for, and so would require a more in-depth analysis, including investigation of cost and typical applications.

Risk Mitigation Design

Overview

While no specific module was deemed best, as there are a number of requirements to still be determined, the risk mitigation design shall continue by choosing the Cypress CY8CPLC10 chip, which is very close in design to the CY8CPLC20. The Cypress chips appear to be a good balance, having an average number of pins falling between the extremes of 16 and 48. This prevents the chip from being complex to route, while still providing some of the more advanced features, including collision avoidance, detection, and retransmission. Choosing the CY8CPLC10 chip allows the focus to remain on the data being sent, and how to connect the chips, rather than focusing on the details of communication.

Design

The pinout of the CY8CPLC10 28-pin SSOP is shown in Figure 1.

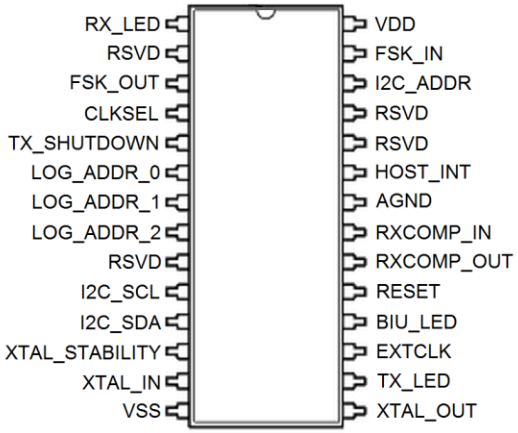

Figure 1. CY8CPLC10 Pinout

Because PLC is a mature technology, the operation of the PLC chip is relatively straight forward. The chip is connected to the main microcontroller using I2C to communicate to the PLC chip. Each module will be equipped with the chosen PLC chip, which will simply act as a black box system to pass information from the outlet modules to the main modules, and vice versa. A simplified view of the system is shown below, in Figure 2.

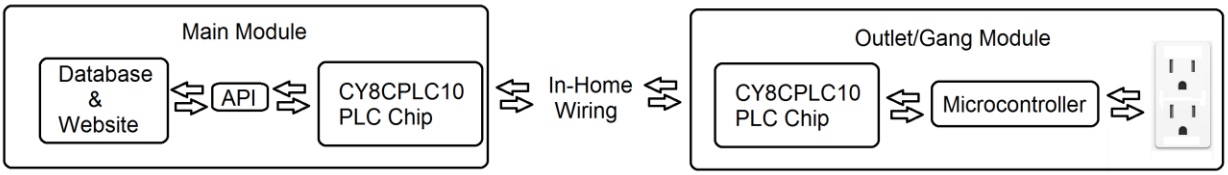

Figure 2. PLC System Overview

Figure 2 shows that each module is equipped with one of the selected PLC chips, and uses it as an interface with other modules. In the case of the Main Module, it interacts with each of the Outlet Modules via the PLC chip. Each Outlet Module need only directly interact with the Main Module however. Each Outlet Module consists of a “gang” (2 outlets) equipped with a single microcontroller, a single PLC chip, coupling, control, and measurement hardware. At the interval specified by the Main Module, the Outlet Modules’ microcontroller will average the power consumption and send the data to the Main Module via the PLC chip. The transmission frequency will be variable, so that the Main Module may request real time data from individual modules. The Main module will constantly receive data from remote modules and update its database, but will also be able to issue commands to turn the remote outlets on and off. Figure 3 summarizes the interactions that are necessary with the PLC connection.

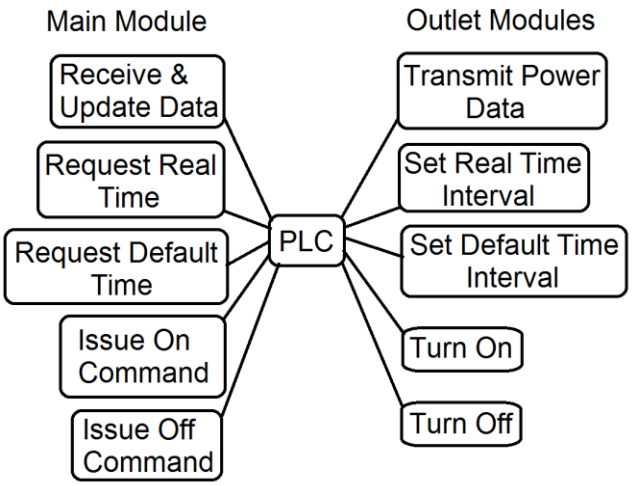

Figure 3. Commands & Updates Facilitated by PLC

As previously mentioned in equations 4 & 5, there are multiple formats that the power data may be transmitted in. If it is decided that the chosen assumptions are valid – or close to accurate – than the margins are close enough that it is probably worthwhile to select the 3 components power (Equation 5) for transmission, as it is a more data rich measurement, and can provide for unique features. However, this data will come preformatted by the microcontroller, and is not a concern of the PLC chip other than the data rates, which have already been considered in selection of the chip.

Receiving and transmitting data on the power line requires that the PLC be coupled with the mains wiring. There are two main coupling types under consideration, which will be chosen between based on the other choices in the design. Utilization of transformers will isolate the PLC while coupling it with the main wiring, and will be utilized if the microcontroller is isolated as well. If the microcontroller is not isolated, then the PLC will be coupled capacitively. Such couplings are already widely available in application notes for many of the discussed chips. Utilization of transformers throughout the design would isolate the design at the expense of space, but would help to protect the system from damage. However, if the microcontroller's supply is not isolated, than the space used at the transformer coupling of the PLC chip would be wasted as it would not be isolated anyways, which is why the selection is dependent on the microcontroller's coupling. For the Main Module, it is expected to be coupled with a transformer, as the data center should definitely be isolated and protected from the power line.

Ultimately, this high risk component was a further developed technology than originally thought. It is a mature technology with complete chips making it a relatively straight forward solution. While it is critical that the PLC system works, the utilization of all in one communication chips will hopefully mitigate any errors that might have been presented in constructing the communication manually otherwise. The utilization of the CY8CPLC10 chip (although not definitively selected) further helps to minimize risk. Although it has a relatively small data rate, it is of average size with an average number of pins, helping to ease concerns of chip space and routing difficulty within the outlet boxes. This helps ensure that the design will have the best chance of fitting within the standard outlet box. Deciding to transmit slowly with an optional real time update for select outlets (as discussed in the investigation section) is a huge

benefit as it greatly reduces the transmission requirements and makes the system more flexible in terms of the number of supportable outlets. Before considering such a solution, the number of outlets was severely limited, which would have made the project only a proof of concept at best. As there is no unique design involved in utilizing the PLC chip, there is no intellectual property discussed worth researching for protection.

Parts List

Digi-Key currently has 834 CY8CPLC10 chips available immediately for the price of $9.04 each (no predicted discount, $3.22 collective shipping). The parts associated with the PLC would also include transformers/capacitor coupling circuit modules based on the selected coupling method. For the purposes of the first prototype, only a few PLC chips would be purchased (~5), to first prove that it worked among the units.

Testing Strategy

As the Power Line Communication chip forms the lynchpin of the remotely connected system, it is vital that the chip is verified as early as possible. To do this, as early as possible, the chip should be decided on, purchased, and tested using minimal components. For example, a small microcontroller with I2C, the PLC chip, and the coupling equipment could be used to verify that chip is generating an appropriate output. Duplicating that setup would allow the user to send and receive single messages/packets across the wiring in a household, which would truly verify that the usage of the chip was entirely understood and verified. It is most critical in this step that the design by isolated (using a transformer) as it is the time most likely that the chips might be damaged. Isolation is also helpful here as it allows the inputs and outputs of the various chips to be measured with relative ease compared to the noise on a not isolated circuit. Finally, the unit can be built into a complete design with all control mechanisms, with a simple resistive load attached to “outlets”. A similar light could be attached to an alternate power measurement utility, and the data could be transmitted and compared. The setup could then be used to test remotely turning the outlet on and off. Altering the transmission rate of the chips would give the ability to test a more heavily loaded medium. I.E rather than each module only transmitting for $1/50^{th}$ of the time, each of 2 modules could be increased to transmit $20/50^{ths}$ of the time, which would simulate a heavily loaded circuit, and help indicate if the system is feasible for the target number of outlets.

Uncertainties

It remains uncertain as to what chip should be selected to provide PLC connectivity. Chip area and routing concerns still remain, in terms of fitting some of the more complex chips within a single gang outlet box. The coupling circuitry is unknown, but will likely be determined by the chosen coupling for the microcontroller.

Appendix

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Datasheets:

http://www.cypress.com/?docID=45757

http://www.cypress.com/?docID=50840

http://www.st.com/web/en/resource/technical/document/datasheet/CD00096923.pdf

http://www.st.com/web/en/resource/technical/document/datasheet/CD00274120.pdf

http://www.st.com/st-web-ui/static/active/en/resource/technical/document/datasheet/CD00294970.pdf

http://www.atmel.com/Images/doc43051H.pdf

http://www.nxp.com/documents/data_sheet/TDA5051A.pdf

Application Notes:

http://www.cypress.com/?docID=46702

http://www.st.com/web/en/resource/technical/document/application_note/CD00143379.pdf

http://www.st.com/web/en/resource/technical/document/application_note/CD00271738.pdf

http://www.st.com/st-web-ui/static/active/jp/resource/technical/document/application_note/DM00037363.pdf