Lab 3: Sequential Divider

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Introduction

For this lab, we had to construct and test a Sequential Divider for our Altera board. The goal of this assignment was to greater familiarize ourselves with the intricacies of VHDL, with special focus on synchronizing the computational tasks of a divider with a clock cycle.

Software and Tools

For this lab, we utilized ModelSim, Quartus Prime 17.0 and Altera DE2-115 Kit.

Design

In order to build a sequential functionality into the divider, we create a second architecture for the divider entity in such a way that it reuses one comparator unit to perform all division steps through multiple successive clock cycles.

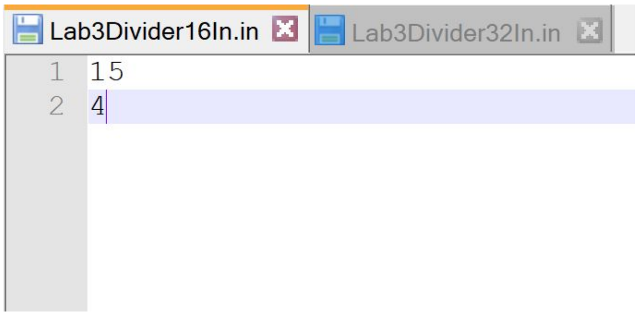
Procedure

1. First, a top level entity display_divider.vhd is created with the same name as the project.
2. A decoder.vhd package is created in order to use the leddcd.vhd code to decode the outputs to be displayed on the 7 segment LED display.
3. divider_const.vhd declares the lengths for all inputs and outputs to the divider and it can be changed at anytime to scale up or scale down the divider and the subsequent comparator.
4. divider.vhd describes the internal working of the divider passing the dividend and divisor to the comparator in order to carry out long division.
5. In order to simulate divider.vhd in ModelSim, we create two separate test benches that reads 16 and 32 bit inputs from .txt files (Lab3Divider16In.in and Lab3Divider32In.in) and stores the computed results in their respective .txt files (Lab3Divider16Out.out and Lab3Divider32Out.out).
6. In order to input real time values to both the operands and the operator, we expand the top level entity display_divider.vhd to include components divider.vhd, comparator.vhd and leddcd.vhd and then map the inputs from the board to obtain the outputs on the 7-segment LED display.

7. After which the inputs and outputs corresponding to the pins on the board are assigned, the code dumped onto the board.

Simulation

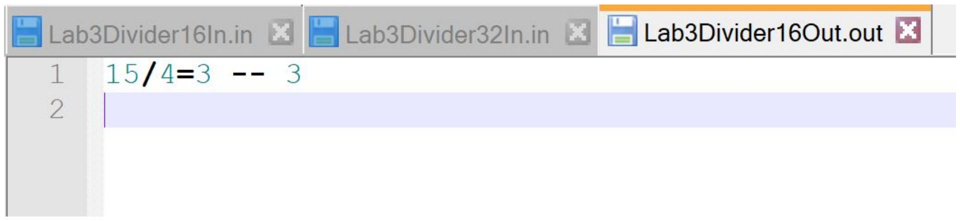
1. 16 bit input: The input file:



Lab3Divider16In.in | Lab3Divider32In.in

```
15
4
```

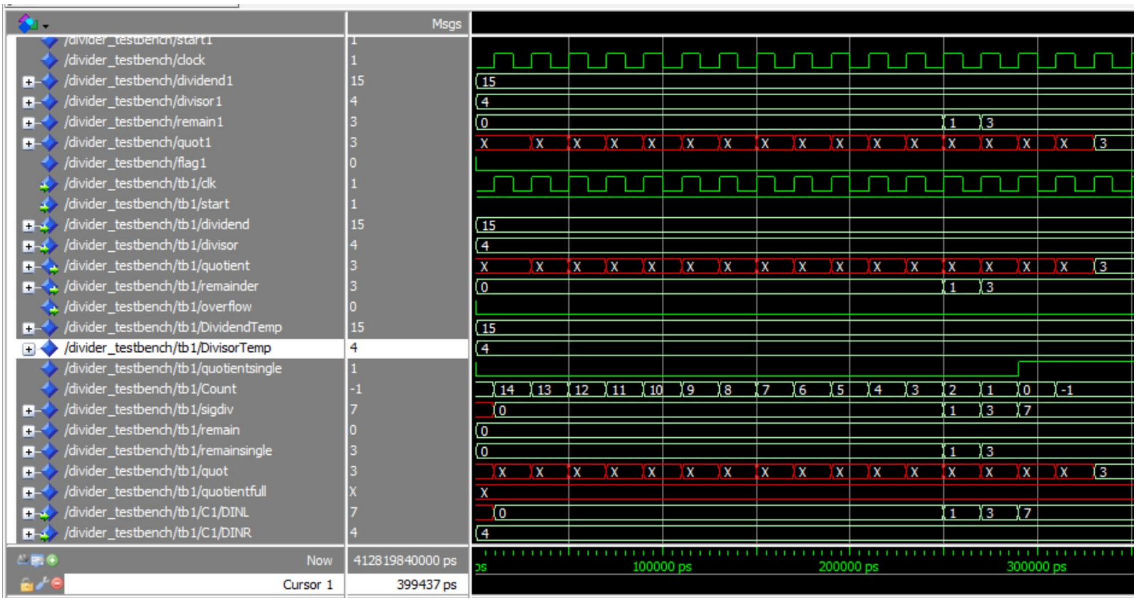
The output file:



Lab3Divider16In.in | Lab3Divider32In.in | Lab3Divider16Out.out

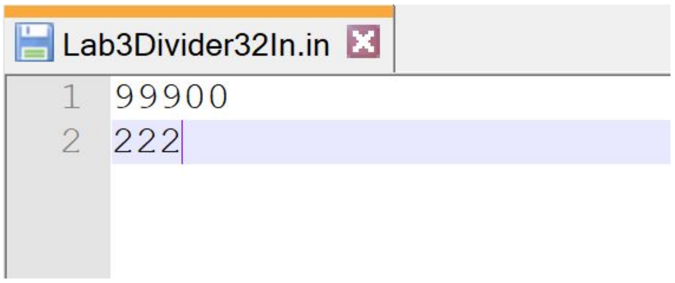
```
15/4=3 -- 3
```

The waveform:



	Msgs
/divider_testbench/start1	1
/divider_testbench/clock	1
/divider_testbench/dividend1	15
/divider_testbench/divisor1	4
/divider_testbench/remain1	3
/divider_testbench/quot1	3
/divider_testbench/flag1	0
/divider_testbench/tb1/clk	1
/divider_testbench/tb1/start	1
/divider_testbench/tb1/dividend	15
/divider_testbench/tb1/divisor	4
/divider_testbench/tb1/quotient	3
/divider_testbench/tb1/remainder	3
/divider_testbench/tb1/overflow	0
/divider_testbench/tb1/DividendTemp	15
/divider_testbench/tb1/DivisorTemp	4
/divider_testbench/tb1/quotientsingle	1
/divider_testbench/tb1/Count	-1
/divider_testbench/tb1/sigdiv	7
/divider_testbench/tb1/remain	0
/divider_testbench/tb1/remainsingle	3
/divider_testbench/tb1/quot	3
/divider_testbench/tb1/quotientfull	X
/divider_testbench/tb1/C1/DINL	7
/divider_testbench/tb1/C1/DINR	4
Now	412819840000 ps
Cursor 1	399437 ps

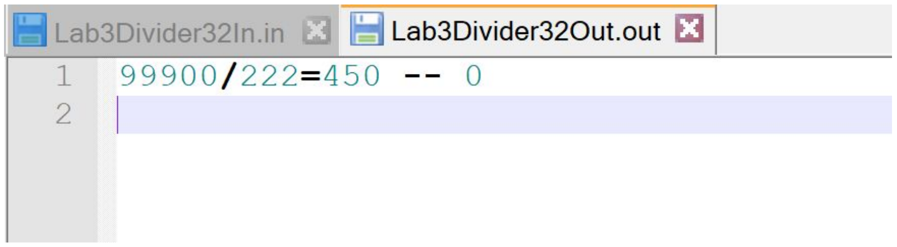
2. 32 bit input: The input file:



Lab3Divider32In.in

```
99900
222
```

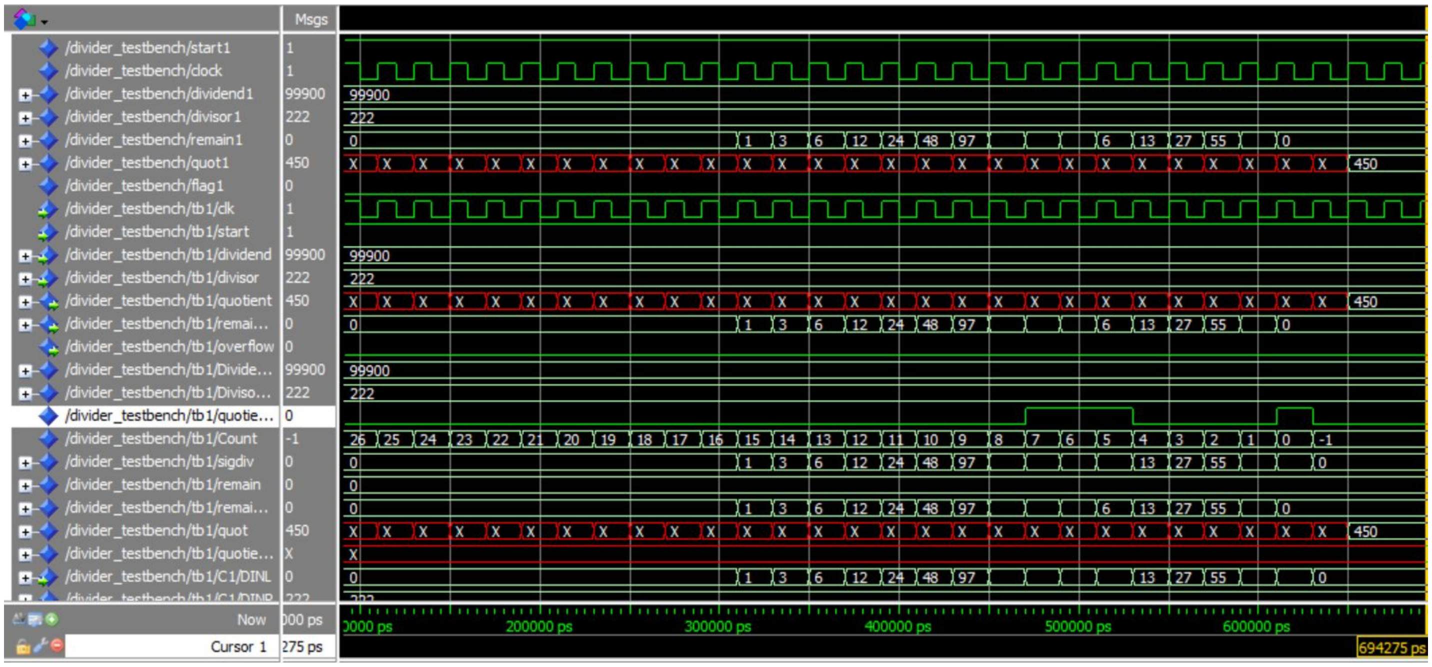
The output file:



Lab3Divider32In.in   Lab3Divider32Out.out

```
99900/222=450 -- 0
```

The waveform:



```
                                  Msgs
/divider_testbench/start1         1
/divider_testbench/clock          1
/divider_testbench/dividend1      99900
/divider_testbench/divisor1       222
/divider_testbench/remain1        0
/divider_testbench/quot1          450
/divider_testbench/flag1          0
/divider_testbench/tb1/clk        1
/divider_testbench/tb1/start      1
/divider_testbench/tb1/dividend   99900
/divider_testbench/tb1/divisor    222
/divider_testbench/tb1/quotient   450
/divider_testbench/tb1/remai...   0
/divider_testbench/tb1/overflow   0
/divider_testbench/tb1/Divide...  99900
/divider_testbench/tb1/Diviso...  222
/divider_testbench/tb1/quotie...  0
/divider_testbench/tb1/Count      -1
/divider_testbench/tb1/sigdiv     0
/divider_testbench/tb1/remain     0
/divider_testbench/tb1/remai...   0
/divider_testbench/tb1/quot       450
/divider_testbench/tb1/quotie...  X
/divider_testbench/tb1/C1/DINL    0
/divider_testbench/tb1/C1/DINR    222

Now      000 ps
Cursor 1 275 ps

0000 ps   200000 ps   300000 ps   400000 ps   500000 ps   600000 ps   694275 ps
```