Simulink Design Verifier Report

C:\Users\bpotter\OneDrive - MathWorks\DO_Project_18b\DO_03_Design\FCC\verification\design_error_detections\design_error\FCC_replacement.slx

bpotter

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Chapter 1. Summary

Analysis Information.

Model:	FCC
Replacement Model:	C:\Users\bpotter\OneDrive - MathWorks\DO_Project_18b\DO_03_Design\FCC\verification\design_error_detections\design_error\FCC_replacement.slx
Mode:	Design error detection
Status:	Exceeded time limit
Analysis Time:	301s

Objectives Status.

Number of Objectives:	**21**
Objectives Valid:	10
Objectives Falsified - Needs Simulation:	6
Objectives Undecided:	5

Chapter 2. Analysis Information

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Model Information

File:	FCC
Version:	1.53
Time Stamp:	Thu Oct 25 13:14:13 2018
Author:	bpotter

Analysis Options

Mode:	DesignErrorDetection
Detect integer overflow:	on
Detect division by zero:	on
Detect specified minimum and maximum value violations:	on
Detect out of bound array access:	on
Detect non-finite and NaN floating-point values:	off
Detect subnormal floating-point values:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	on

Constraints

Design Min Max Constraints

Name	Design Min Max Constraint
Act_Pos1	[-32768..32767]
Act_Pos2	[-32768..32767]
Act_Pos3	[-32768..32767]
Pilot_theta_cmd	[-32768..32767]
Pilot_phi_cmd	[-32768..32767]
Pilot_r_cmd	[-32768..32767]
AHRS1	[-180..180]
AHRS2	[-180..180]
AHRS3	[-180..180]

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

#	Type	Description
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic. Specifying minimum and maximum values that mimic environmental constraints on root-level Inport blocks may reduce instances of rational approximation.
2	Multi-instance Model reference approximation	The model being analyzed references at least one model more than once. Simulink Design Verifier copies referenced model contents into the replacement model before analysis so that coverage objectives for each instance of a model are treated separately. This differs from Model Coverage reporting that combines instances for coverage. Coverage results from simulating test cases may differ from analysis results.

Chapter 3. Design Error Detection Objectives Status

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Objectives Valid

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Design Range	RateTransition1	Design Range: [-0.1..0.1]	13	n/a
3	Design Range	RateTransition2	Design Range: [-0.1..0.1]	13	n/a
5	Design Range	RateTransition3	Design Range: [-0.1..0.1]	13	n/a
21	Division by zero	TypeConversion6	Division by zero	13	n/a
39	Division by zero	TypeConversion7	Division by zero	13	n/a
57	Division by zero	TypeConversion8	Division by zero	13	n/a
77	Integer overflow	Model2/Sum	Overflow	13	n/a
94	Design Range	Model1/Saturation	Design Range: [-30..30]	13	n/a
97	Design Range	Model1/Saturation1	Design Range: [-30..30]	13	n/a
100	Design Range	Model1/Saturation2	Design Range: [-30..30]	13	n/a

Objectives Falsified - Needs Simulation

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
9	Design Range	Scaling3	Design Range: [-0.1..0.1]	57	6 [10]

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
27	Design Range	Scaling4	Design Range: [-0.1..0.1]	57	5 [11]
45	Design Range	Scaling5	Design Range: [-0.1..0.1]	57	4 [12]
63	Design Range	Scaling	Design Range: [-30..30]	51	3 [12]
67	Design Range	Scaling1	Design Range: [-30..30]	48	2 [13]
71	Design Range	Scaling2	Design Range: [-15..15]	47	1 [14]

Objectives Undecided

Simulink Design Verifier was not able to process these objectives with the current options.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
22	Integer overflow	TypeConversion6	Overflow	-1	n/a
40	Integer overflow	TypeConversion7	Overflow	-1	n/a
58	Integer overflow	TypeConversion8	Overflow	-1	n/a
79	Design Range	Model2/MultiportSwitch	Design Range: [-180..180]	-1	n/a
102	Design Range	UnitDelay	Design Range: [-180..180]	-1	n/a

Chapter 4. Derived Ranges

Signal	Derived Ranges
RateTransition1- Outport 1	[-0.1..0.1]
RateTransition2- Outport 1	[-0.1..0.1]
RateTransition3- Outport 1	[-0.1..0.1]
Act_Pos1- Outport 1	[-32768..32767]
TypeConversion3- Outport 1	[-32768..32767]
Scaling3- Outport 1	[-0.1..0.1]
ActuatorControl1/Sum- Outport 1	[-0.2..0.2]
ActuatorControl1/Difference/UD- Outport 1	[-0.2..0.2]
ActuatorControl1/Difference/Diff- Outport 1	[-0.4..0.4]
ActuatorControl1/Gain- Outport 1	[-0.06..0.060001]
ActuatorControl1/Gain1- Outport 1	[-0.0080001..0.0080001]
ActuatorControl1/Gain2- Outport 1	[-0.024..0.024]
ActuatorControl1/Integrator- Outport 1	[-0.1..0.1]
ActuatorControl1/Sum1- Outport 1	[-0.164..0.168]
ActuatorControl1/Saturation- Outport 1	[-0.164..0.168]
Scaling6- Outport 1	[-53738..55049]
TypeConversion6- Outport 1	[-32768..32767]
Actuator1- Outport 1	[-32768..32767]
Act_Pos2- Outport 1	[-32768..32767]
TypeConversion4- Outport 1	[-32768..32767]
Scaling4- Outport 1	[-0.1..0.1]
ActuatorControl2/Sum- Outport 1	[-0.2..0.2]
ActuatorControl2/Difference/UD- Outport 1	[-0.2..0.2]
ActuatorControl2/Difference/Diff- Outport 1	[-0.4..0.4]
ActuatorControl2/Gain- Outport 1	[-0.06..0.060001]
ActuatorControl2/Gain1- Outport 1	[-0.0080001..0.0080001]
ActuatorControl2/Gain2- Outport 1	[-0.024..0.024]
ActuatorControl2/Integrator- Outport 1	[-0.1..0.1]
ActuatorControl2/Sum1- Outport 1	[-0.164..0.168]
ActuatorControl2/Saturation- Outport 1	[-0.164..0.168]
Scaling7- Outport 1	[-53738..55049]
TypeConversion7- Outport 1	[-32768..32767]
Actuator2- Outport 1	[-32768..32767]
Act_Pos3- Outport 1	[-32768..32767]
TypeConversion5- Outport 1	[-32768..32767]
Scaling5- Outport 1	[-0.1..0.1]

Signal	Derived Ranges
ActuatorControl3/Sum- Outport 1	[-0.2..0.2]
ActuatorControl3/Difference/UD- Outport 1	[-0.2..0.2]
ActuatorControl3/Difference/Diff- Outport 1	[-0.4..0.4]
ActuatorControl3/Gain- Outport 1	[-0.06..0.060001]
ActuatorControl3/Gain1- Outport 1	[-0.0080001..0.0080001]
ActuatorControl3/Gain2- Outport 1	[-0.024..0.024]
ActuatorControl3/Integrator- Outport 1	[-0.1..0.1]
ActuatorControl3/Sum1- Outport 1	[-0.168..0.168]
ActuatorControl3/Saturation- Outport 1	[-0.168..0.168]
Scaling8- Outport 1	[-55049..55049]
TypeConversion8- Outport 1	[-32768..32767]
Actuator3- Outport 1	[-32768..32767]
Pilot_theta_cmd- Outport 1	[-32768..32767]
TypeConversion- Outport 1	[-32768..32767]
Scaling- Outport 1	[-30.001..30]
Pilot_phi_cmd- Outport 1	[-32768..32767]
TypeConversion1- Outport 1	[-32768..32767]
Scaling1- Outport 1	[-30.001..30]
Pilot_r_cmd- Outport 1	[-32768..32767]
TypeConversion2- Outport 1	[-32768..32767]
Scaling2- Outport 1	[-15..15]
Model2/Constant- Outport 1	0
AHRS1_Valid- Outport 1	[F..T]
AHRS2_Valid- Outport 1	[F..T]
AHRS3_Valid- Outport 1	[F..T]
Model2/Sum- Outport 1	[0..3]
Model2/MultiportSwitch- Outport 1	[-540..540]
Model1/Sum- Outport 1	[-570..570]
Model1/Gain- Outport 1	[-758.1..758.1]
Model1/Sum1- Outport 1	[-570..570]
Model1/Gain1- Outport 1	[-49.02..49.02]
Model1/Gain2- Outport 1	[-1282.5..1282.5]
Model1/Gain3- Outport 1	[-678.3..678.3]
Model1/Sum2- Outport 1	[-555..555]
Model1/Gain4- Outport 1	[-73.815..73.815]
Model1/Gain5- Outport 1	[-1293.2..1293.2]
Model1/Integrator- Outport 1	[-10..10]
Model1/Integrator1- Outport 1	[-10..10]

Signal	Derived Ranges
Model1/Integrator2- Outport 1	[-10..10]
Model1/Sum3- Outport 1	[-768.1..768.1]
Model1/Saturation- Outport 1	[-30..30]
Model1/Sum4- Outport 1	[-59.02..59.02]
Model1/Saturation1- Outport 1	[-30..30]
Model1/Sum5- Outport 1	[-83.815..83.815]
Model1/Saturation2- Outport 1	[-30..30]
UnitDelay- Outport 1	[-540..540]
Model/SOF- Outport 1	[-1937.1..1937.1]
Model/Sum5- Outport 1	[-1967.1..1967.1]
Model/RollOff1/s_1- Outport 1	[-331.27..331.27]
Model/RollOff1/UnitDelay- Outport 1	[-Inf..Inf]
Model/RollOff1/a_2_1- Outport 1	[-Inf..Inf]
Model/RollOff1/SumA21- Outport 1	[-Inf..Inf]
Model/Sum4- Outport 1	[-811.55..811.55]
Model/RollOff2/s_1- Outport 1	[-136.67..136.67]
Model/RollOff2/UnitDelay- Outport 1	[-Inf..Inf]
Model/RollOff2/a_2_1- Outport 1	[-Inf..Inf]
Model/RollOff2/SumA21- Outport 1	[-Inf..Inf]
Model/Sum6- Outport 1	[-1200.8..1200.8]
Model/RollOff3/s_1- Outport 1	[-202.23..202.23]
Model/RollOff3/UnitDelay- Outport 1	[-Inf..Inf]
Model/RollOff3/a_2_1- Outport 1	[-Inf..Inf]
Model/RollOff3/SumA21- Outport 1	[-Inf..Inf]
Model/Saturation- Outport 1	[-0.1..0.1]
AHRS1- Outport 1	[-180..180]
AHRS2- Outport 1	[-180..180]
Model2/Mid_Value/MinMax- Outport 1	[-180..180]
AHRS3- Outport 1	[-180..180]
Model2/Mid_Value/MinMax1- Outport 1	[-180..180]
Model2/Mid_Value/MinMax2- Outport 1	[-180..180]
Model2/Mid_Value/MinMax3- Outport 1	[-180..180]
Model2/Avg_Value/Constant- Outport 1	0
Model2/Avg_Value/Switch- Outport 1	[-180..180]
Model2/Avg_Value/Switch1- Outport 1	[-180..180]
Model2/Avg_Value/Switch2- Outport 1	[-180..180]
Model2/Avg_Value/Sum- Outport 1	[-540..540]
Model2/Avg_Value/Gain- Outport 1	[-270..270]

Signal	Derived Ranges
Model2/Single_Value/Constant- Outport 1	0
Model2/Single_Value/Switch- Outport 1	[-180..180]
Model2/Single_Value/Switch1- Outport 1	[-180..180]
Model2/Single_Value/Switch2- Outport 1	[-180..180]
Model2/Single_Value/Sum- Outport 1	[-540..540]

Chapter 5. Design Errors

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Scaling3

Summary.

Model Item:	Scaling3
Type:	Design Range: [-0.1..0.1]
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
Act_Pos1	-32768
Act_Pos2	0
Act_Pos3	0
Pilot_theta_cmd	0
Pilot_phi_cmd	0
Pilot_r_cmd	0
AHRS1	[-180 -180 -180 -180 -180]
AHRS2	[-180 -180 -180 -180 -180]
AHRS3	[-180 -180 -180 -180 -180]
AHRS1_Valid	0
AHRS2_Valid	0
AHRS3_Valid	0

TypeConversion6

Summary.

Model Item:	TypeConversion6
Type:	Overflow
Status:	Undecided

Scaling4

Summary.

Model Item:	Scaling4
Type:	Design Range: [-0.1..0.1]
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
Act_Pos1	0
Act_Pos2	-32768
Act_Pos3	0
Pilot_theta_cmd	0
Pilot_phi_cmd	0
Pilot_r_cmd	0
AHRS1	[-180 -180 -180 -180 -180]
AHRS2	[-180 -180 -180 -180 -180]
AHRS3	[-180 -180 -180 -180 -180]
AHRS1_Valid	0
AHRS2_Valid	0
AHRS3_Valid	0

TypeConversion7

Summary.

Model Item:	TypeConversion7
Type:	Overflow
Status:	Undecided

Scaling5

Summary.

Model Item:	Scaling5
Type:	Design Range: [-0.1..0.1]
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
Act_Pos1	0
Act_Pos2	0
Act_Pos3	-32768
Pilot_theta_cmd	0
Pilot_phi_cmd	0
Pilot_r_cmd	0
AHRS1	[-180 -180 -180 -180 -180]
AHRS2	[-180 -180 -180 -180 -180]
AHRS3	[-180 -180 -180 -180 -180]
AHRS1_Valid	0
AHRS2_Valid	0
AHRS3_Valid	0

TypeConversion8

Summary.

Model Item:	TypeConversion8
Type:	Overflow
Status:	Undecided

Scaling

Summary.

Model Item:	Scaling
Type:	Design Range: [-30..30]
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
Act_Pos1	0
Act_Pos2	0
Act_Pos3	0
Pilot_theta_cmd	-32768
Pilot_phi_cmd	0
Pilot_r_cmd	0
AHRS1	[-180 -180 -180 -180 -180]
AHRS2	[-180 -180 -180 -180 -180]
AHRS3	[-180 -180 -180 -180 -180]
AHRS1_Valid	0
AHRS2_Valid	0
AHRS3_Valid	0

Scaling1

Summary.

Model Item:	Scaling1
Type:	Design Range: [-30..30]
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
Act_Pos1	0
Act_Pos2	0
Act_Pos3	0
Pilot_theta_cmd	0
Pilot_phi_cmd	-32768
Pilot_r_cmd	0
AHRS1	[-180 -180 -180 -180 -180]
AHRS2	[-180 -180 -180 -180 -180]
AHRS3	[-180 -180 -180 -180 -180]
AHRS1_Valid	0
AHRS2_Valid	0
AHRS3_Valid	0

Scaling2

Summary.

Model Item:	Scaling2
Type:	Design Range: [-15..15]
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
Act_Pos1	0
Act_Pos2	0
Act_Pos3	0
Pilot_theta_cmd	0
Pilot_phi_cmd	0
Pilot_r_cmd	-32768
AHRS1	[-180 -180 -180 -180 -180]
AHRS2	[-180 -180 -180 -180 -180]
AHRS3	[-180 -180 -180 -180 -180]
AHRS1_Valid	0
AHRS2_Valid	0
AHRS3_Valid	0

Model2/MultiportSwitch

Summary.

Model Item:	Model2/MultiportSwitch
Type:	Design Range: [-180..180]
Status:	Undecided

UnitDelay

Summary.

Model Item:	UnitDelay
Type:	Design Range: [-180..180]
Status:	Undecided