

# **DisplayModel\_Step5\_start**

## **Design Description**

**hualongy**

## DisplayModel\_Step5\_start: Design Description

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# Chapter 1. Model Version

**Version:** 1.78

**Last modified:** Sun Sep 08 12:12:55 2013

**Checksum:** 3991650596 4187630608 1660554039 3505155770

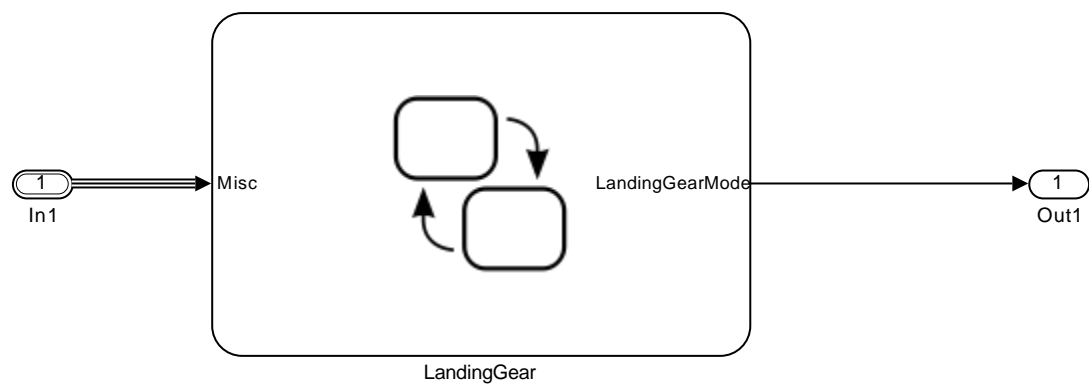
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# Chapter 2. Root System

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**Figure 2.1. DisplayModel\_Step5\_start**



## 2.1. Interface

### 2.1.1. Input Signals

**Table 2.1.**

Description:  
Data Type: MiscData  
Width: 1  
Dimensions: [1 1]

### 2.1.2. Output Signals

**Table 2.2.**

Description:

Data Type: double

Width: 1

Dimensions: [1 1]

## 2.2. Blocks

### 2.2.1. Parameters

#### 2.2.1.1. "In1" (Inport)

**Table 2.3. "In1" Parameters**

Parameter	Value
Port number	1
Port dimensions (-1 for inherited)	-1
Sample time (-1 for inherited)	-1
Minimum	[]
Maximum	[]
Data type	Bus: MiscData

#### 2.2.1.2. "Out1" (Outport)

**Table 2.4. "Out1" Parameters**

Parameter	Value
Port number	1
Icon display	Port number
Minimum	[]
Maximum	[]
Data type	Inherit: auto
Lock output data type setting against changes by the fixed-point tools	off
Output as nonvirtual bus in parent model	off
Port dimensions (-1 for inherited)	-1
Variable-size signal	Inherit
Sample time (-1 for inherited)	-1



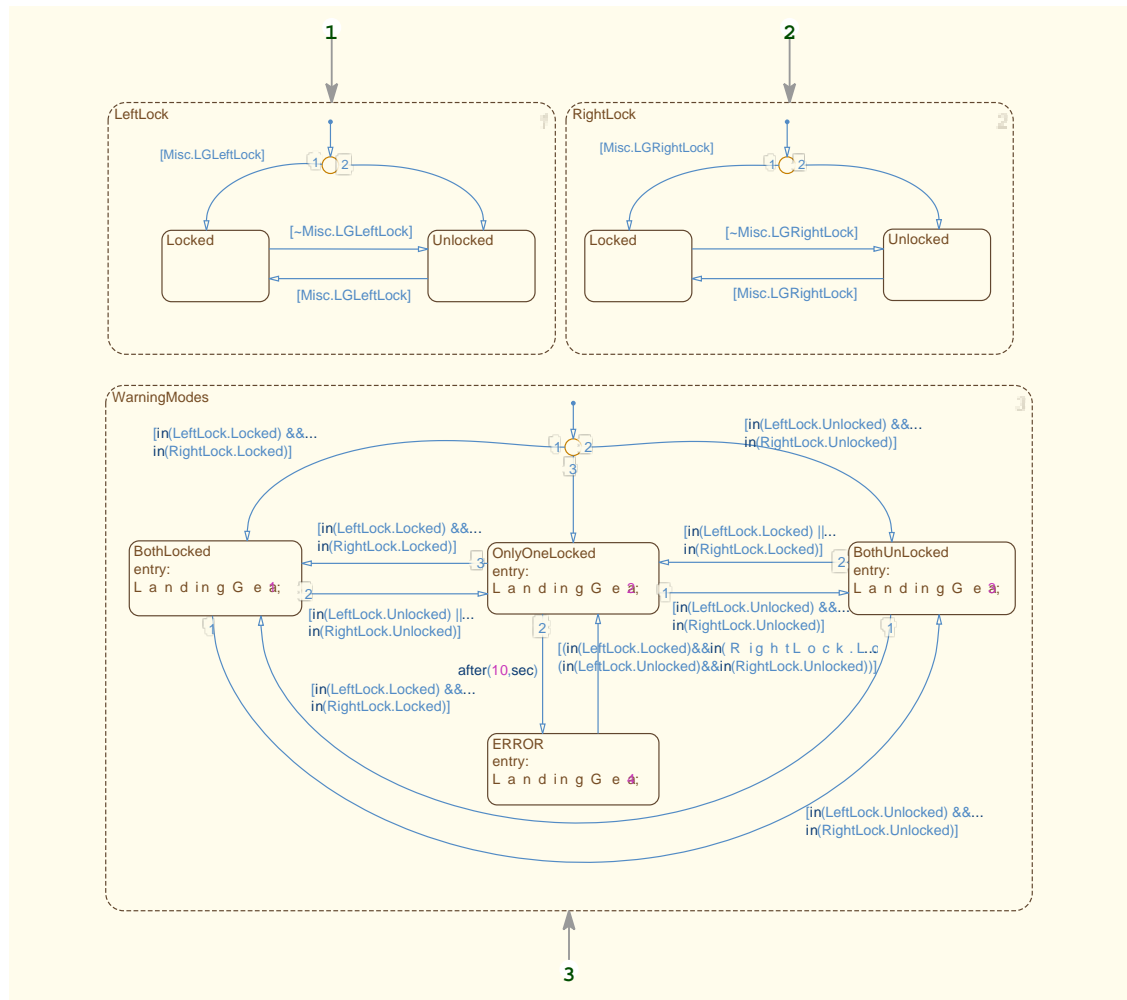
Parameter	Value
Source of initial output value	Dialog
Output when disabled	held
Initial output	[]

## 2.2.2. Block Execution Order

1. BusConversion\_InsertedFor\_In1\_at\_output\_0\_BusSelector\_1 (BusSelector)
2. BusConversion\_InsertedFor\_LandingGear\_at\_inport\_0\_BusCreator\_1 (BusCreator)
3. *LandingGear*
4. Out1 [3] (Output)

## 2.3. State Charts

### 2.3.1. Chart

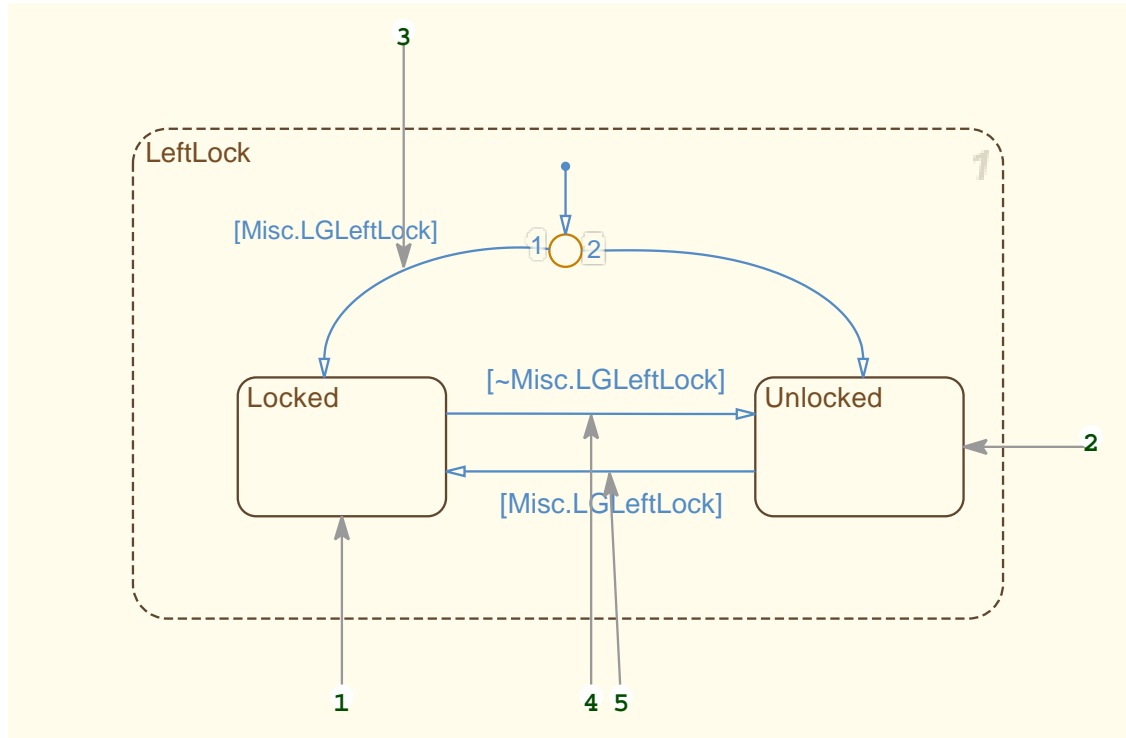


- ❶ LeftLock [5]
- ❷ RightLock [6]

③ WarningModes [7]

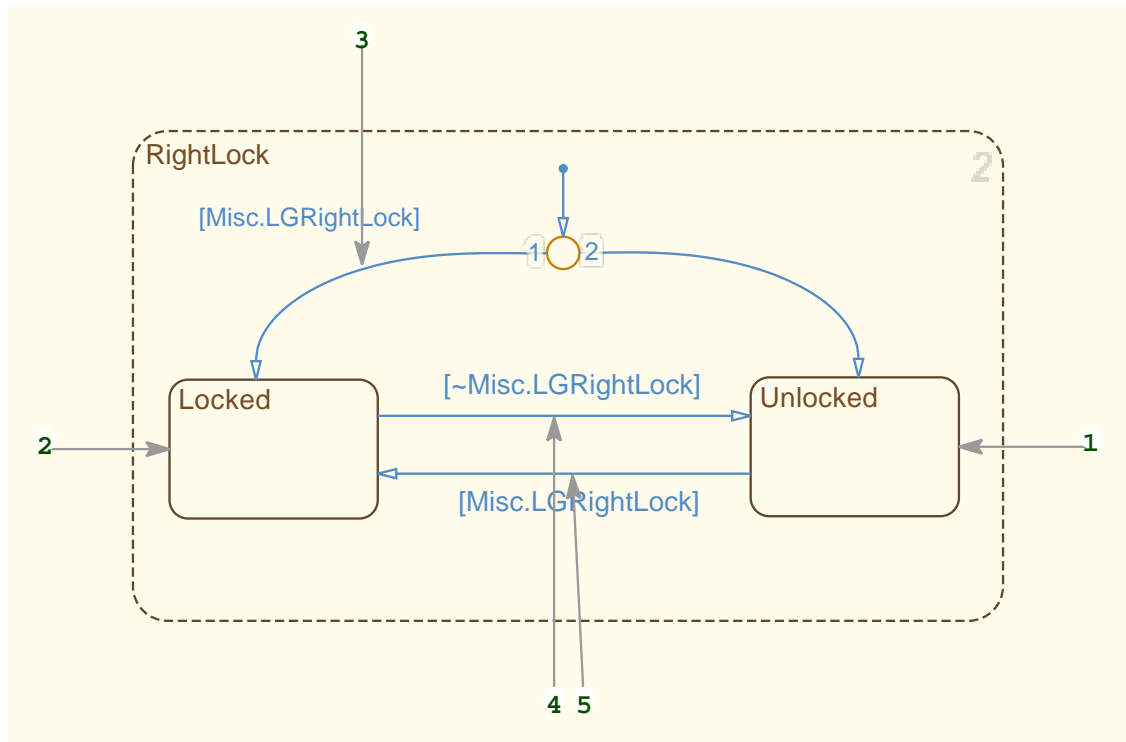
## 2.3.2. States

### 2.3.2.1. AND State - LeftLock



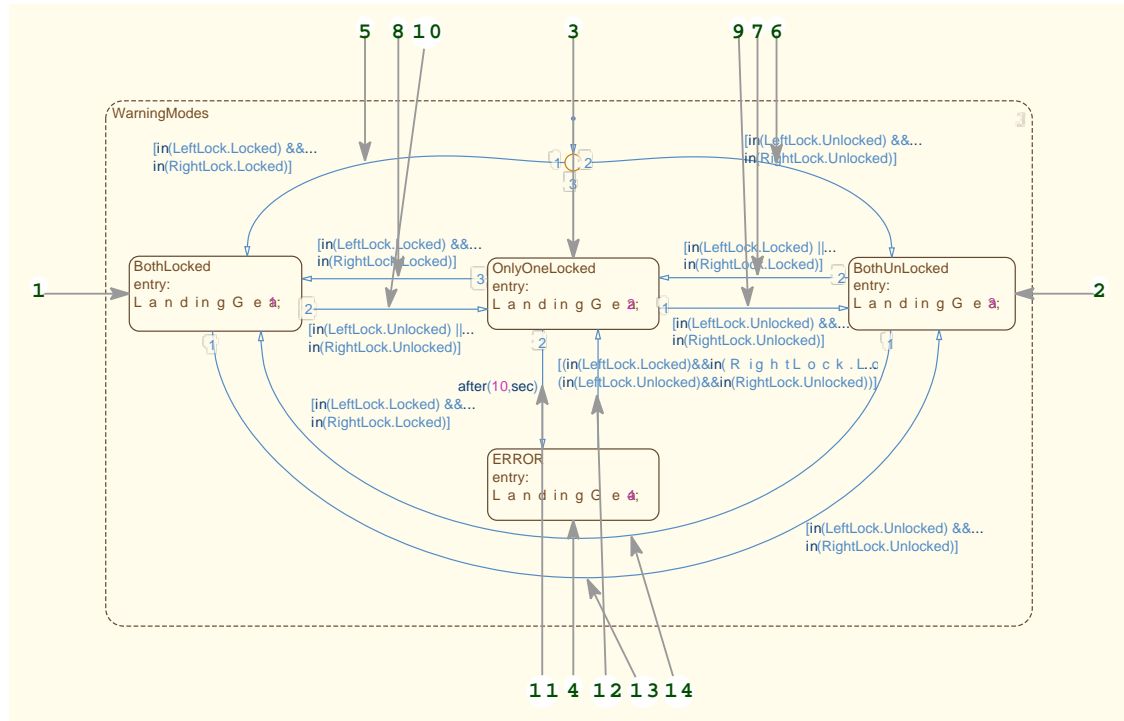
- ① Locked [7]
- ② Unlocked [8]
- ③ [Misc.LGLeftLock]
- ④ [~Misc.LGLeftLock]
- ⑤ [Misc.LGLeftLock]

### 2.3.2.2. AND State - RightLock



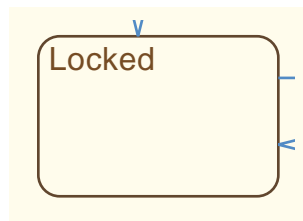
- ❶ Unlocked [8]
- ❷ Locked [8]
- ❸ [Misc.LGRightLock]
- ❹ [~Misc.LGRightLock]
- ❺ [Misc.LGRightLock]

### 2.3.2.3. AND State - WarningModes

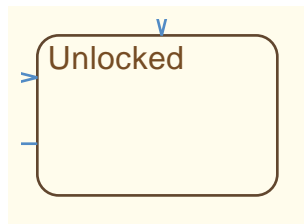


- ① BothLocked [8]
- ② BothUnLocked [8]
- ③ OnlyOneLocked [9]
- ④ ERROR [9]
- ⑤  $[(in(LeftLock.Locked) \&\&... in(RightLock.Locked))]$
- ⑥  $[(in(LeftLock.Unlocked) \&\&... in(RightLock.Unlocked))]$
- ⑦  $[(in(LeftLock.Locked) \&\&... in(RightLock.Unlocked))]$
- ⑧  $[(in(LeftLock.Locked) \&\&... in(RightLock.Locked))]$
- ⑨  $[(in(LeftLock.Unlocked) \&\&... in(RightLock.Unlocked))]$
- ⑩  $[(in(LeftLock.Unlocked) \&\&... in(RightLock.Unlocked))]$
- ⑪  $after(10,sec)$
- ⑫  $[(in(LeftLock.Locked) \&\&... in(RightLock.Locked))]$
- ⑬  $[(in(LeftLock.Unlocked) \&\&... in(RightLock.Unlocked))]$
- ⑭  $[(in(LeftLock.Locked) \&\&... in(RightLock.Unlocked))]$

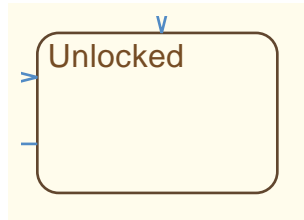
### 2.3.2.4. OR State - Locked



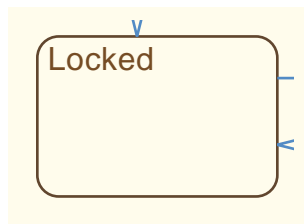
### 2.3.2.5. OR State - Unlocked



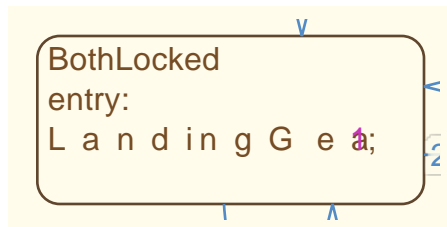
### 2.3.2.6. OR State - Unlocked



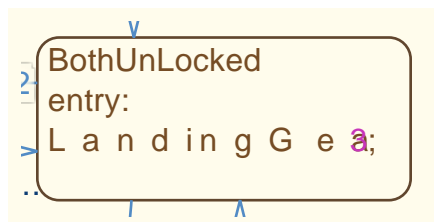
### 2.3.2.7. OR State - Locked



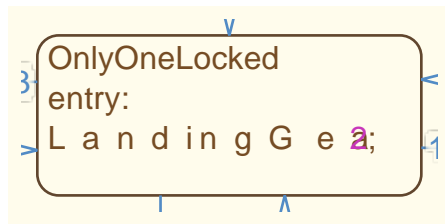
### 2.3.2.8. OR State - BothLocked



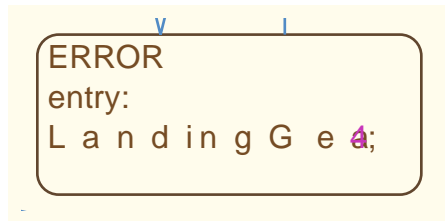
### 2.3.2.9. OR State - BothUnLocked



### 2.3.2.10. OR State - OnlyOneLocked



### 2.3.2.11. OR State - ERROR



## 2.3.3. Data

**Table 2.5. Data - LandingGearMode**

Scope	Output
-------	--------

**Table 2.6. Data - Misc**

Scope	Input
Data Type	Bus: MiscData

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# Chapter 3. System Design Variables

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## 3.1. Design Variable Details

**Table 3.1. MiscData**

Property	Value
Alignment	-1
Elements	[MiscData.Elements(1) [10], MiscData.Elements(2) [10], MiscData.Elements(3) [11], MiscData.Elements(4) [11], MiscData.Elements(5) [12], MiscData.Elements(6) [12]]
Description	
DataScope	Auto
HeaderFile	

**Table 3.2. MiscData.Elements [10](1)**

Property	Value
Min	
Max	
DimensionsMode	Fixed
SamplingMode	Sample based
SampleTime	-1
Description	
DocUnits	
Name	FlapPosition
DataType	double
Complexity	real
Dimensions	1

**Table 3.3. MiscData.Elements [10](2)**

Property	Value
Min	

Max	
DimensionsMode	Fixed
SamplingMode	Sample based
SampleTime	-1
Description	
DocUnits	
Name	CabinPressure
DataType	double
Complexity	real
Dimensions	1

**Table 3.4. MiscData.Elements [10](3)**

Property	Value
Min	
Max	
DimensionsMode	Fixed
SamplingMode	Sample based
SampleTime	-1
Description	
DocUnits	
Name	HydraulicPressure
DataType	double
Complexity	real
Dimensions	1

**Table 3.5. MiscData.Elements [10](4)**

Property	Value
Min	
Max	
DimensionsMode	Fixed
SamplingMode	Sample based
SampleTime	-1
Description	
DocUnits	
Name	APUData
DataType	double



Complexity	real
Dimensions	1

**Table 3.6. MiscData.Elements [10](5)**

Property	Value
Min	
Max	
DimensionsMode	Fixed
SamplingMode	Sample based
SampleTime	-1
Description	
DocUnits	
Name	LGLeftLock
DataType	boolean
Complexity	real
Dimensions	1

**Table 3.7. MiscData.Elements [10](6)**

Property	Value
Min	
Max	
DimensionsMode	Fixed
SamplingMode	Sample based
SampleTime	-1
Description	
DocUnits	
Name	LGRightLock
DataType	boolean
Complexity	real
Dimensions	1

**Used by Blocks:**

- DisplayModel\_Step5\_start/In1 [3]
- DisplayModel\_Step5\_start/LandingGear [3]

Workspace: Base

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# Chapter 4. Requirements Traceability

DisplayModel\_Step5\_start does not contain requirements traceability links.

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# Chapter 5. System Model Configuration

**Table 5.1. DisplayModel\_Step5\_start Configuration Set**

Property	Value
Description	
Components	[DisplayModel_Step5_start Configuration Set.Components(1) [14], DisplayModel_Step5_start Configuration Set.Components(2) [15], DisplayModel_Step5_start Configuration Set.Components(3) [16], DisplayModel_Step5_start Configuration Set.Components(4) [17], DisplayModel_Step5_start Configuration Set.Components(5) [19], DisplayModel_Step5_start Configuration Set.Components(6) [21], DisplayModel_Step5_start Configuration Set.Components(7) [21], DisplayModel_Step5_start Configuration Set.Components(8) [22], DisplayModel_Step5_start Configuration Set.Components(9) [24], DisplayModel_Step5_start Configuration Set.Components(10) [24]]
Name	Configuration
SimulationMode	normal

**Table 5.2. DisplayModel\_Step5\_start Configuration Set.Components [14](1)**

Property	Value
Name	Solver
Description	
Components	
StartTime	0.0
StopTime	10.0
AbsTol	auto
FixedStep	0.2
InitialStep	auto
MaxNumMinSteps	-1
MaxOrder	5
ZcThreshold	auto
ConsecutiveZCsStepRelTol	10*128*eps
MaxConsecutiveZCs	1000
ExtrapolationOrder	4
NumberNewtonIterations	1
MaxStep	auto
MinStep	auto

MaxConsecutiveMinStep	1
RelTol	1e-3
SolverMode	Auto
EnableConcurrentExecution	off
ConcurrentTasks	off
Solver	FixedStepDiscrete
SolverName	FixedStepDiscrete
SolverType	Fixed-step
SolverJacobianMethodControl	auto
ShapePreserveControl	DisableAll
ZeroCrossControl	UseLocalSettings
ZeroCrossAlgorithm	Nonadaptive
SolverResetMethod	Fast
PositivePriorityOrder	off
AutoInsertRateTranBlk	off
SampleTimeConstraint	Unconstrained
InsertRTBMode	Whenever possible
SampleTimeProperty	

**Table 5.3. DisplayModel\_Step5\_start Configuration Set.Components [14](2)**

Property	Value
Name	Data Import/Export
Description	
Components	
Decimation	1
ExternalInput	[t, u]
FinalStateName	xFinal
InitialState	xInitial
LimitDataPoints	on
MaxDataPoints	1000
LoadExternalInput	off
LoadInitialState	off
SaveFinalState	off
SaveCompleteFinalSimState	off
SaveFormat	Array
SignalLoggingSaveFormat	Dataset
SaveOutput	on
SaveState	off
SignalLogging	on

DSMLogging	on
InspectSignalLogs	off
SaveTime	on
ReturnWorkspaceOutputs	off
StateSaveName	xout
TimeSaveName	tout
OutputSaveName	yout
SignalLoggingName	logsout
DSMLoggingName	dsmout
OutputOption	RefineOutputTimes
OutputTimes	[]
ReturnWorkspaceOutputsName	out
Refine	1

**Table 5.4. DisplayModel\_Step5\_start Configuration Set.Components [14](3)**

Property	Value
Name	Optimization
Description	
Components	
BlockReduction	on
BooleanDataType	on
ConditionallyExecuteInputs	on
InlineParams	on
UseIntDivNetSlope	off
UseFloatMulNetSlope	off
DefaultUnderspecifiedDataType	double
UseSpecifiedMinMax	off
InlineInvariantSignals	off
OptimizeBlockIOStorage	on
BufferReuse	on
EnhancedBackFolding	off
StrengthReduction	off
AdvancedOptControl	
EnforceIntegerDowncast	on
ExpressionFolding	on
BooleansAsBitfields	off
BitfieldContainerType	uint_T
EnableMemcpy	on
MemcpyThreshold	64

PassReuseOutputArgsAs	Structure reference
PassReuseOutputArgsThreshold	12
FoldNonRolledExpr	on
LocalBlockOutputs	on
RollThreshold	5
SystemCodeInlineAuto	off
StateBitsets	off
DataBitsets	off
ActiveStateOutputEnumStorageType	Native Integer
UseTempVars	off
ZeroExternalMemoryAtStartup	on
ZeroInternalMemoryAtStartup	on
InitFltsAndDblsToZero	off
NoFixptDivByZeroProtection	off
EfficientFloat2IntCast	off
EfficientMapNaN2IntZero	on
OptimizeModelRefInitCode	on
LifeSpan	1
EvaledLifeSpan	1
MaxStackSize	Inherit from target
BufferReusableBoundary	on
SimCompilerOptimization	Off
AccelVerboseBuild	off
ParallelExecutionInRapidAccelerator	on

**Table 5.5. DisplayModel\_Step5\_start Configuration Set.Components [14](4)**

Property	Value
Name	Diagnostics
Description	
Components	
RTPrefix	error
ConsistencyChecking	none
ArrayBoundsChecking	none
SignalInfNanChecking	none
SignalRangeChecking	none
ReadBeforeWriteMsg	UseLocalSettings
WriteAfterWriteMsg	UseLocalSettings
WriteAfterReadMsg	UseLocalSettings
AlgebraicLoopMsg	warning

ArtificialAlgebraicLoopMsg	warning
SaveWithDisabledLinksMsg	warning
SaveWithParameterizedLinksMsg	warning
CheckSSInitialOutputMsg	on
UnderspecifiedInitializationDetection	Classic
MergeDetectMultiDrivingBlocksExec	none
CheckExecutionContextPreStartOutputMsg	off
CheckExecutionContextRuntimeOutputMsg	off
SignalResolutionControl	UseLocalSettings
BlockPriorityViolationMsg	warning
MinStepSizeMsg	warning
TimeAdjustmentMsg	none
MaxConsecutiveZCsMsg	error
MaskedZcDiagnostic	warning
IgnoredZcDiagnostic	warning
SolverPrmCheckMsg	warning
InheritedTsInSrcMsg	warning
DiscreteInheritContinuousMsg	warning
MultiTaskDSMMsg	error
MultiTaskCondExecSysMsg	error
MultiTaskRateTransMsg	error
SingleTaskRateTransMsg	none
TasksWithSamePriorityMsg	warning
SigSpecEnsureSampleTimeMsg	warning
CheckMatrixSingularityMsg	none
IntegerOverflowMsg	warning
Int32ToFloatConvMsg	warning
ParameterDowncastMsg	error
ParameterOverflowMsg	error
ParameterUnderflowMsg	none
ParameterPrecisionLossMsg	warning
ParameterTunabilityLossMsg	warning
FixptConstUnderflowMsg	none
FixptConstOverflowMsg	none
FixptConstPrecisionLossMsg	none
UnderSpecifiedDataTypeMsg	none
UnnecessaryDatatypeConvMsg	none
VectorMatrixConversionMsg	none
InvalidFcnCallConnMsg	error

FcnCallInpInsideContextMsg	EnableAllAsError
SignalLabelMismatchMsg	none
UnconnectedInputMsg	warning
UnconnectedOutputMsg	warning
UnconnectedLineMsg	warning
SFCnCompatibilityMsg	none
FrameProcessingCompatibilityMsg	warning
UniqueDataStoreMsg	none
BusObjectLabelMismatch	warning
RootOutportRequireBusObject	warning
AssertControl	UseLocalSettings
Echo	
EnableOverflowDetection	off
ModelReferenceIOMsg	none
ModelReferenceVersionMismatchMessage	none
ModelReferenceIOMismatchMessage	none
ModelReferenceCSMismatchMessage	none
ModelReferenceSimTargetVerbose	off
UnknownTsInhSupMsg	warning
ModelReferenceDataLoggingMessage	warning
ModelReferenceSymbolNameMessage	warning
ModelReferenceExtraNoncontSigs	error
StateNameClashWarn	warning
SimStateInterfaceChecksumMismatchMsg	warning
SimStateOlderReleaseMsg	error
InitInArrayFormatMsg	warning
StrictBusMsg	ErrorLevel1
BusNameAdapt	WarnAndRepair
NonBusSignalsTreatedAsBus	none
LoggingUnavailableSignals	error
SFUnusedDataAndEventsDiag	warning
SFUnexpectedBacktrackingDiag	warning
SFInvalidInputDataAccessInChartInitDiag	warning
SFNoUnconditionalDefaultTransitionDiag	warning
SFTransitionOutsideNaturalParentDiag	warning
SFUnconditionalTransitionShadowingDiag	warning
SFUndirectedBroadcastEventsDiag	warning
SFTransitionActionBeforeConditionDiag	warning



**Table 5.6. DisplayModel\_Step5\_start Configuration Set.Components [14](5)**

Property	Value
Name	Hardware Implementation
Description	
Components	
ProdBitPerChar	8
ProdBitPerShort	16
ProdBitPerInt	32
ProdBitPerLong	32
ProdBitPerLongLong	64
ProdBitPerFloat	32
ProdBitPerDouble	64
ProdBitPerPointer	32
ProdLargestAtomicInteger	Char
ProdLargestAtomicFloat	None
ProdIntDivRoundTo	Undefined
ProdEndianess	Unspecified
ProdWordSize	32
ProdShiftRightIntArith	on
ProdLongLongMode	off
ProdHWDeviceType	32-bit Generic
TargetBitPerChar	8
TargetBitPerShort	16
TargetBitPerInt	32
TargetBitPerLong	32
TargetBitPerLongLong	64
TargetBitPerFloat	32
TargetBitPerDouble	64
TargetBitPerPointer	32
TargetLargestAtomicInteger	Char
TargetLargestAtomicFloat	None
TargetShiftRightIntArith	on
TargetLongLongMode	off
TargetIntDivRoundTo	Undefined
TargetEndianess	Unspecified
TargetWordSize	32
TargetTypeEmulationWarnSuppressLevel	0
TargetPreprocMaxBitsSint	32
TargetPreprocMaxBitsUint	32

TargetHWDeviceType	Specified
TargetUnknown	off
ProdEqTarget	on

**Table 5.7. DisplayModel\_Step5\_start Configuration Set.Components [14](6)**

Property	Value
Name	Model Referencing
Description	
Components	
UpdateModelReferenceTargets	IfOutOfDateOrStructuralChange
CheckModelReferenceTargetMessage	error
EnableParallelModelReferenceBuilds	off
ParallelModelReferenceErrorOnInvalidPool	on
ParallelModelReferenceMATLABWorkerInit	None
ModelReferenceNumInstancesAllowed	Multi
PropagateVarSize	Infer from blocks in model
ModelDependencies	
ModelReferencePassRootInputsByReference	on
ModelReferenceMinAlgLoopOccurrences	off
PropagateSignalLabelsOutOfModel	off
SupportModelReferenceSimTargetCustomCode	off

**Table 5.8. DisplayModel\_Step5\_start Configuration Set.Components [14](7)**

Property	Value
Name	Simulation Target
Description	
Components	
SimCustomSourceCode	
SimCustomHeaderCode	
SimCustomInitializer	
SimCustomTerminator	
SimReservedNameArray	
SimUserSources	
SimUserIncludeDirs	
SimUserLibraries	
SFSimEnableDebug	on
SFSimOverflowDetection	on
SFSimEcho	on
SimBlas	on

SimCtrlC	on
SimExtrinsic	on
SimIntegrity	on
SimUseLocalCustomCode	off
SimParseCustomCode	on
SimBuildMode	sf_incremental_build
SimDataInitializer	
SimGenImportedTypeDefs	off

**Table 5.9. DisplayModel\_Step5\_start Configuration Set.Components [14](8)**

Property	Value
Name	Code Generation
SystemTargetFile	ert.tlc
TLCOptions	
CodeGenDirectory	
GenCodeOnly	off
MakeCommand	make_rtw
GenerateMakefile	on
PackageGeneratedCodeAndArtifacts	off
PackageName	
TemplateMakefile	ert_default_tmf
PostCodeGenCommand	
Description	Embedded Coder
GenerateReport	on
SaveLog	off
RTWVerbose	on
RetainRTWFile	off
ProfileTLC	off
TLCDebug	off
TLCCoverage	off
TLCAssert	off
ProcessScriptMode	Default
ConfigurationMode	Optimized
ProcessScript	ert_make_rtw_hook
ConfigurationScript	
ConfigAtBuild	off
RTWUseLocalCustomCode	off
RTWUseSimCustomCode	off
CustomSourceCode	

CustomHeaderCode	
CustomInclude	
CustomSource	
CustomLibrary	
CustomInitializer	
CustomTerminator	
Toolchain	Automatically locate an installed toolchain
BuildConfiguration	Faster Builds
CustomToolchainOptions	
IncludeHyperlinkInReport	on
LaunchReport	on
PortableWordSizes	on
GenerateErtSFunction	off
CreateSILPILBlock	None
CodeExecutionProfiling	off
CodeExecutionProfileVariable	executionProfile
CodeProfilingSaveOptions	SummaryOnly
CodeProfilingInstrumentation	off
SILDebugging	off
TargetLang	C
IncludeRootSignalInRTWFile	off
IncludeVirtualBlocksInRTWFileBlockHierarchy-Map	off
IncludeRegionsInRTWFileBlockHierarchyMap	off
IncludeERTFirstTime	off
GenerateTraceInfo	on
GenerateTraceReport	on
GenerateTraceReportSl	on
GenerateTraceReportSf	on
GenerateTraceReportEml	on
GenerateCodeInfo	off
GenerateWebview	off
GenerateCodeMetricsReport	off
GenerateCodeReplacementReport	off
RTWCompilerOptimization	Off
ObjectivePriorities	
RTWCustomCompilerOptimizations	
CheckMdlBeforeBuild	Off
CustomRebuildMode	OnUpdate

DataInitializer	
Components	[DisplayModel_Step5_start Configuration Set.Components(8).Components(1) [25], DisplayModel_Step5_start Configuration Set.Components(8).Components(2) [26]]

**Table 5.10. DisplayModel\_Step5\_start Configuration Set.Components [14](9)**

Property	Value
Description	HDL Coder custom configuration component
Components	
Name	HDL Coder

**Table 5.11. DisplayModel\_Step5\_start Configuration Set.Components [14](10)**

Property	Value
Description	Design Verifier Custom Configuration Component
Components	
Name	Design Verifier
DVMode	TestGeneration
DVMaxProcessTime	300
DVDisplayUnsatisfiableObjectives	off
DVAutomaticStubbing	on
DVDesignMinMaxConstraints	on
DVOutputDir	sldv_output/\$ModelName\$
DVMakeOutputFilesUnique	on
DVBlockReplacement	off
DVBlockReplacementRulesList	<FactoryDefaultRules>
DVBlockReplacementModelFileName	\$ModelName\$_replacement
DVParameters	off
DVParametersConfigFileName	sldv_params_template.m
DVModelCoverageObjectives	MCDC
DVTestConditions	UseLocalSettings
DVTestObjectives	UseLocalSettings
DVMaxTestCaseSteps	500
DVTestSuiteOptimization	CombinedObjectives (Nonlinear Extended)
DVAssertions	UseLocalSettings
DVProofAssumptions	UseLocalSettings
DVExtendExistingTests	off
DVExistingTestFile	
DVIgnoreExistTestSatisfied	on

DVIgnoreCovSatisfied	off
DVCoverageDataFile	
DVCovFilter	off
DVCovFilterFileName	
DVDetectIntegerOverflow	on
DVDetectDivisionByZero	on
DVDesignMinMaxCheck	off
DVDetectDeadLogic	off
DVDetectOutOfBounds	off
DVProvingStrategy	Prove
DVMaxViolationSteps	20
DVSaveDataFile	on
DVDataFileName	\$ModelName\$_sldvdata
DVSaveExpectedOutput	off
DVRandomizeNoEffectData	off
DVSaveHarnessModel	on
DVHarnessModelFileName	\$ModelName\$_harness
DVModelReferenceHarness	on
DVSaveSystemTestHarness	off
DVSystemTestFileName	\$ModelName\$_harness
DVSaveReport	off
DVReportFileName	\$ModelName\$_report
DVReportIncludeGraphics	off
DVDisplayReport	on
DVDisplayResultsOnModel	off

**Table 5.12. DisplayModel\_Step5\_start Configuration Set.Components(8).Components [24](1)**

Property	Value
Name	Code Appearance
Description	
Components	
Comment	
ForceParamTrailComments	off
GenerateComments	on
IgnoreCustomStorageClasses	off
IgnoreTestpoints	off
IncHierarchyInIds	off
MaxIdLength	31

PreserveName	off
PreserveNameWithParent	off
ShowEliminatedStatement	off
OperatorAnnotations	off
IncAutoGenComments	off
SimulinkDataObjDesc	off
SFDataObjDesc	off
MATLABFcnDesc	off
IncDataTypeInIds	off
PrefixModelToSubsysFcnNames	on
MangleLength	1
CustomSymbolStr	\$R\$N\$M
CustomSymbolStrGlobalVar	\$R\$N\$M
CustomSymbolStrType	\$N\$R\$M
CustomSymbolStrField	\$N\$M
CustomSymbolStrFcn	\$R\$N\$M\$F
CustomSymbolStrFcnArg	rt\$I\$N\$M
CustomSymbolStrBlkIO	rtb_\$N\$M
CustomSymbolStrTmpVar	\$N\$M
CustomSymbolStrMacro	\$R\$N\$M
CustomSymbolStrUtil	\$N\$C
CustomCommentsFcn	
DefineNamingRule	None
DefineNamingFcn	
ParamNamingRule	None
ParamNamingFcn	
SignalNamingRule	None
SignalNamingFcn	
InsertBlockDesc	off
InsertPolySpaceComments	off
SimulinkBlockComments	on
MATLABSourceComments	off
EnableCustomComments	off
InternalIdentifier	Classic
InlinedPrmAccess	Literals
ReqsInCode	on
UseSimReservedNames	off
ReservedNameArray	

**Table 5.13. DisplayModel\_Step5\_start Configuration Set.Components(8).Components [24](2)**

Property	Value
Name	Target
Description	
Components	
IsERTTarget	on
TargetFcnLib	ansi_tfl_table_tmw.mat
TargetLibSuffix	
TargetPreCompLibLocation	
GenFloatMathFcnCalls	ANSI_C
TargetFunctionLibrary	ANSI_C
CodeReplacementLibrary	ANSI_C
UtilityFuncGeneration	Auto
ERTMultiwordTypeDef	System defined
ERTMultiwordLength	256
MultiwordLength	2048
GenerateFullHeader	on
GenerateSampleERTMain	on
GenerateTestInterfaces	off
IsPILTarget	off
ModelReferenceCompliant	on
ParMdlRefBuildCompliant	on
CompOptLevelCompliant	on
ConcurrentExecutionCompliant	on
IncludeMdlTerminateFcn	on
GeneratePreprocessorConditionals	Use local settings
CombineOutputUpdateFcns	on
CombineSignalStateStructs	off
SuppressErrorStatus	off
ERTFirstTimeCompliant	on
IncludeFileDelimiter	Auto
ERTCustomFileBanners	on
SupportAbsoluteTime	on
LogVarNameModifier	rt_
MatFileLogging	off
MultiInstanceERTCode	off
SupportNonFinite	on
SupportComplex	on



PurelyIntegerCode	off
SupportContinuousTime	off
SupportNonInlinedSFCns	off
SupportVariableSizeSignals	off
ParenthesesLevel	Nominal
GenerateClassInterface	off
ModelStepFunctionPrototypeControlCompliant	on
CPPClassGenCompliant	on
AutosarCompliant	off
GRTInterface	off
GenerateAllocFcn	off
UseToolchainInfoCompliant	on
GenerateASAP2	off
ExtMode	off
ExtModeTransport	0
ExtModeStaticAlloc	off
ExtModeStaticAllocSize	1000000
ExtModeTesting	off
ExtModeMexFile	ext_comm
ExtModeMexArgs	
ExtModeIntrfLevel	Level1
InlinedParameterPlacement	NonHierarchical
TargetOS	BareBoardExample
MultiInstanceErrorCode	Error
RateGroupingCode	on
RootIOFormat	Individual arguments
RTWCAPISignals	off
RTWCAPIParams	off
RTWCAPISates	off
RTWCAPIRootIO	off
ERTSrcFileBannerTemplate	ert_code_template.cgt
ERTHdrFileBannerTemplate	ert_code_template.cgt
ERTDataSrcFileTemplate	ert_code_template.cgt
ERTDataHdrFileTemplate	ert_code_template.cgt
ERTCustomFileTemplate	example_file_process.tlc
InitialValueSource	Model
ModuleNamingRule	Unspecified
ModuleName	
EnableDataOwnership	off

SignalDisplayLevel	10
ParamTuneLevel	10
GlobalDataDefinition	Auto
DataDefinitionFile	global.c
GlobalDataReference	Auto
ERTFilePackagingFormat	Modular
DataReferenceFile	global.h
PreserveExpressionOrder	off
PreserveIfCondition	off
ConvertIfToSwitch	off
PreserveExternInFcnDecls	on
SuppressUnreachableDefaultCases	off
IndentStyle	K&R
IndentSize	2
EnableUserReplacementTypes	off
ReplacementTypes	DisplayModel_Step5_start Configuration Set.Components(8).Components(2).ReplacementTypes-[29]
MemSecPackage	--- None ---
MemSecDataConstants	Default
MemSecDataIO	Default
MemSecDataInternal	Default
MemSecDataParameters	Default
MemSecFuncInitTerm	Default
MemSecFuncExecute	Default
MemSecFuncSharedUtil	Default

**Table 5.14. DisplayModel\_Step5\_start Configuration Set.Components(8).Components(2) [26].ReplacementTypes**

Field	Value
double	
single	
int32	
int16	
int8	
uint32	
uint16	
uint8	
boolean	

## System Model Configuration

---

int	
uint	
char	

---

# Chapter 6. Glossary

**Atomic Subsystem.** A subsystem treated as a unit by an implementation of the design documented in this report. The implementation computes the outputs of all the blocks in the atomic subsystem before computing the next block in the parent system's block execution order (sorted list).

**Block Diagram.** A Simulink block diagram represents a set of simultaneous equations that relate a system or subsystem's inputs to its outputs as a function of time. Each block in the diagram represents an equation of the form  $y = f(t, x, u)$  where  $t$  is the current time,  $u$  is a block input,  $y$  is a block output, and  $x$  is a system state (see the Simulink documentation for information on the functions represented by the various types of blocks that make up the diagram). Lines connecting the blocks represent dependencies among the blocks, i.e., inputs whose current values are the outputs of other blocks. An implementation of a design described in this document computes a root or atomic system's outputs at each time step by computing the outputs of the blocks in an order determined by block input/output dependencies.

**Block Parameter.** A variable that determines the output of a block along with its inputs, for example, the gain parameter of a Gain block.

**Block Execution Order.** The order in which Simulink evaluates blocks during simulation of a model. The block execution order determined by Simulink ensures that a block executes only after all blocks on whose outputs it depends are executed.

**Checksum.** A number that indicates whether different versions of a model or atomic subsystem differ functionally or only cosmetically. Different checksums for different versions of the same model or subsystem indicate that the versions differ functionally.

**Design Variable.** A symbolic (MATLAB) variable or expression used as the value of a block parameter. Design variables allow the behavior of the model to be altered by altering the value of the design variable.

**Signal.** A block output, so-called because block outputs typically vary with time.

**Virtual Subsystem.** A subsystem that is purely graphical, i.e., is intended to reduce the visual complexity of the block diagram of which it is a subsystem. An implementation of the design treats the blocks in the subsystem as part of the first nonvirtual ancestor of the virtual subsystem (see Atomic Subsystem).

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# Chapter 7. About this Report

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## 7.1. Report Overview

This report describes the design of the DisplayModel\_Step5\_start system. The report was generated automatically from a Simulink model used to validate the design. It contains the following sections:

**Model Version.** Specifies information about the version of the model from which this design description was generated. Includes the model checksum, a number that indicates whether different versions of the model differ functionally or only cosmetically. Different checksums for different versions indicate that the versions differ functionally.

**Root System.** Describes the design's root system.

**Subsystems.** Describes each of the design's subsystems.

**Design Variables.** Describes system design variables, i.e., MATLAB variables and expressions used as block parameter values.

**System Model Configuration.** Lists the configuration parameters, e.g., start and stop time, of the model used to simulate the system described by this report.

**Requirements Traceability.** Shows design requirements associated with elements of the design model. This section appears only if the design model contains requirements links.

**Glossary.** Defines Simulink terms used in this report.

## 7.2. Root System Description

This section describes a design's root system. It contains the following sections:

**Diagram.** Simulink block diagram that represents the algorithm used to compute the root system's outputs.

**Description.** Description of the root system. This section appears only if the model's root system has a Documentation property or a Doc block.

**Interface.** Name, data type, width, and other properties of the root system's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the root system has input or output ports.

**Blocks.** This section has two subsections:

- **Parameters.** Describes key parameters of blocks in the root system. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, i.e., blocks that use lookup tables to compute their outputs.

- **Block Execution Order.** Order in which blocks must be executed at each time step in order to ensure that each block's inputs are available when it executes.

**State Charts.** Describes state charts used in the root system. This section appears only if the root system contains Stateflow blocks.

## 7.3. Subsystem Descriptions

This section describes a design's subsystems. Each subsystem description contains the following sections:

**Checksum.** This section appears only if the subsystem is an atomic subsystem. The checksum indicates whether the version of the model subsystem used to generate this report differs functionally from other versions of the model subsystem. If two model checksums differ, the corresponding versions of the model differ functionally.

**Diagram.** Simulink block diagram that graphically represents the algorithm used to compute the subsystem's outputs.

**Description.** Description of the subsystem. This section appears only if the subsystem has a Documentation property or contains a Doc block.

**Interface.** Name, data type, width, and other properties of the subsystem's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the subsystem is atomic and has input or output ports.

**Blocks.** Blocks that this subsystem contains. This section has two subsections:

- **Parameters.** Key parameters of blocks in the subsystem. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which the subsystem's blocks must be executed at each time step in order to ensure that each block's inputs are available when the block executes. This section appears only if the subsystem is atomic.

**State Charts.** Describes state charts used in the subsystem. This section appears only if the root system contains Stateflow blocks.

## 7.4. State Chart Descriptions

This section describes the state machines used by Stateflow blocks to compute their outputs, i.e., Stateflow blocks. Each state machine description contains the following sections:

**Chart.** Diagram representing the state machine.

**States.** Describes the state machine's states. Each state description includes the state's diagram and diagrams and/or descriptions of graphical functions, Simulink functions, truth tables, and MATLAB functions parented by the state.

**Transitions.** Transitions between the state machine's states. Each transition description specifies the values of key transition properties. Appears only if a transition has properties that do not appear on the chart.

**Junctions.** Transition junctions. Each junction description specifies the values of key junction properties. Appears only if a junction has properties that do not appear on the chart.

**Events.** Events that trigger state transitions. Each event description specifies the values of key event properties.

**Data.** Data types and other properties of the Stateflow block's inputs, outputs, and other state machine data.

**Targets.** Executable implementations of the state machine used to compute the outputs of the corresponding Stateflow block.

**MATLAB Supporting Functions.** List of functions invoked by MATLAB functions defined in the chart.