Simulink Design Verifier Report

C:\Users\bpotter\OneDrive - MathWorks\DO_Project_18b\DO_03_Design\F-CC\verification\design_error_detections\dead_logic\FCC_replacement.slx bpotter Simulink Design Verifier Report: C:\Users\bpotter\OneDrive - MathWorks\DO_Project_18b\DO_03_Design\FCC\verification\design_error_detections\dead_logic\FCC_replacement.slx bpotter

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Chapter 1. Summary

Analysis Information.

Model: FCC

Replacement Model: C:\Users\bpotter\OneDrive - MathWorks\DO_Pr-

oject_18b\DO_03_Design\FCC\verification\design_error_detections\dead_logic\FCC_replacemen-

t.slx

Mode: Design error detection Status: Completed normally

Analysis Time: 70s

Objectives Status.

Number of Objectives: 121

Dead Logic: 6

Chapter 2. Analysis Information

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Model Information

File: FCC Version: 1.53

Time Stamp: Thu Oct 25 13:14:13 2018

Author: bpotter

Analysis Options

Mode: DesignErrorDetection Detect dead logic: on Detect active logic: off Maximum Analysis Time: 300s **Block Replacement:** off off Parameters Analysis: Include expected output values: off Randomize data that do not affect the off outcome: Additional analysis to reduce instanc- on es of rational approximation: Save Data: on Save Harness: off Save Report: on

Constraints

Design Min Max Constraints

Name	Design Min Max Constraint	
Act_Pos1	[-3276832767]	
Act_Pos2	[-3276832767]	

Name	Design Min Max Constraint
Act_Pos3	[-3276832767]
Pilot_theta_cmd	[-3276832767]
Pilot_phi_cmd	[-3276832767]
Pilot_r_cmd	[-3276832767]
AHRS1	[-180180]
AHRS2	[-180180]
AHRS3	[-180180]

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

#	Туре	Description
1	Multi-instance Model reference approximation	The model being analyzed references at least one model more than once. Simulink Design Verifier copies referenced model contents into the replacement model before analysis so that coverage objectives for each instance of a model are treated separately. This differs from Model Coverage reporting that combines instances for coverage. Coverage results from simulating test cases may differ from analysis results.

Chapter 3. Dead Logic

Simulink Design Verifier found that these decision and condition outcomes cannot occur and are dead-logic in the model. Dead-logic in the model can also be a side-effect of parameter configurations or input specified minimum maximum constraints.

#	Type	Model Item	Description
1	Decision	ActuatorControl1/Saturation	input > lower limit can only be true
2	Decision	ActuatorControl1/Saturation	input >= upper limit can never be true
3	Decision	ActuatorControl2/Saturation	input > lower limit can only be true
4	Decision	ActuatorControl2/Saturation	input >= upper limit can never be true
5	Decision	ActuatorControl3/Saturation	input > lower limit can only be true
6	Decision	ActuatorControl3/Saturation	input >= upper limit can never be true

Chapter 4. Derived Ranges

Signal	Derived Ranges
RateTransition1- Outport 1	[-0.10.1]
RateTransition2- Outport 1	[-0.10.1]
RateTransition3- Outport 1	[-0.10.1]
Act_Pos1- Outport 1	[-3276832767]
TypeConversion3- Outport 1	[-3276832767]
Scaling3- Outport 1	[-0.10.1]
ActuatorControl1/Sum- Outport 1	[-0.20.2]
ActuatorControl1/Difference/UD- Outport 1	[-0.20.2]
ActuatorControl1/Difference/Diff- Outport 1	[-0.40.4]
ActuatorControl1/Gain- Outport 1	[-0.060.060001]
ActuatorControl1/Gain1- Outport 1	[-0.00800010.0080001]
ActuatorControl1/Gain2- Outport 1	[-0.0240.024]
ActuatorControl1/Integrator- Outport 1	[-0.10.1]
ActuatorControl1/Sum1- Outport 1	[-0.1640.168]
ActuatorControl1/Saturation- Outport 1	[-0.1640.168]
Scaling6- Outport 1	[-5373855049]
TypeConversion6- Outport 1	[-3276832767]
Actuator1- Outport 1	[-3276832767]
Act_Pos2- Outport 1	[-3276832767]
TypeConversion4- Outport 1	[-3276832767]
Scaling4- Outport 1	[-0.10.1]
ActuatorControl2/Sum- Outport 1	[-0.20.2]
ActuatorControl2/Difference/UD- Outport 1	[-0.20.2]
ActuatorControl2/Difference/Diff- Outport 1	[-0.40.4]
ActuatorControl2/Gain- Outport 1	[-0.060.060001]
ActuatorControl2/Gain1- Outport 1	[-0.00800010.0080001]
ActuatorControl2/Gain2- Outport 1	[-0.0240.024]
ActuatorControl2/Integrator- Outport 1	[-0.10.1]
ActuatorControl2/Sum1- Outport 1	[-0.1640.168]
ActuatorControl2/Saturation- Outport 1	[-0.1640.168]
Scaling7- Outport 1	[-5373855049]
TypeConversion7- Outport 1	[-3276832767]
Actuator2- Outport 1	[-3276832767]
Act_Pos3- Outport 1	[-3276832767]
TypeConversion5- Outport 1	[-3276832767]
Scaling5- Outport 1	[-0.10.1]

Signal	Derived Ranges
ActuatorControl3/Sum- Outport 1	[-0.20.2]
ActuatorControl3/Difference/UD- Outport 1	[-0.20.2]
ActuatorControl3/Difference/Diff- Outport 1	[-0.40.4]
ActuatorControl3/Gain- Outport 1	[-0.060.060001]
ActuatorControl3/Gain1- Outport 1	[-0.00800010.0080001]
ActuatorControl3/Gain2- Outport 1	[-0.0240.024]
ActuatorControl3/Integrator- Outport 1	[-0.10.1]
ActuatorControl3/Sum1- Outport 1	[-0.1640.168]
ActuatorControl3/Saturation- Outport 1	[-0.1640.168]
Scaling8- Outport 1	[-5373855049]
TypeConversion8- Outport 1	[-3276832767]
Actuator3- Outport 1	[-3276832767]
Pilot_theta_cmd- Outport 1	[-3276832767]
TypeConversion- Outport 1	[-3276832767]
Scaling- Outport 1	[-30.00130]
Pilot_phi_cmd- Outport 1	[-3276832767]
TypeConversion1- Outport 1	[-3276832767]
Scaling1- Outport 1	[-30.00130]
Pilot_r_cmd- Outport 1	[-3276832767]
TypeConversion2- Outport 1	[-3276832767]
Scaling2- Outport 1	[-1515]
Model2/Constant- Outport 1	0
AHRS1_Valid- Outport 1	[FT]
AHRS2_Valid- Outport 1	[FT]
AHRS3_Valid- Outport 1	[FT]
Model2/Sum- Outport 1	[03]
Model2/MultiportSwitch- Outport 1	[-540540]
Model1/Sum- Outport 1	[-570570]
Model1/Gain- Outport 1	[-758.1758.1]
Model1/Sum1- Outport 1	[-570570]
Model1/Gain1- Outport 1	[-49.0249.02]
Model1/Gain2- Outport 1	[-1282.51282.5]
Model1/Gain3- Outport 1	[-678.3678.3]
Model1/Sum2- Outport 1	[-555555]
Model1/Gain4- Outport 1	[-73.81573.815]
Model1/Gain5- Outport 1	[-1293.21293.2]
Model1/Integrator- Outport 1	[-1010]
Model1/Integrator1- Outport 1	[-1010]

Signal	Derived Ranges
Model1/Integrator2- Outport 1	[-1010]
Model1/Sum3- Outport 1	[-768.1768.1]
Model1/Saturation- Outport 1	[-3030]
Model1/Sum4- Outport 1	[-59.0259.02]
Model1/Saturation1- Outport 1	[-3030]
Model1/Sum5- Outport 1	[-83.81583.815]
Model1/Saturation2- Outport 1	[-3030]
UnitDelay- Outport 1	[-540540]
Model/SOF- Outport 1	[-1937.11937.1]
Model/Sum5- Outport 1	[-1967.11967.1]
Model/RollOff1/s_1- Outport 1	[-331.27331.27]
Model/RollOff1/UnitDelay- Outport 1	[-InfInf]
Model/RollOff1/a_2_1- Outport 1	[-InfInf]
Model/RollOff1/SumA21- Outport 1	[-InfInf]
Model/Sum4- Outport 1	[-811.55811.55]
Model/RollOff2/s_1- Outport 1	[-136.67136.67]
Model/RollOff2/UnitDelay- Outport 1	[-InfInf]
Model/RollOff2/a_2_1- Outport 1	[-InfInf]
Model/RollOff2/SumA21- Outport 1	[-InfInf]
Model/Sum6- Outport 1	[-1200.81200.8]
Model/RollOff3/s_1- Outport 1	[-202.23202.23]
Model/RollOff3/UnitDelay- Outport 1	[-InfInf]
Model/RollOff3/a_2_1- Outport 1	[-InfInf]
Model/RollOff3/SumA21- Outport 1	[-InfInf]
Model/Saturation- Outport 1	[-0.10.1]
AHRS1- Outport 1	[-180180]
AHRS2- Outport 1	[-180180]
Model2/Mid_Value/MinMax- Outport 1	[-180180]
AHRS3- Outport 1	[-180180]
Model2/Mid_Value/MinMax1- Outport 1	[-180180]
Model2/Mid_Value/MinMax2- Outport 1	[-180180]
Model2/Mid_Value/MinMax3- Outport 1	[-180180]
Model2/Avg_Value/Constant- Outport 1	0
Model2/Avg_Value/Switch- Outport 1	[-180180]
Model2/Avg_Value/Switch1- Outport 1	[-180180]
Model2/Avg_Value/Switch2- Outport 1	[-180180]
Model2/Avg_Value/Sum- Outport 1	[-540540]
Model2/Avg_Value/Gain- Outport 1	[-270270]

Derived Ranges

Signal	Derived Ranges
Model2/Single_Value/Constant- Outport 1	0
Model2/Single_Value/Switch- Outport 1	[-180180]
Model2/Single_Value/Switch1- Outport 1	[-180180]
Model2/Single_Value/Switch2- Outport 1	[-180180]
Model2/Single_Value/Sum- Outport 1	[-540540]