CS m51A: Logic Design of Digital Systems
UCLA Computer Science Department
Fall 2009
Final

Time: 3 hours
Note: Closed book, closed notes, no electronic computing or communications devices.

Name: _____

Student ID: _____

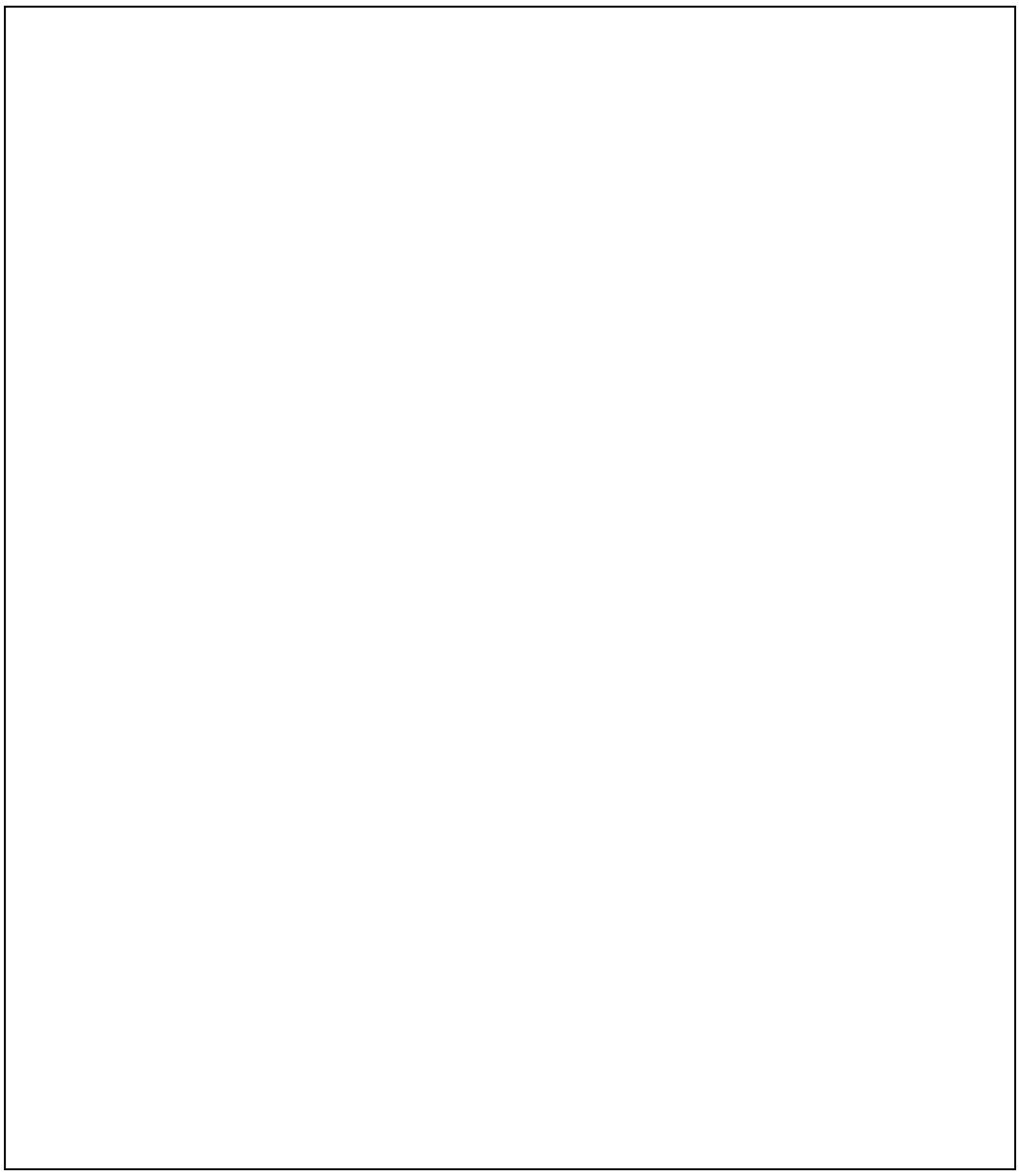
Question	Points	Grades
1	10	
2	15	
3	20	
4	15	
5	20	
6	20	
Total	100	

Question 1: Combinational System

Design a 4-bit priority encoder, where a priority encoder converts a 4-bit input into a binary representation of the signal with the highest priority. The table below summarizes the functionality.

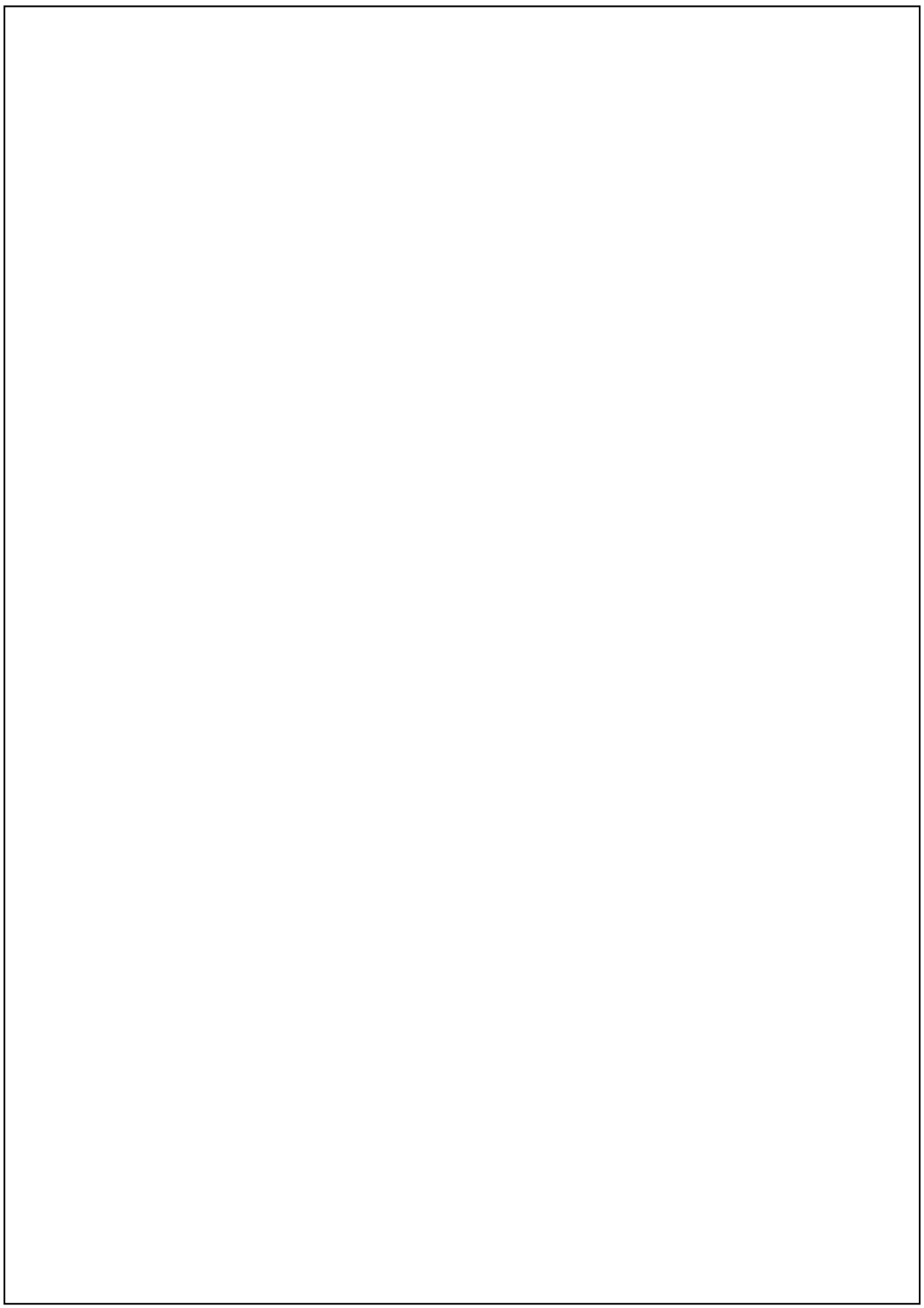
Input	Output
x3,x2,x1,x0	**y1,y0**
1---	11
01--	10
001-	01
000-	00

For full credit use an encoder and the minimum number of gates.



Question 2: Counters

A *superstitious counter* is a 4-bit counter that skips the value 13. Build a superstitious counter using one 4-bit loadable binary counter and two 2-input gates.

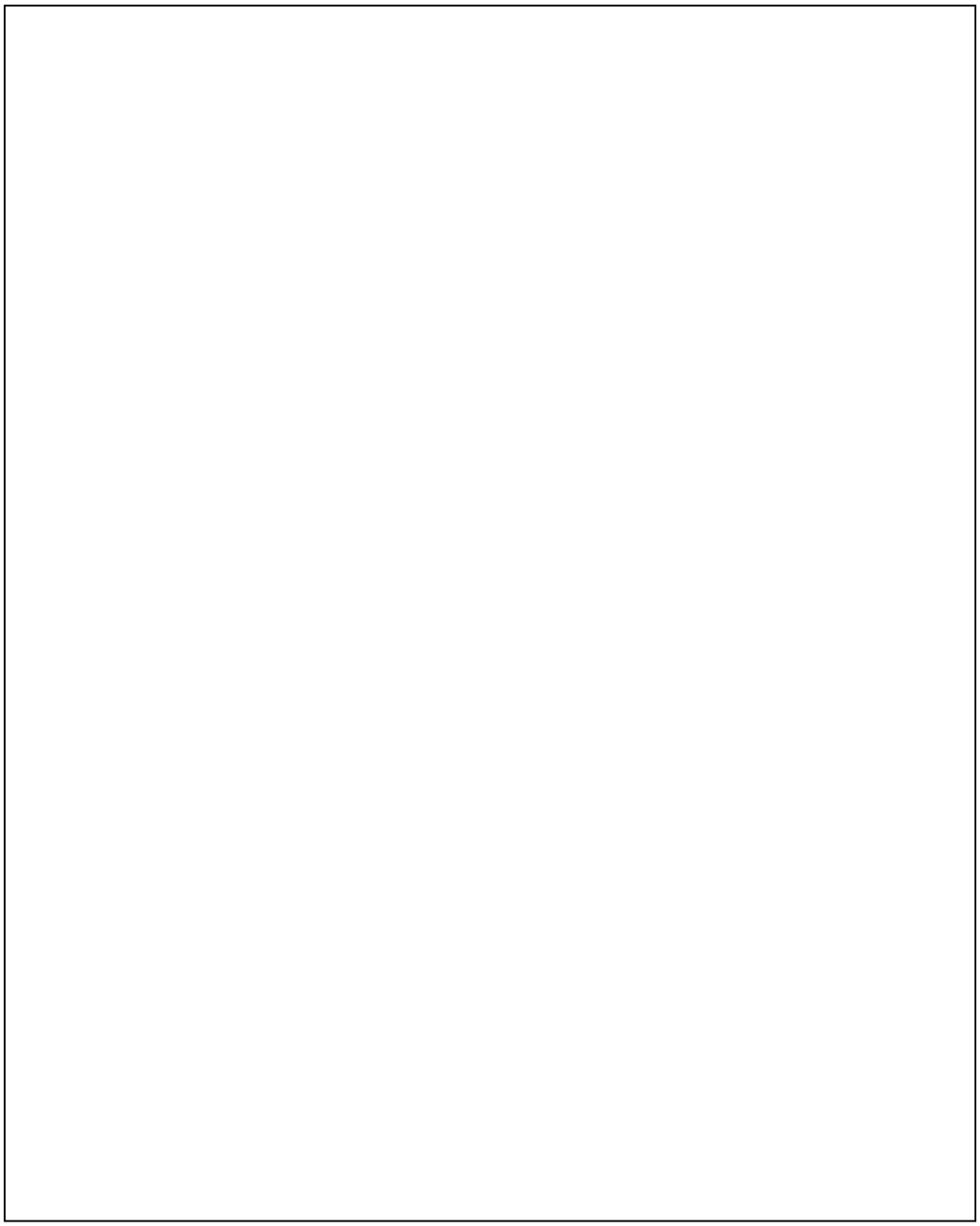


Question 3: Network of Counters

Using only modulo-16 counters, T-flip-flops, multiplexers, and gates, design a counter with the following counting sequence:

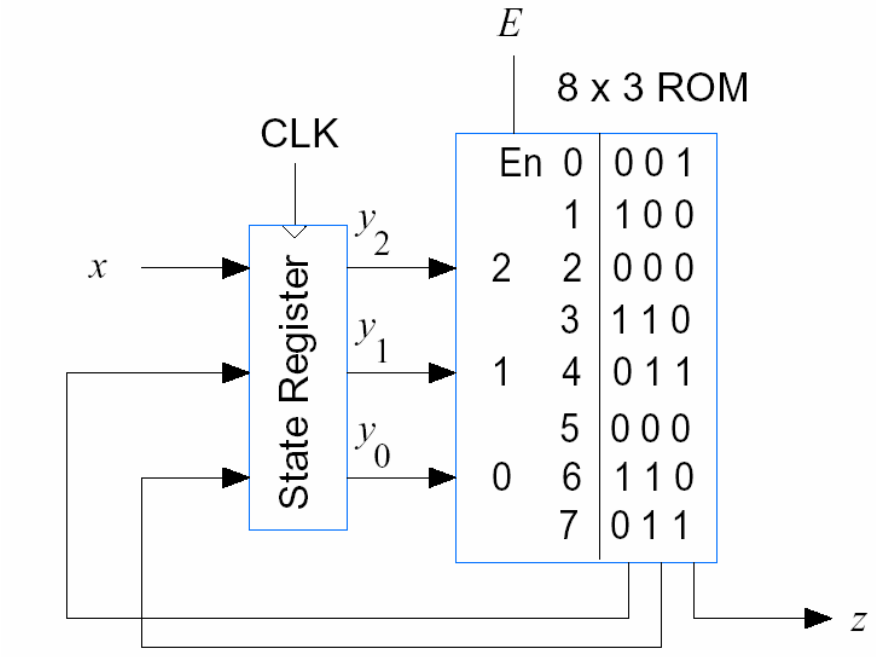
0, 1, 2, …, 14, 15, 15, 14, ..., 2, 1, 0
0, 1, 2, …, 13, 14, 14, 13, …, 2, 1, 0
0, 1, 2, …, 12, 13, 13, 12, …, 2, 1, 0
…

For full credit, use the minimal amount of components and the minimal number of counters.



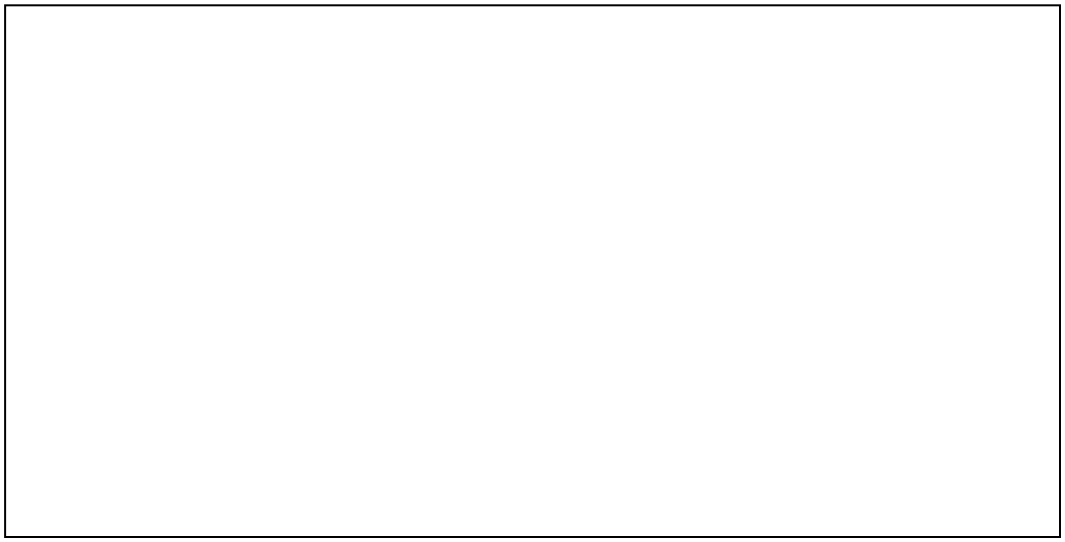
Question 4: ROM

Give the state table for the following sequential system.

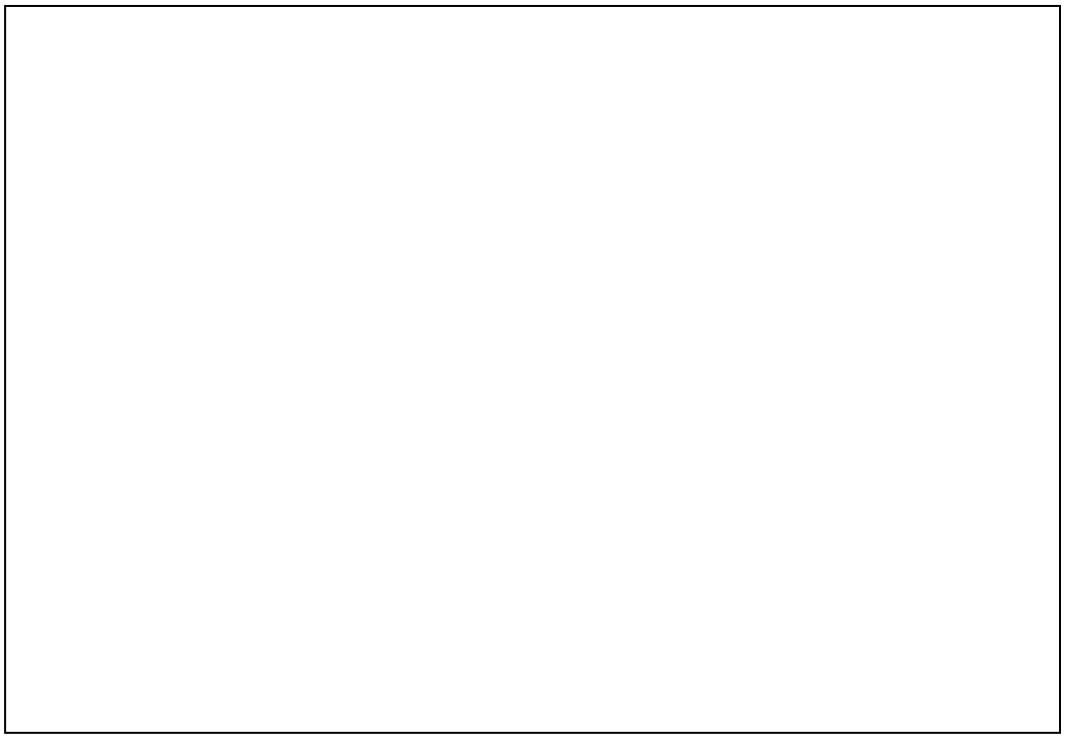


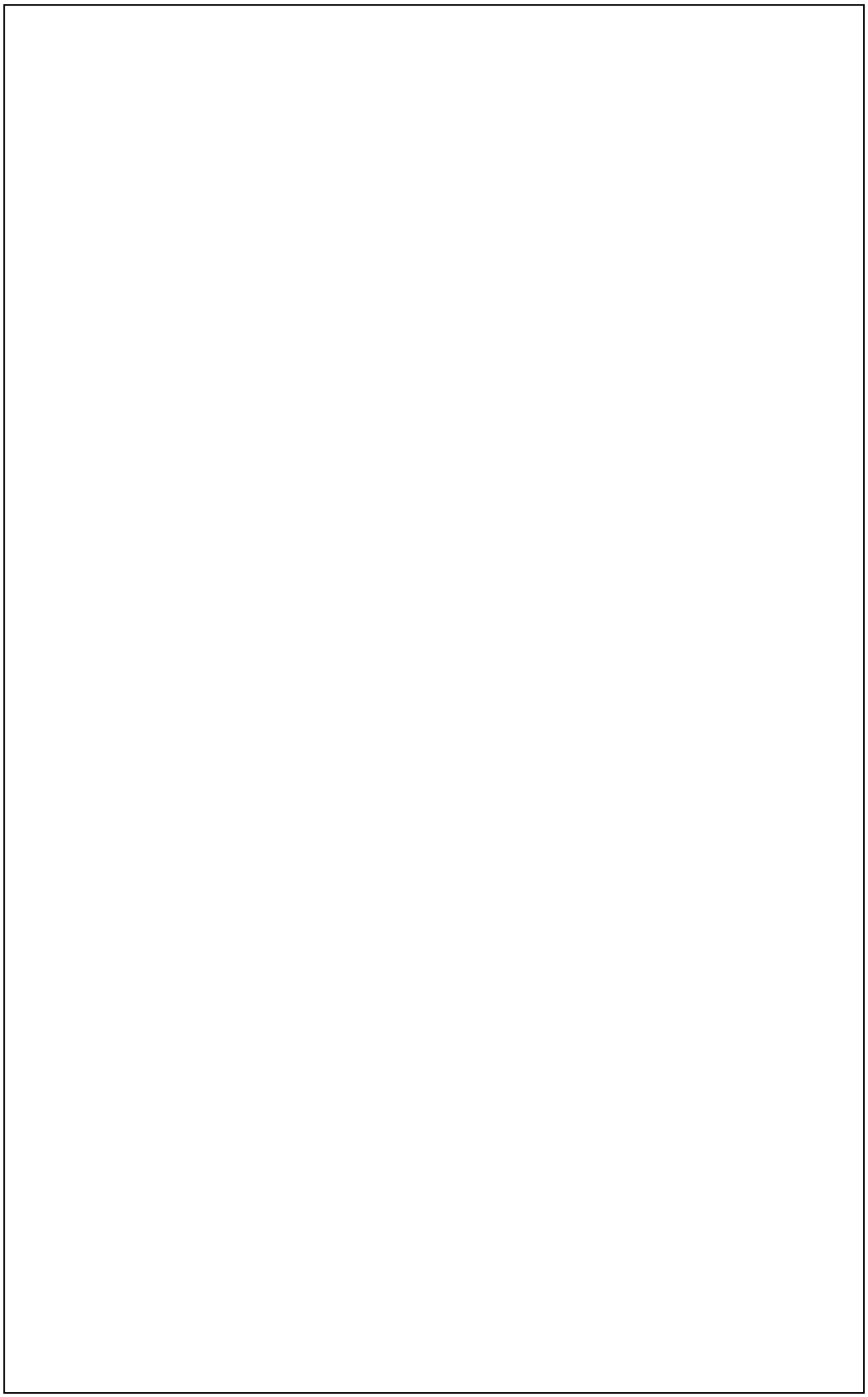
Question 5: Sequential Systems with Flip-Flops
Implement a pattern recognizer using JK flip-flops and multiplexers only. The pattern recognizers has a one bit input x ={0,1} and an output $\underline{z}$ ={0, 1, 2}. The output is 1, when the last input symbols are 01 or 011. The output is 2, whenever the last three input signals are identical. It is 0, otherwise. Give a state diagram of your system. For full credit use the smallest number of components. You can use the constants 0 and 1.

a) Provide the state diagram

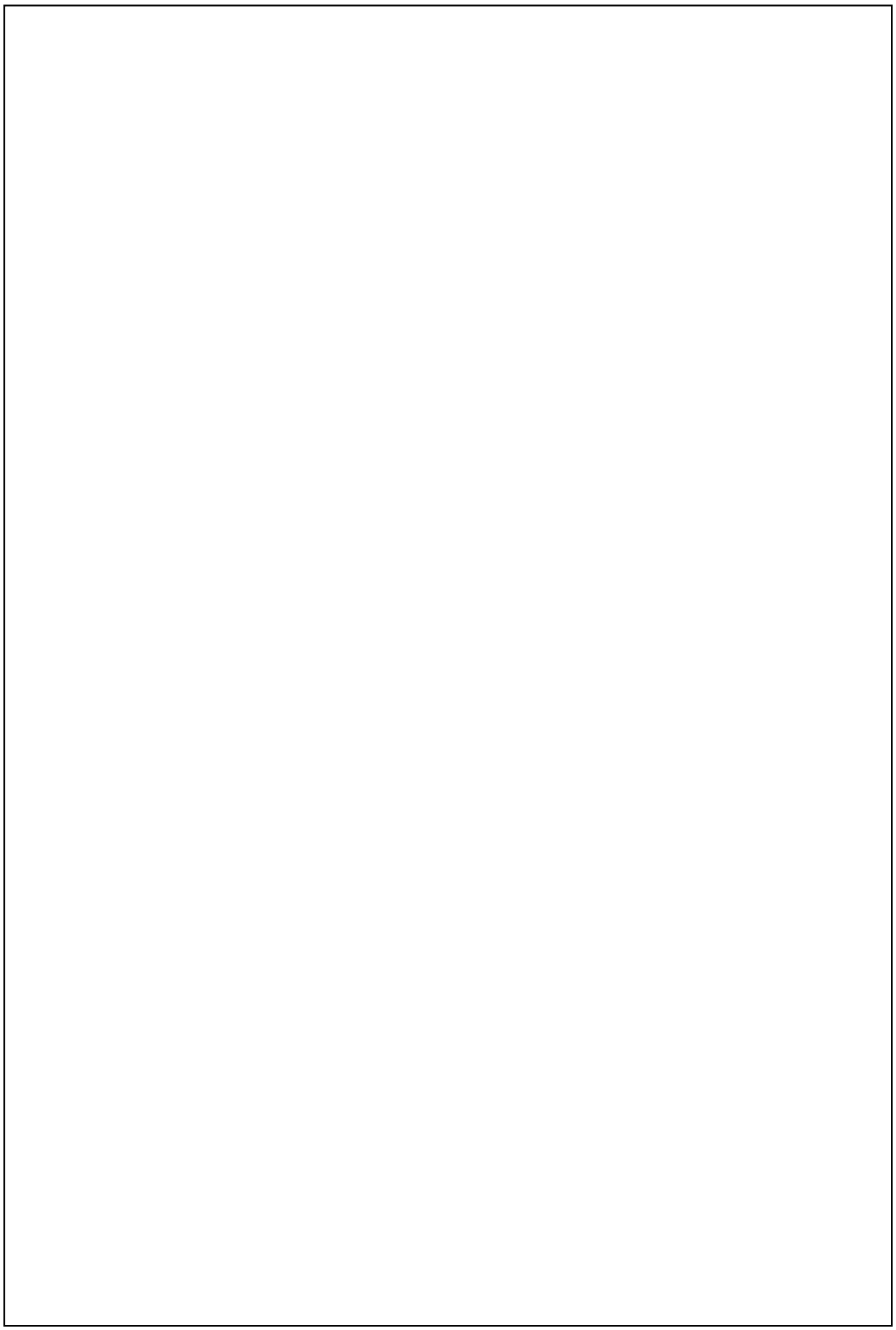


b) Show your design process (e.g. excitation tables, k-maps, etc)





c) Give your final design here.



Question 6: Sequential System with Modules

Design a sequential system given by the state diagram below. The available components are parallel-in/parallel-out shift registers, decoders, and NOR gates. For full credit use, the minimal amount of components.

Present State	**State Inputs**	
	x=0	**x=1**
A	D, 1	C, 0
B	C, 1	D, 1
C	A, 0	A, 0
D	H, 1	F, 0
E	F, 1	G, 0
F	A, 0	G, 1
G	H, 1	E, 0
H	E, 1	B, 1
	Next State, Output