CS M51A/EE M16 FINAL EXAM
– closed books and notes –
(8 problems, 180 minutes)
PLEASE BE SYSTEMATIC, ORGANIZED, and NEAT:
– this will be considered in the grading.

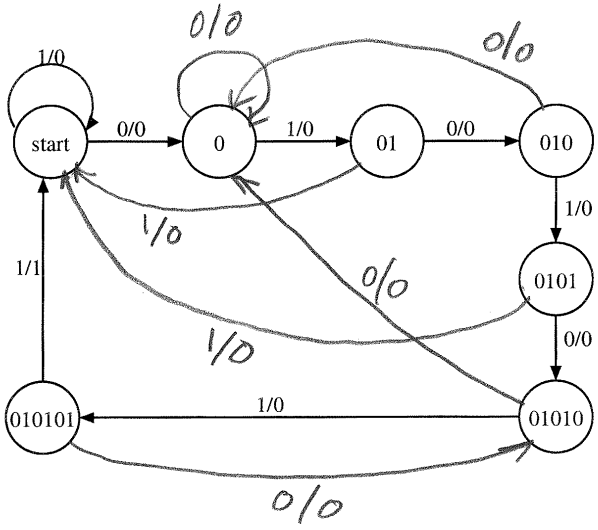
December 13, 2002

Name: SOLUTIONS

Problem	Points	Score
1	20	
2	10	
3	14	
4	12	
5	8	
6	13	
7	13	
8	10	
Total	100	

Problem 1. (20 points) Design a sequential system which recognizes the pattern 0101011.

a) [6 points] Complete the following state diagram. Each state is labeled with a sequence that it "recognizes".



The correspondence between the state assignment and sequence that it detects is shown in the next table.

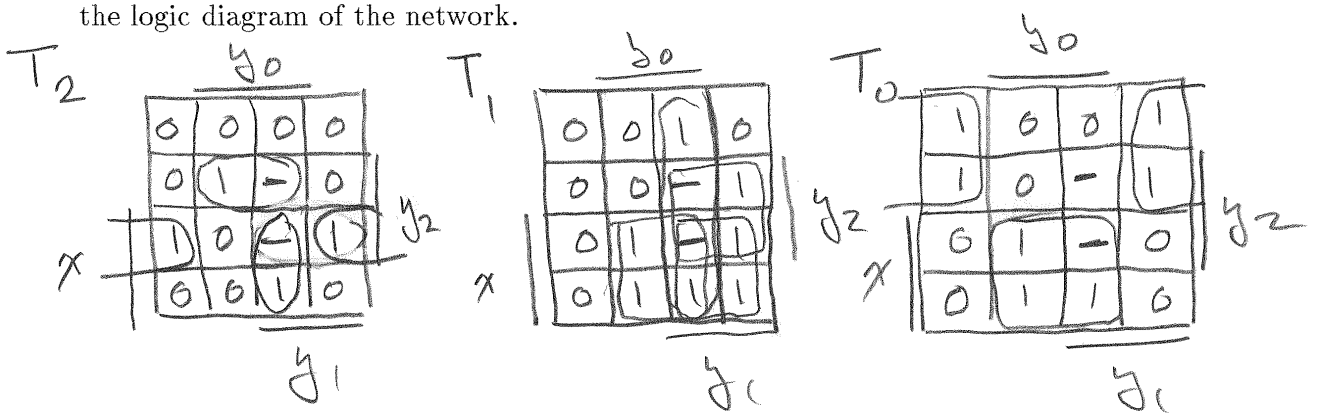
State	Sequence
S_0	start
S_1	0
S_2	01
S_3	010
S_4	0101
S_5	01010
S_6	010101

b) [4 points] Encode these states using three state variables (y_2, y_1, y_0) so that the state assignment of state S_i is the radix-2 representation of i. Complete the state and transition table:

	PS	Input		Input	
	$y_2y_1y_0$	$x=0$	$x=1$	$x=0$	$x=1$
S_0	000	000,0	000,0	000	000
S_1	001	001,0	010,0	000	011
S_2	010	011,0	000,0	001	010
S_3	011	001,0	100,0	010	111
S_4	100	101,0	000,0	001	100
S_5	101	001,0	110,0	100	011
S_6	110	101,0	000,1	011	110
		$Y_2Y_1Y_0, z$		$T_2T_1T_0$	

S_0	S_1	S_3	S_2
S_4	S_5	S_7	S_6
S_0	S_1	S_3	S_2

c) [6 points] Implement the network using NAND gates and T flip-flops. Indicate the T inputs in the state table. Give minimal sum of products expressions for T inputs. Show the logic diagram of the network.

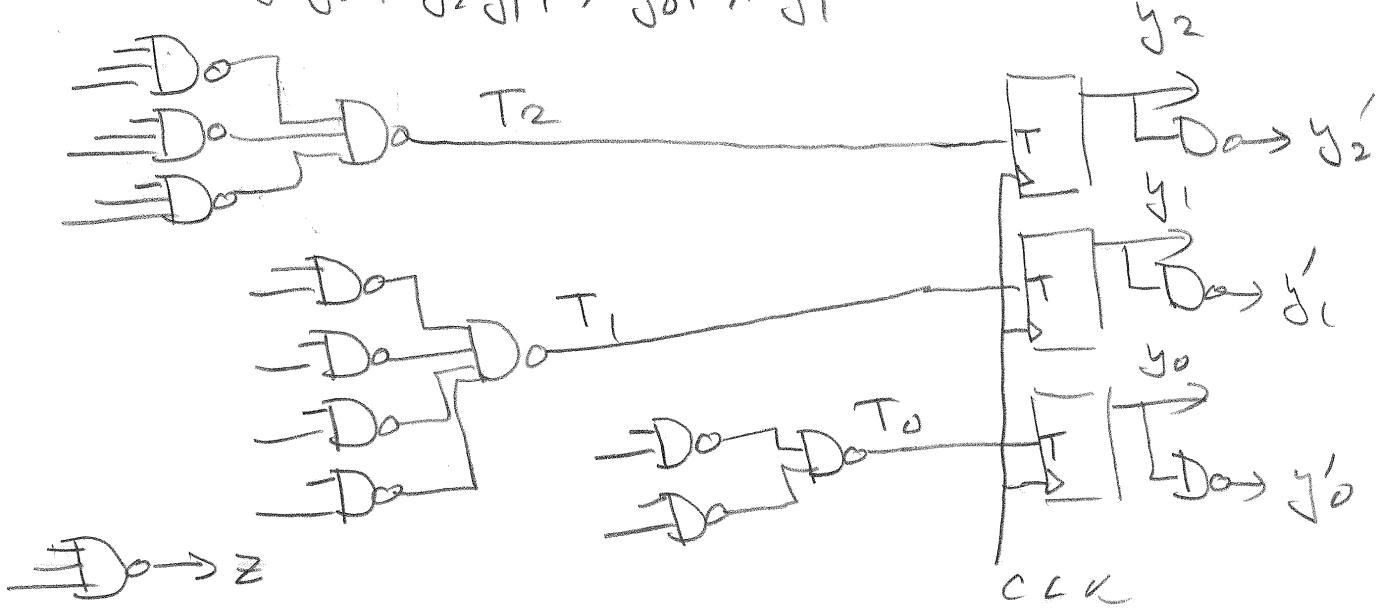


$T_2 = x\,y_2\,y_0' + x\,y_1\,y_0 + x'\,y_2\,y_0$

$T_1 = y_1\,y_0 + y_2\,y_1 + x\,y_0 + x\,y_1$

$T_0 = x'\,y_0' + x\,y_0$

$z = x\,y_1\,y_2$



d) [4 points] If the propagation delays are $t_p = 3.5ns$, $t_{su} = 0.9ns$, $t_{NAND} = 2ns$, $t_{in} = 1.5ns$, and $t_{out} = 2.5ns$, determine the maximum clock frequency.

$$T_{min} = max\left[(t_{in} + t_{su}^{x}(net)),\ (t_p(cell) + t_{su}^{y}(net)),\ (t_p(net) + t_{out})\right]$$

$$t_{su}^{x}net = 2.2 + 0.9 = 4.9\,ns$$

$$t_{su}^{y}net = 3.2 + 0.9 = 6.9\,ns$$

$$t_p(net) = 3.5 + 2 = 5.5\,ns$$

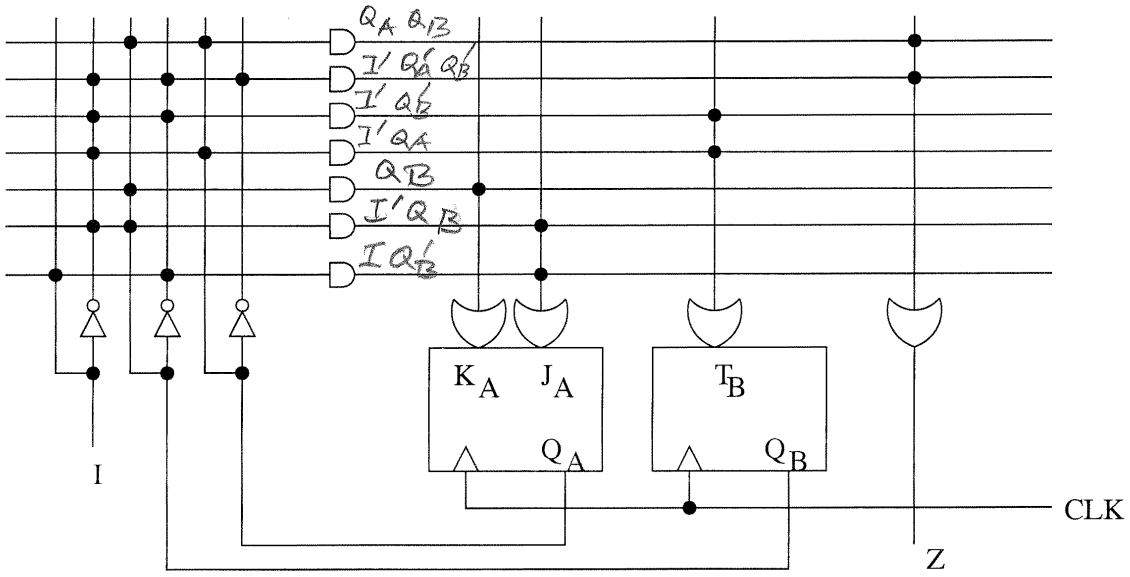
$$T_{min} = max\left[(1.5 + 4.9),\ (3.5 + 6.9),\ (5.5 + 2.5)\right]$$

(6.9 over 4.9; 10.4 over 6.9; 8 over 5.5 + 2.5)

$$= 10.4\,ns$$

$$f_{max} = \frac{1}{10.4 \times 10^{-9}} \approx 100\,MHz$$

Problem 2. (10 points) Derive the state transition/output table for the implementation of the sequential system shown in the figure below. The next state and output functions are implemented by a PLA structure. The machine has one input I and one output Z. Show expressions for the flip-flop inputs. Show the state transition/output table.



$J_A = I'Q_B + IQ_B' = I \oplus Q_B$

$K_A = Q_B$

$T_B = I'(Q_A + Q_B')$

$z = I'Q_A'Q_B' + Q_A Q_B$

PS(Q_AQ_B)	I	J_A	K_A	T_B	NS	Z
00	0	0	0	1	01	1
00	1	1	0	0	10	0
01	0	1	1	0	11	0
01	1	0	1	0	01	0
10	0	0	0	1	11	0
10	1	1	0	0	10	0
11	0	1	1	1	00	1
11	1	0	1	0	01	1

Problem 3. (14 points)

(a) [8 points] Design a cyclic counter with the output sequence $0, 1, 4, 7, 6, 3, 0, 1, \ldots$ (of period 6) using JK flip-flops and AND, OR, NOT gates as needed. Assume that the input x is always 1. Select a state assignment that is the same as the coding for the output, that is $z(t) = s(t)$. Show the state/output table. Minimize all expressions. Show the logic diagram of the counter.

State/output table:

PS	NS
S_0	S_1
S_1	S_4
S_4	S_7
S_7	S_6
S_6	S_3
S_3	S_0

PS $Q_2\ Q_1\ Q_0$	NS $Q_2\ Q_1\ Q_0$
0 0 0	0 0 1
0 0 1	1 0 0
1 0 0	1 1 1
1 1 1	1 1 0
1 1 0	0 1 1
0 1 1	0 0 0

JK:

PS \ NS	0	1
0	0–	1–
1	–1	–0

J K

S_2, S_5 – d.c.

J_2

Q2 \ Q0	0	1	0	–
Q2	–	–	–	–

Q1

J_1

Q2 \ Q0	0	0	–	–
Q2	1	–	–	–

Q1

J_0

Q2 \ Q0	1	–	–	–
Q2	1	–	–	1

Q1

K_2

Q2 \ Q0	–	–	–	–
Q2	0	–	0	1

Q1

K_1

Q2 \ Q0	–	–	1	–
Q2	–	–	0	0

Q1

K_0

Q2 \ Q0	–	1	1	–
Q2	–	–	1	–

Q1

$J_0 = 1$

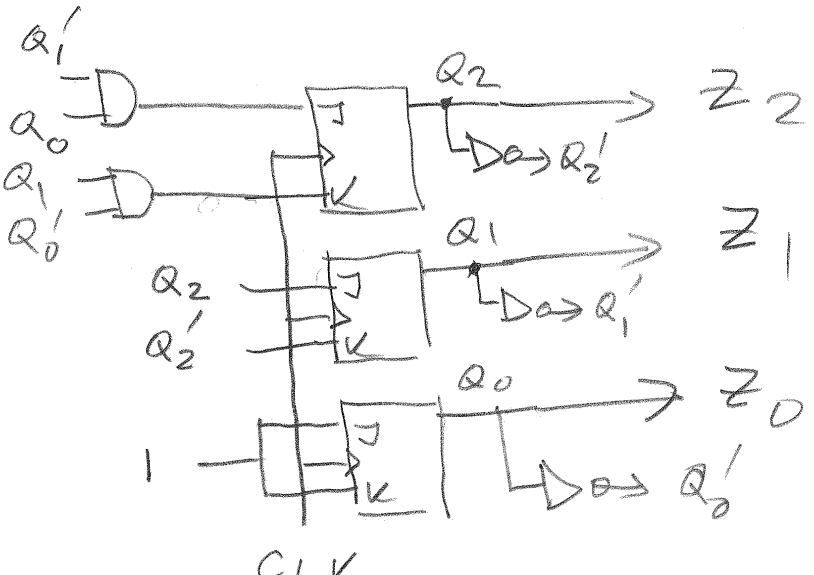
$K_0 = 1$

$J_1 = Q_2$

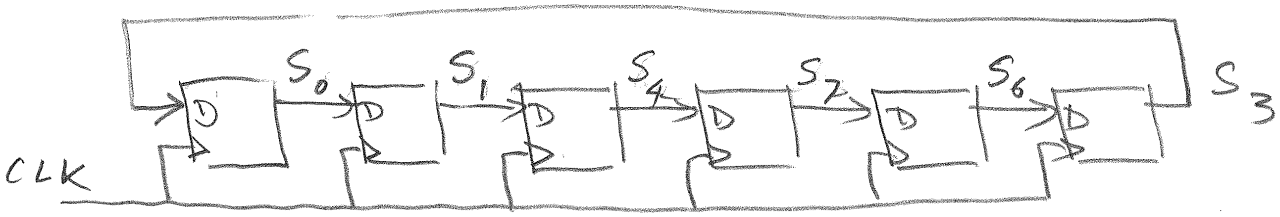
$K_1 = Q_2'$

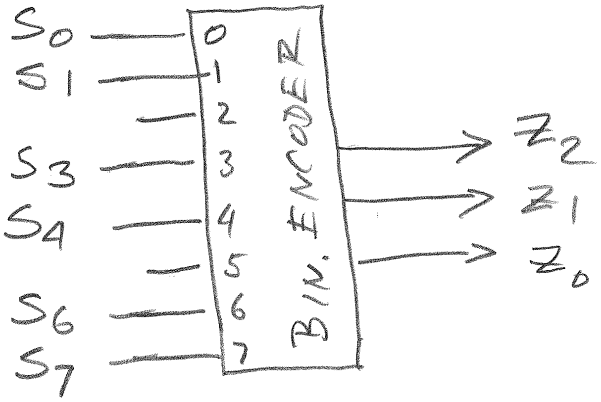
$J_2 = Q_1' Q_0$

$K_2 = Q_1 Q_0'$

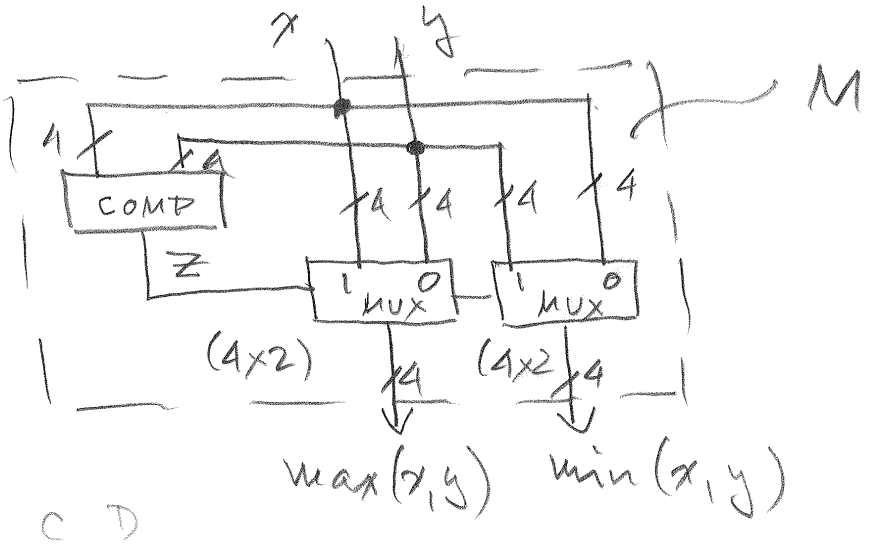


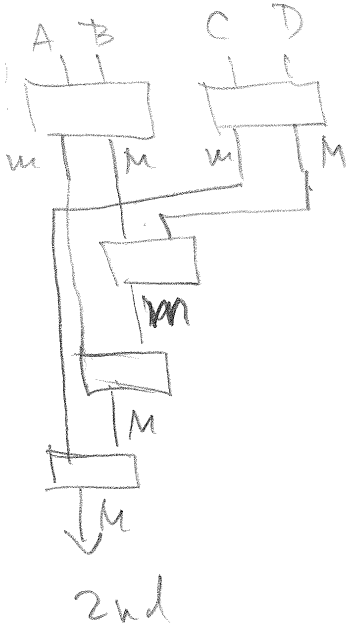
(b) [6 points] Design the cyclic counter defined in part (a) using the "one flip-flop per state" approach with D flip-flops. To obtain the output, use a suitable standard combinational module - do not design a gate network! Show all connections. Show the initial state of this implementation.

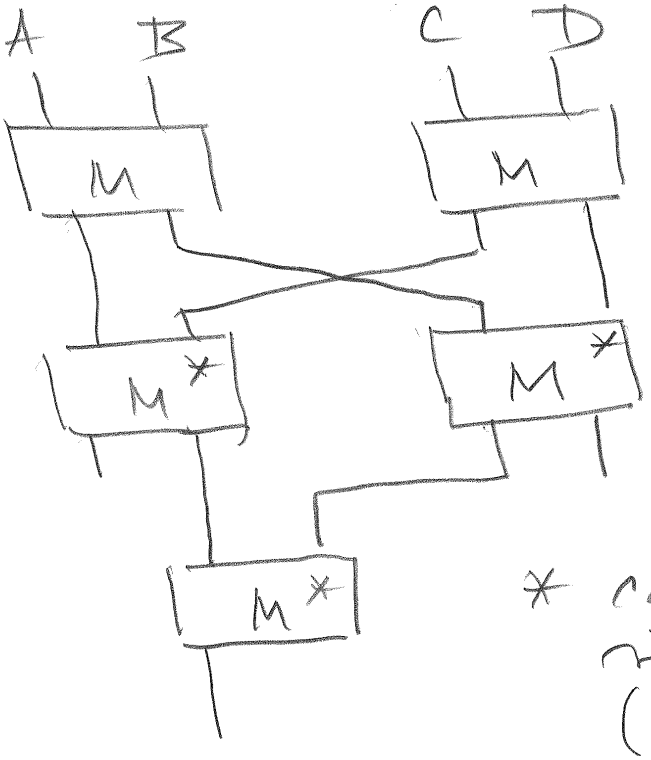




Problem 4. (12 points) Design a hierarchical combinational network that finds the second largest of four nonnegative integers A, B, C, D. Each integer is represented by four bits. You may use only the following module types: 4×2-input multiplexer and four-bit comparator. The single-bit output of the comparator is z. If the first integer is larger than the second, the output is $z = 1$. Otherwise, $z = 0$. Define first your basic module and then design the network using your module. Indicate all inputs and connections on the modules being used.







* can be simplified (eliminate one 4x2 MUX)

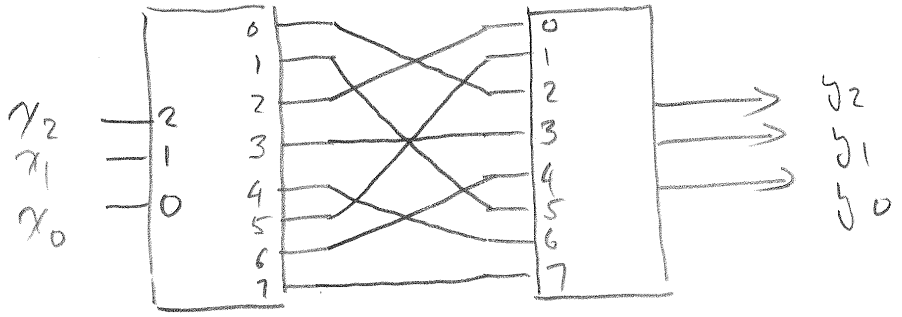
Problem 5. (8 points) Implement the following systems using standard combinational modules (no gate networks allowed):

Input: $x \in \{0,1,2,3,4,5,6,7\}$, represented in binary by $\underline{x} = \{x_2, x_1, x_0\}, x_i \in \{0,1\}$.

Output: $y \in \{0,1,2,3,4,5,6,7\}$, represented in binary by $\underline{y} = \{y_2, y_1, y_0\}, y_i \in \{0,1\}$

Function: $y = (3x + 2) \bmod 8$

x	0	1	2	3	4	5	6	7
y	2	5	0	3	6	1	4	7



Problem 6. (13 points)

a) [8 points] Complete the following table. If an entry in the table cannot be filled properly, explain why and how to fix it. Representation values are given in the decimal number system.

Number system	Number of digits n	Signed integer x	Representation value x_R	Digit-vector X
2's compl.	7	-35	93	1011101
1s' compl.	8	-86	169	10101001
2's compl.	9	-218	294	100100110
2's compl.	6	-33	—	—

↑ requires $n = 7$

b) [5 points] Compute $z = a + 2b - c$ in 2's complement for $a = -9$, $b = 17$, and $c = -77$. Perform calculations on bit-vectors representing a, b and c and show every step of your work. How many bits should z have to represent the correct result? Check your work by showing, for each step, the corresponding values in decimal number system.

$z = -9 + 34 + 77 = 102$

in 2's complement $\Rightarrow$ 8 bits

$a = -9$ 11110111

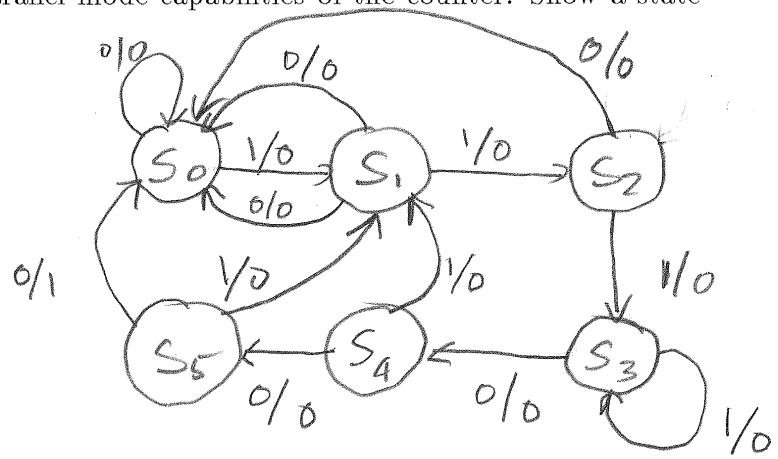
$2b = 34$ 00100010

$-c = 77$ 01001101

102 01100110

Problem 7. (13 points) Design a sequential system specified by the following state transition and output table using a modulo-8 counter with parallel load as the state register, a 8-to-1 multiplexer for the CNT input and NAND gates. Assume LD = CNT'. The design must take advantage of the count and parallel mode capabilities of the counter. Show a state diagram and all your work.

	PS $Q_2Q_1Q_0$	Input $x=0$	Input $x=1$
S_0	000	000,0	001,0
S_1	001	000,0	010,0
S_2	010	000,0	011,0
S_3	011	100,0	011,0
S_4	100	101,0	001,0
S_5	101	000,1	001,0
		NS, z	NS, z



$CNT = S_0x + S_1x + S_2x + S_3x' + S_4x'$

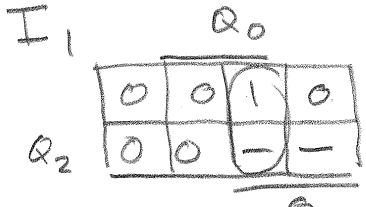
$LD = CNT'$

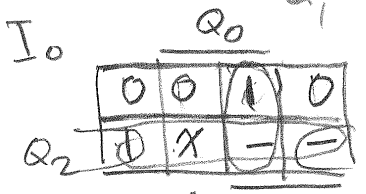
$I_2 I_1 I_0$

0 0 0 if $S_0 + S_1 + S_2 + S_5x'$

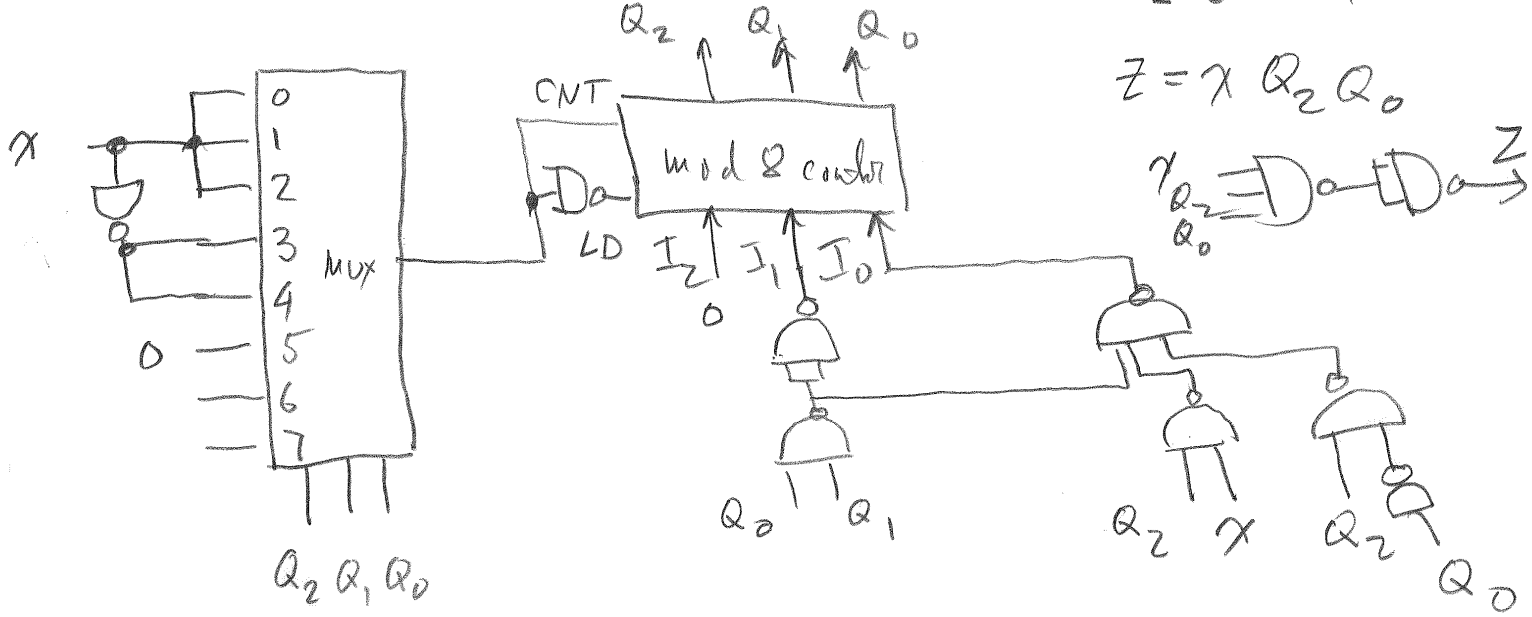
0 0 1 if $S_4 + S_5x$

0 1 1 if S_3





$I_2 = 0 \quad I_1 = Q_0Q_1 \quad I_0 = Q_0Q_1 + Q_2x + Q_2Q_0'$



Problem 8. (10 points) Design a sequential system using combinational and sequential standard modules that detects when $x(t-7, t-4) < x(t-3, t)$, where four-bit input sequences are interpreted as positive integers.