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CS220 Computer Architecture

Practical 4 Report

Part A

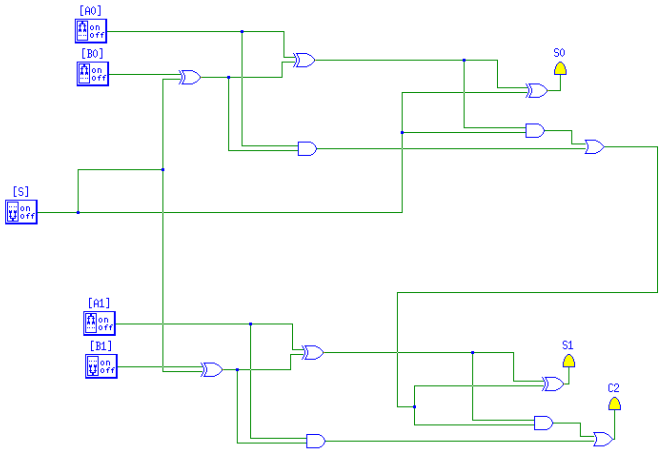
a. *Construct a 2–bit adder circuit by composing two 1–bit adders with additional logic so that it can act both as a 2–bit adder and as a 2–bit subtractor. Use the 5 gate adder design seen already for each 1–bit adder.*

b. *The relevant truth table used in deriving the circuit*

When S = 0, the circuit is an adder; When S = 1, the circuit is a subtractor.

B		A		S=0			S=1		
B1	B0	A1	A0	C2	S1	S0	C2	S1	S0
0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	1	0	0	1	0
1	0	0	0	0	1	0	0	1	0
1	1	0	0	0	1	1	0	0	1
0	0	0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1	0	0
1	0	0	1	0	1	1	0	1	1
1	1	0	1	1	0	0	1	0	0
0	0	1	0	0	1	0	1	1	0
0	1	1	0	0	1	1	1	0	1
1	0	1	0	1	0	0	1	0	0
1	1	1	0	1	0	1	1	1	0
0	0	1	1	0	1	1	1	1	1
0	1	1	1	1	0	0	1	1	0
1	0	1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	1	0	0

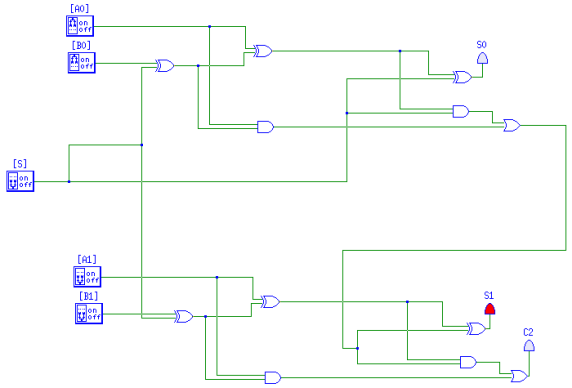
c. *Implement the function on the simulator*



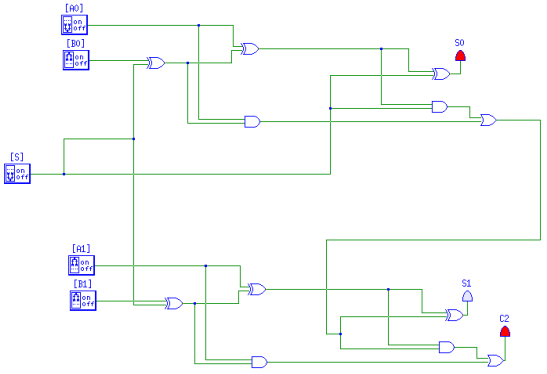
d. *Verification of Experiment and Observations*

The circuit worked in accordance with the truth table for all input combinations.

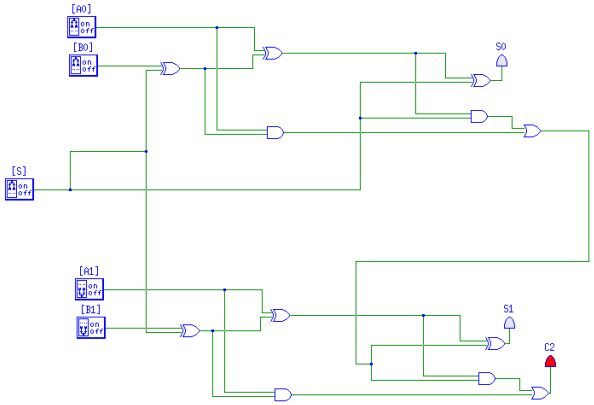
e.g.,1 S=0; B1=0,B0=1,A1=0,A0=1; C2=0,S1=1,S0=0



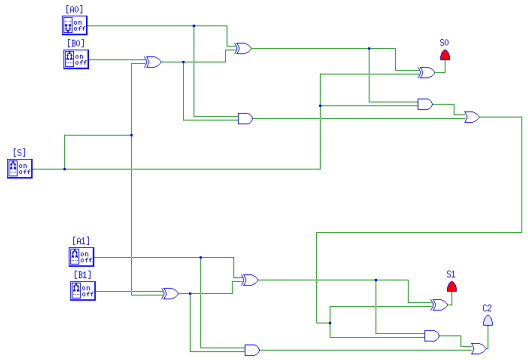
e.g.,2 S=0; B1=1,B0=1,A1=1,A0=0; C2=1,S1=0,S0=1



e.g.,3 S=1; B1=0,B0=1,A1=0,A0=1; C2=0,S1=0,S0=1



e.g.,4 S=1; B1=1,B0=1,A1=1,A0=0; C2=0,S1=1,S0=1



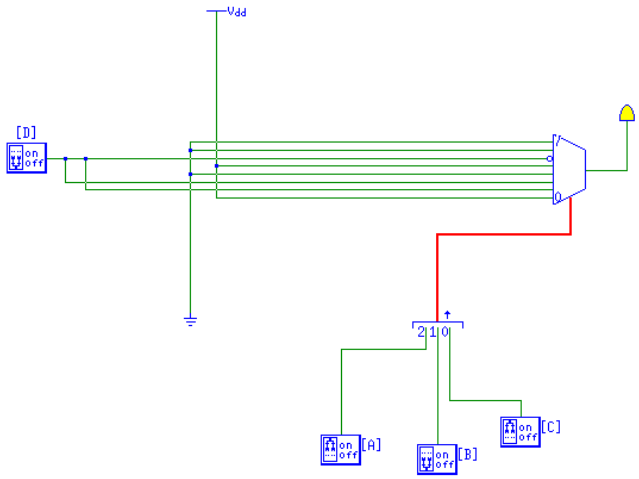
Part B

a. *Implement the four variable switching function* $f(A,B,C,D) = \sum m(0,4,5,8,9,10,12)$ *using an 8–1 Multiplexer. The four variables should be represented as switches. Three switches (A,B,C) will be connected to the control inputs of the multiplexer. The eight inputs to the multiplexer will be connected in turn either to logic 0 (GND), logic 1 (Vdd), Switch D or the complement of switch D as determined from the function output requirements. Switches representing A,B and C can be connected to the wire merge device ports 2,1 and 0 respectively*

b. *The relevant truth table used in deriving the circuit*

Control Inputs			Data Input			
A	B	C	D′	D		
0	0	0	1	0	D0	1/Vdd
0	0	1	0	0	D1	D
0	1	0	1	1	D2	D
0	1	1	0	1	D3	0/GND
1	0	0	1	1	D4	1/Vdd
1	0	1	1	0	D5	D′
1	1	0	0	1	D6	0/GND
1	1	1	0	0	D7	0/GND

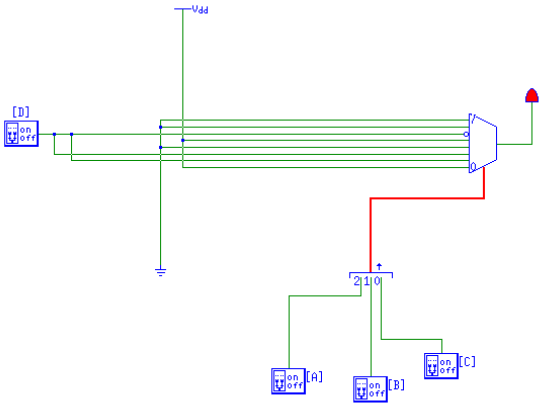
c. *Implement the function on the simulator*



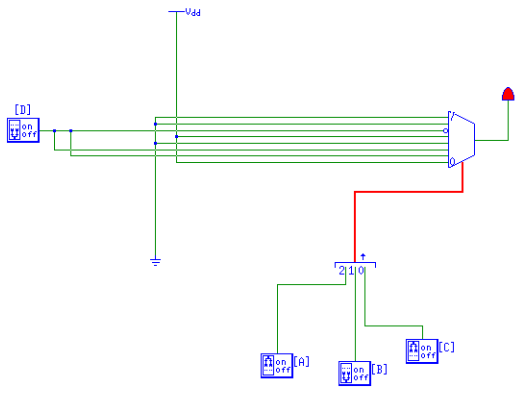
d. *Verification of Experiment and Observations*

The circuit worked in accordance with the truth table for all input combinations.

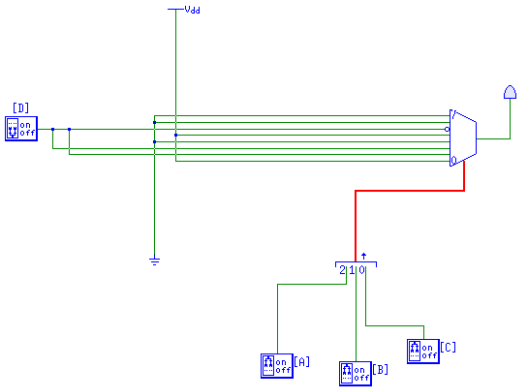
e.g.,1 m_0: *DCBA=0000, f=1*



e.g.,1 m_5: *DCBA=0101, f=1*



e.g.,3 m_7: *DCBA=0111, f=0*



e.g.,4 m_{13}: *DCBA=1101, f=0*