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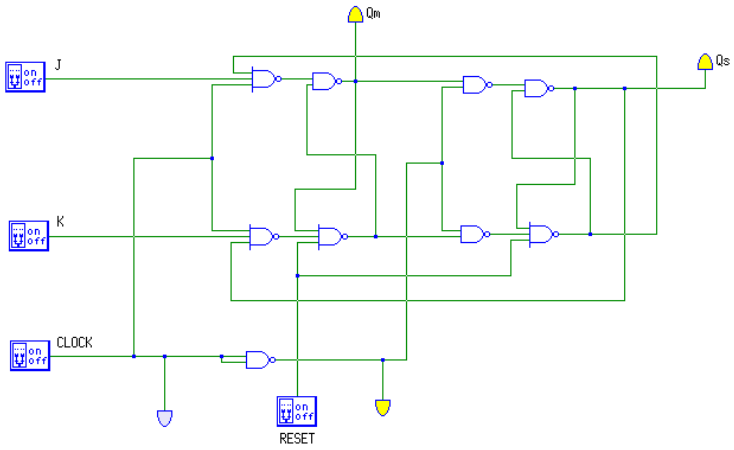
FZU ID	832103316

CS220 Computer Architecture

Practical 5 Report

Part A

a. *Implement a Master–Slave J–K flip–flop circuit on the simulator.*



b. *The flip–flop obeys the truth table given below.*

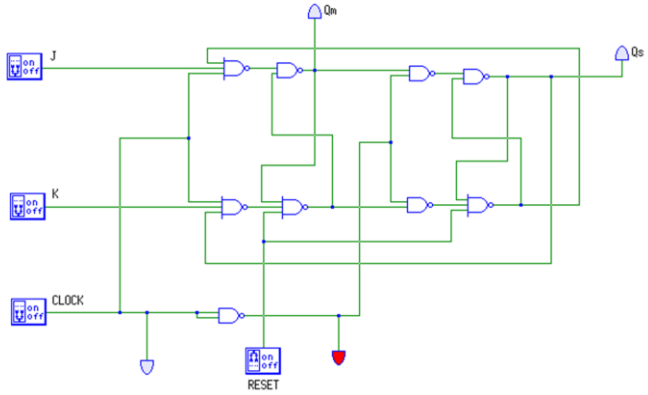
J	K	Qn	Qn+1	Description
0	0	0	0	No change
		1	1	
0	1	0	0	Reset
		1	0	
1	0	0	1	Set
		1	1	
1	1	1	0	Toggle
		0	1	

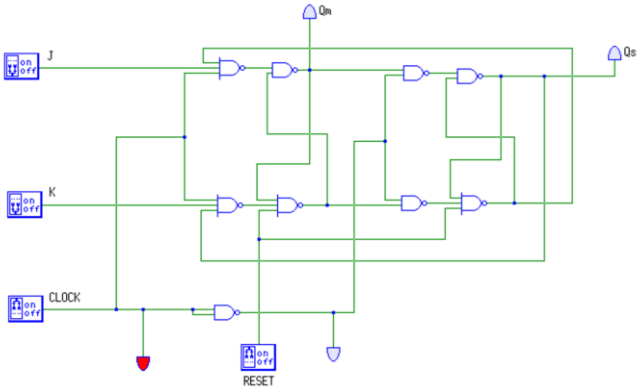
c. ***Verification of Experiment and Observations***

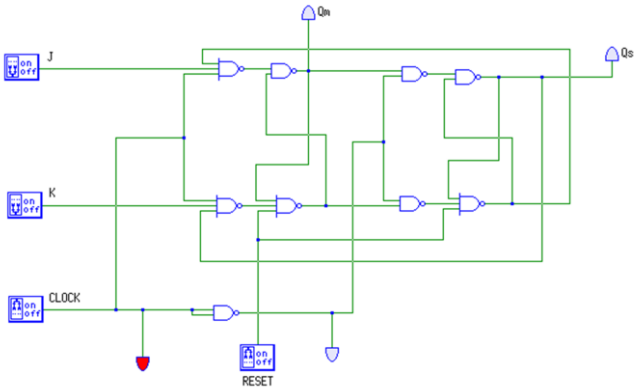
The three screenshots in one case corresponds to the change of Q during one clock pulse period.

J = 0, K = 0

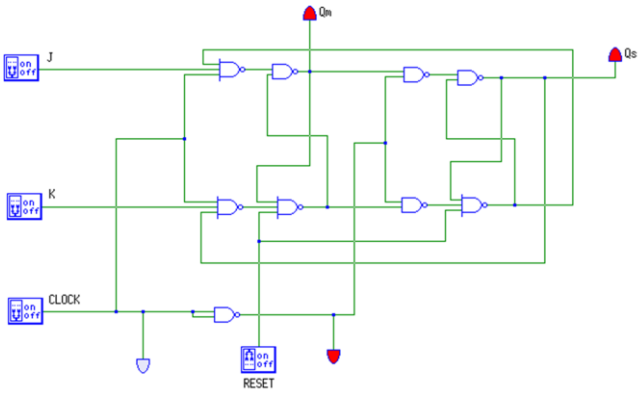
Q = 0 , Qn+1 = 0

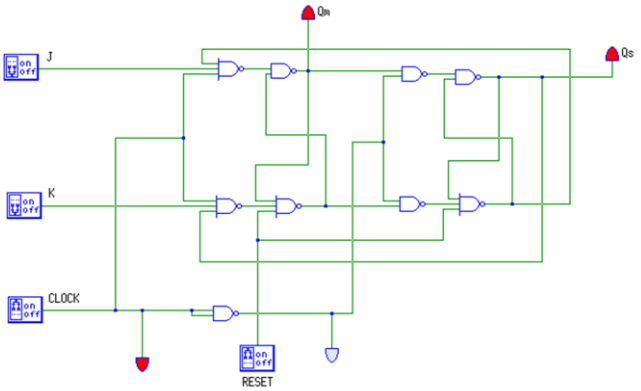


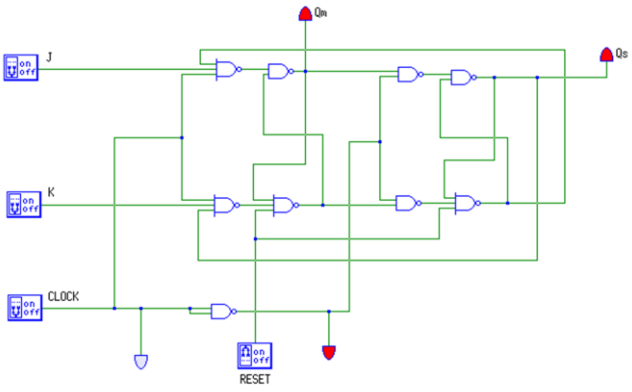




Q = 1 , Qn+1 = 1

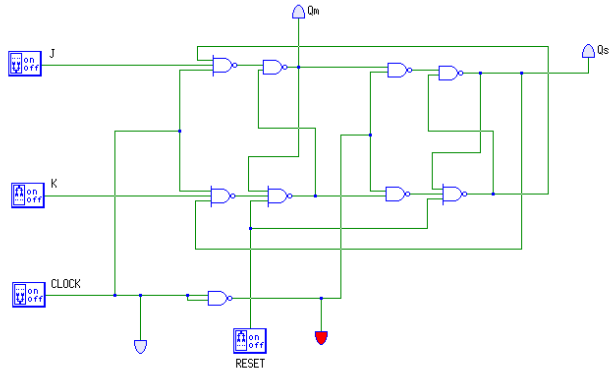


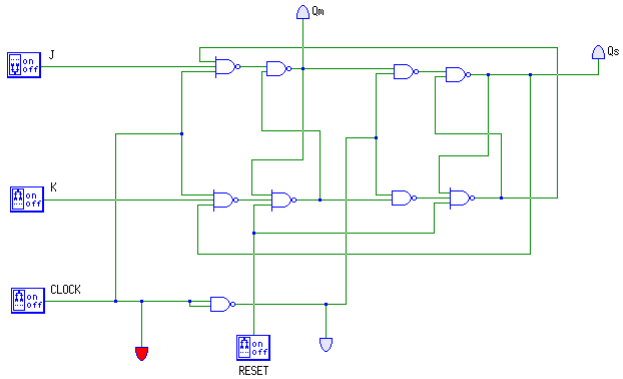


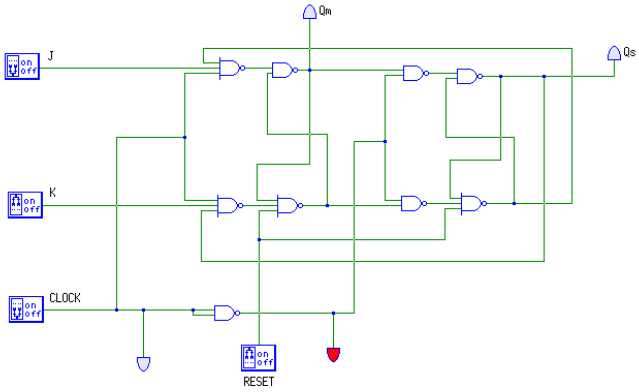


J = 0, K = 1

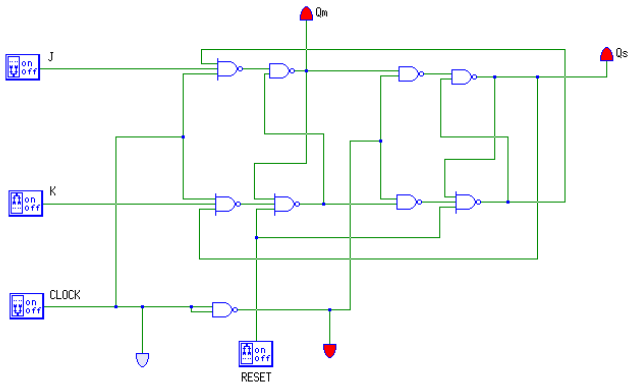
Q = 0 , Qn+1 = 0

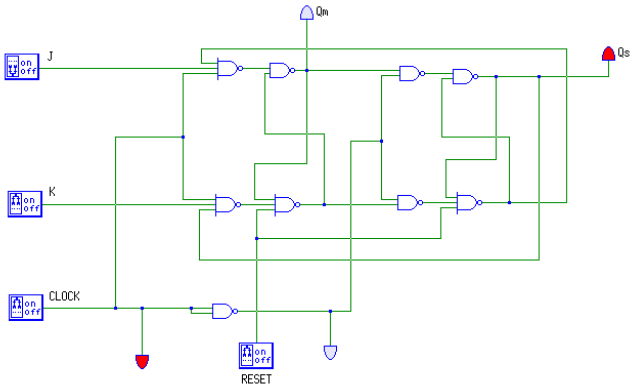


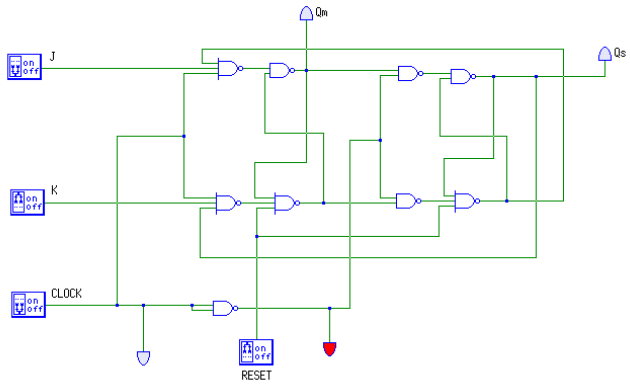




Q = 1 , Qn+1 = 0

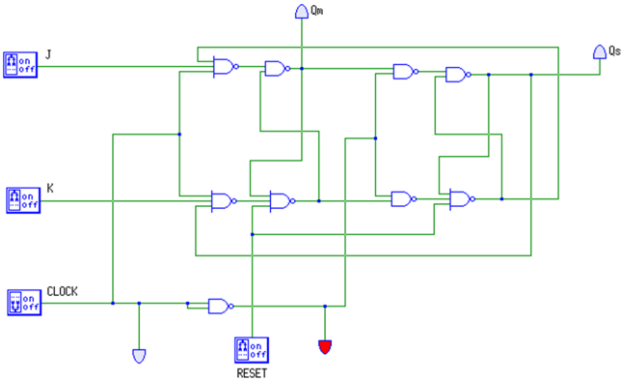


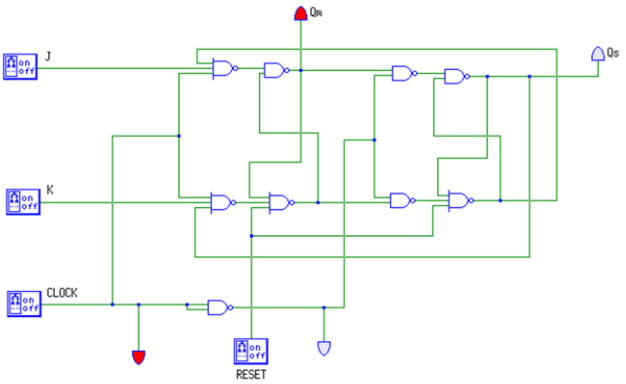


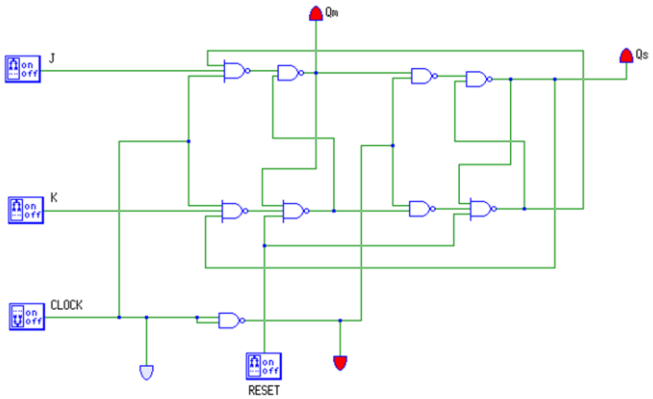


J = 1, K = 0

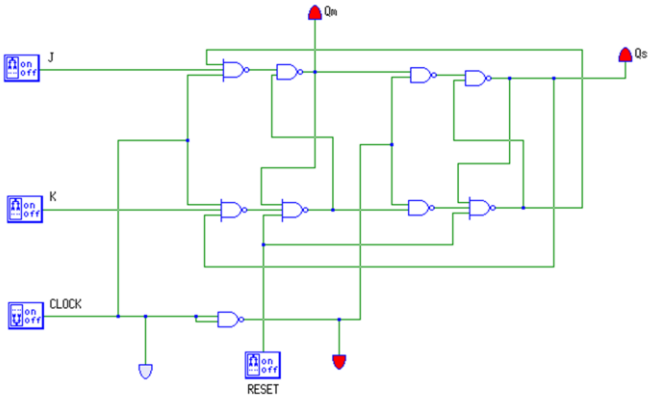
Q = 0 , Qn+1 = 1

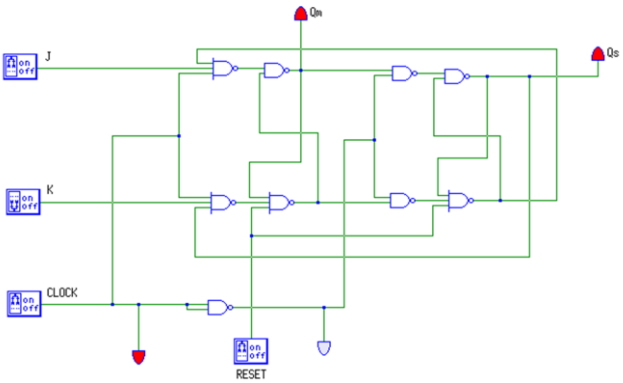


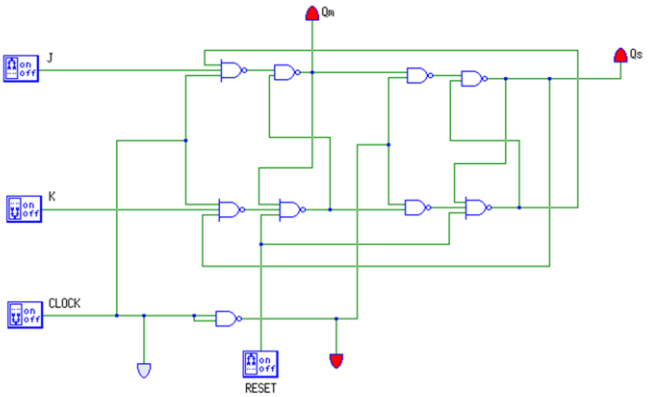




Q = 1 , Qn+1 = 1

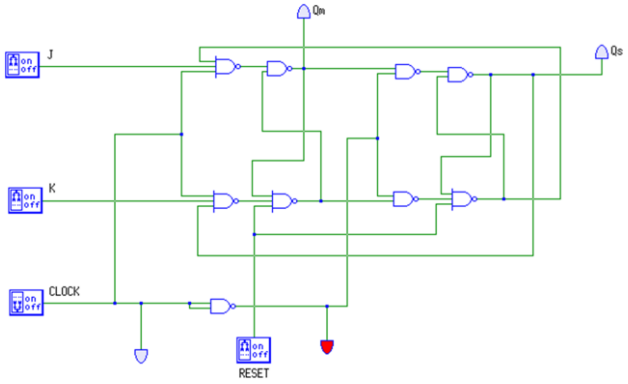


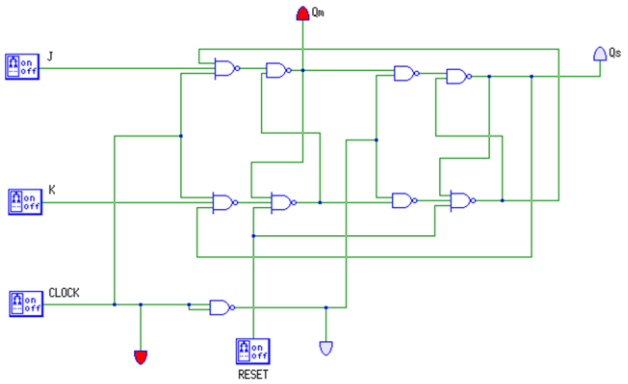


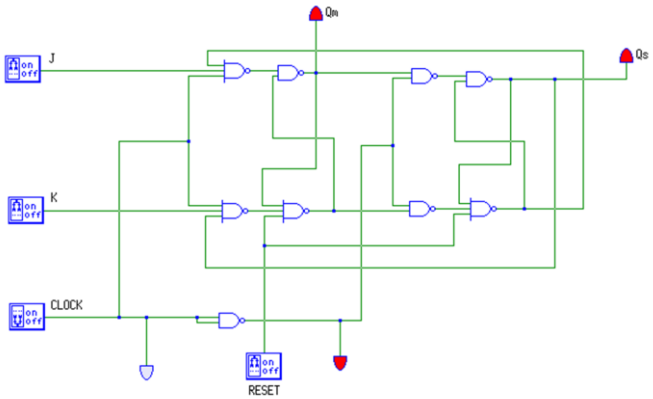


J = 1, K = 1

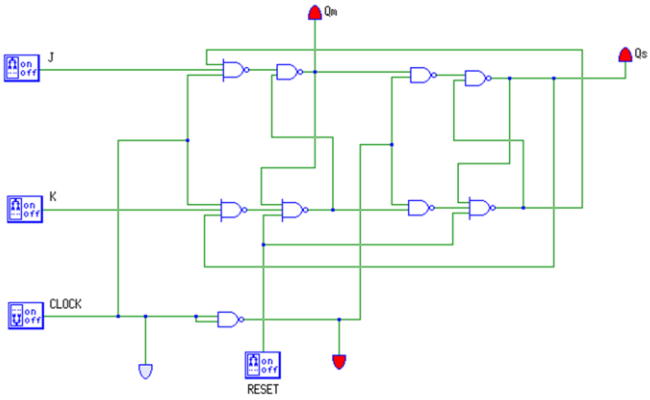
Q = 0 , Qn+1 = 1

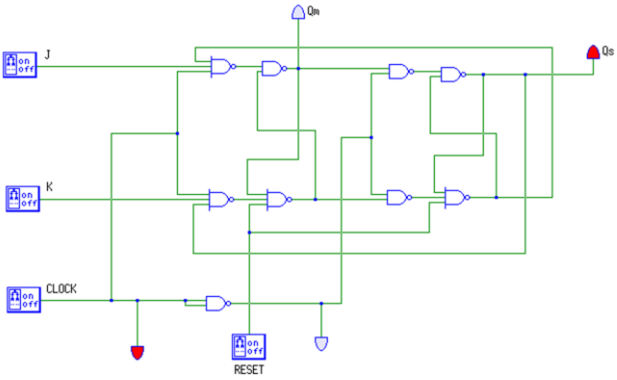


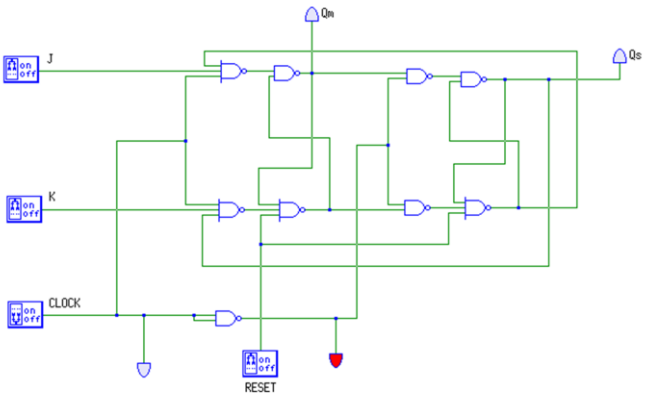




Q = 1 , Qn+1 = 0



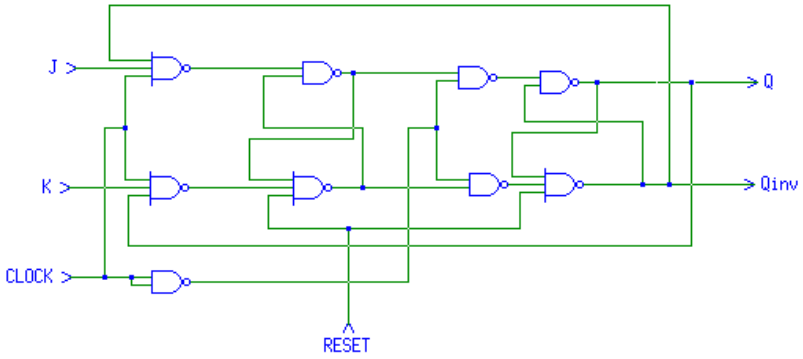




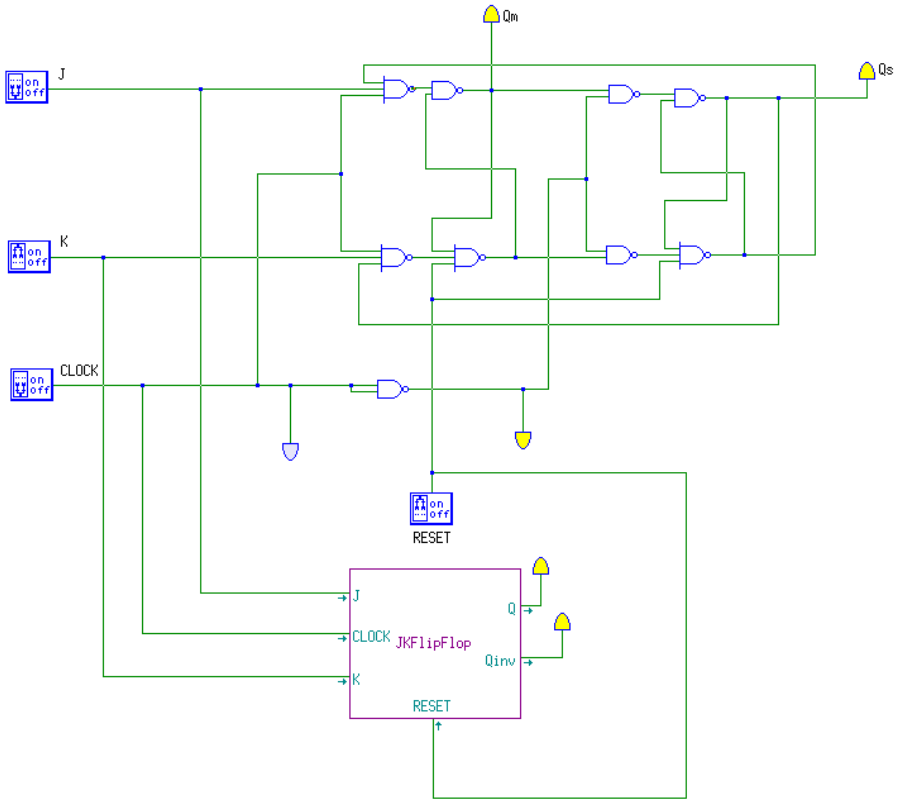
Part B

a. *Construct a Master–Slave J–K flip–flop circuit Modules in TKGate.*

b. *Edit Module Implementations.*



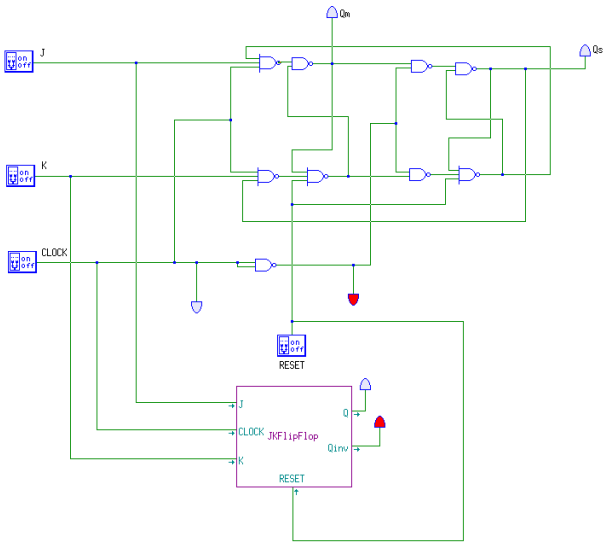
c. *Use User Defined Modules combined with the circuit used in part A.*



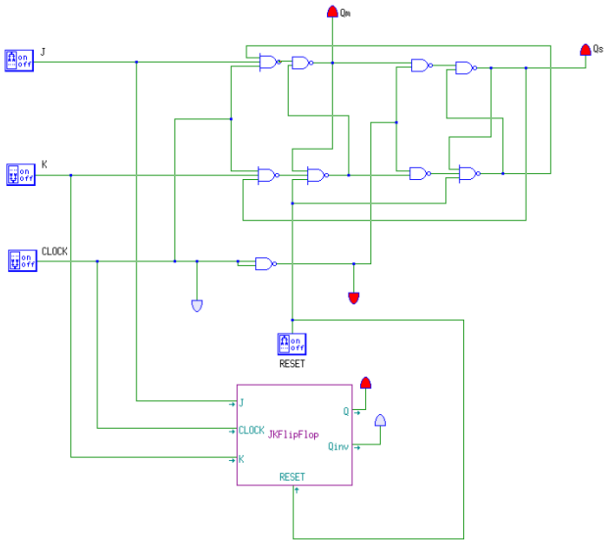
d. ***Verification of Experiment and Observations***

The flip–flop Qs is as the same as the module Q output for different input combinations. Here are two examples in all cases.

e.g.,1 J = K = 0, Q = Qs = 0

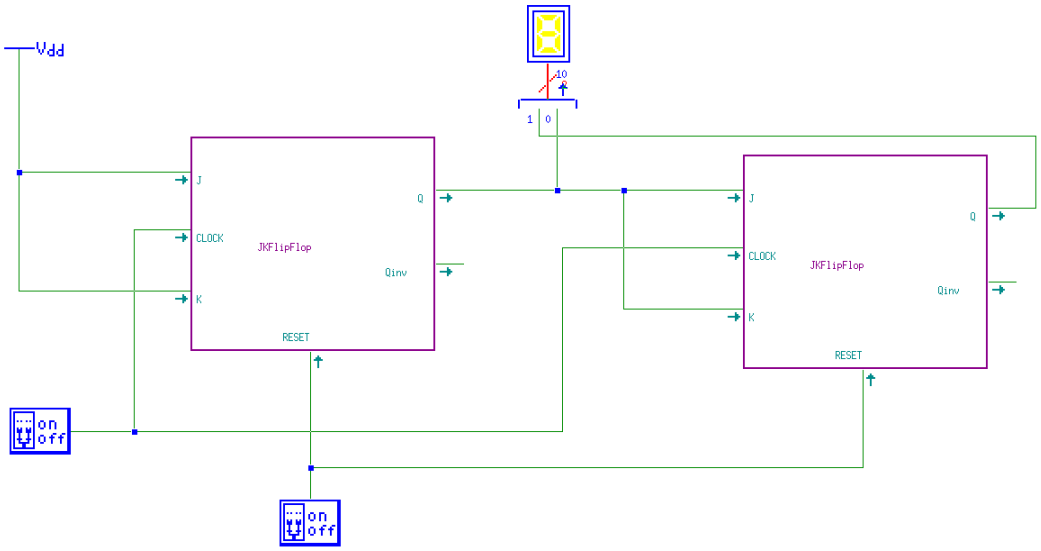


e.g.,2 J = 1, K =0, Q = Qs = 1



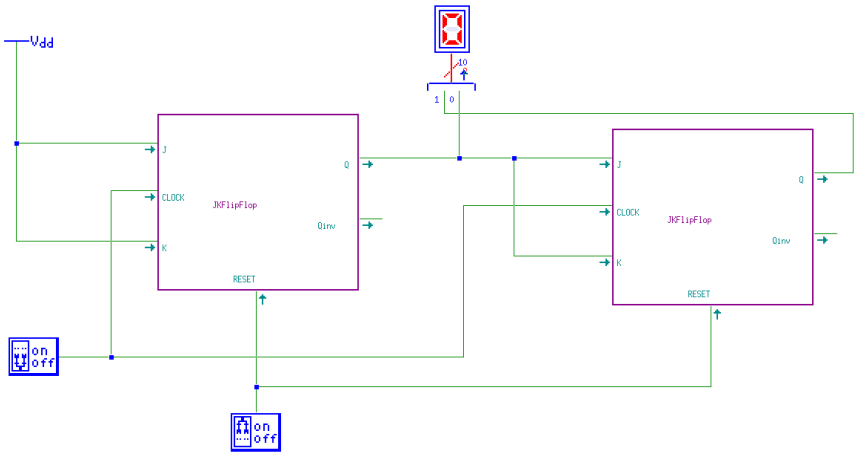
Part C

a. *Implement a 2–bit synchronous counter using two instances of the module used in part B. The output of the counter should be displayed on a decimal counter.*

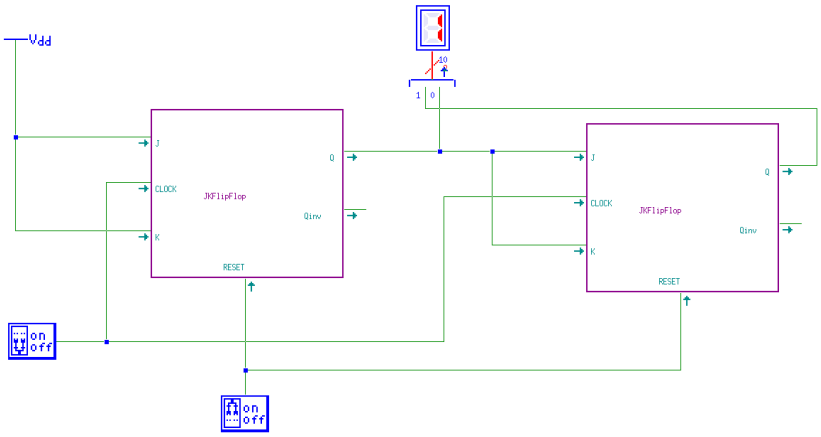


b. ***Verification of Experiment and Observations***

Count = 0



Count = 1



Count = 2