1 LABORATION 1 - COMBINATORIAL CIRCUITS

In the laboration, we build the first component of the microprocessor, the ALU. We will describe the design using RTL-modelling in System Verilog. We also exercise how to build a basic testbench to check its functionality.

The lab only requires simulation in Questasim, Modelsim or other HDL simulation tool.

1.1 TASKS

To complete this lab you must successfully complete the following tasks:

1) Build an RTL model of the ALU. The definition of the module is given in the file `ALU.sv`. The ALU should use 2's complement arithmetic. The implementation has to follow the schematic shown in figure 1.1.

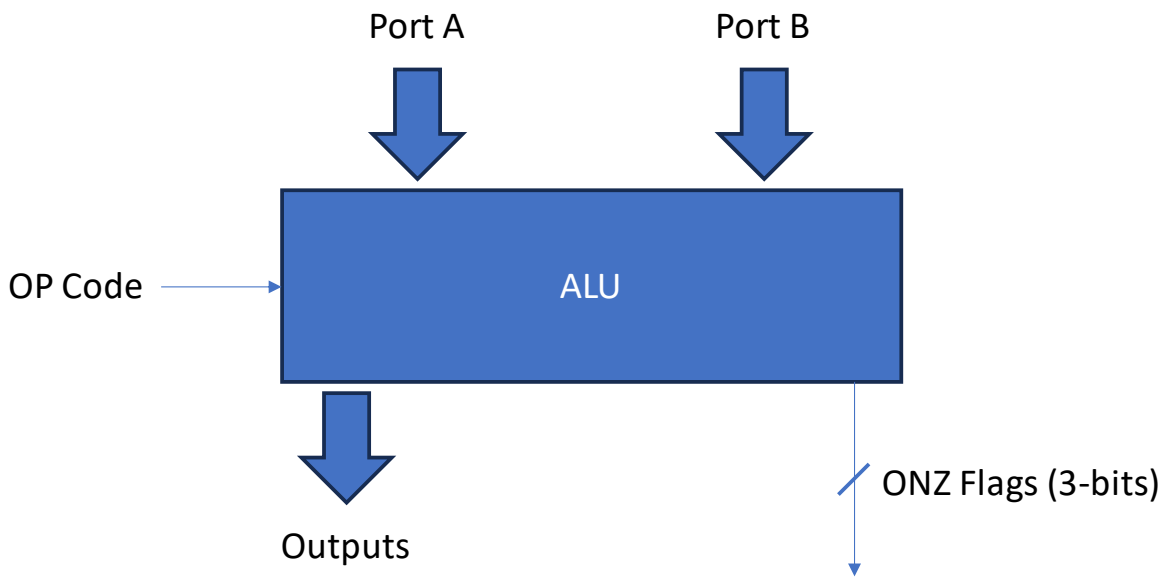

FIGURE 1.1. ALU SCHEMATIC.

2) The ALU should implement the following functions:

Operation		Outputs	Flags		
Name	Code	Y	O	N	Z
ADD	000	A+B	Is active (=1) if the result of an ADD- or SUB- operation gives the wrong sign bit on Y.	Is active (=1) if the result on Y is negative.	Is active (=1) if the all bits in Y are 0.
SUB	001	A-B			
AND	010	A AND B			
OR	011	A OR B			
XOR	100	A XOR B			
INC	101	A+1			
MOVA	110	A			
MOVB	111	B			

3) The ALU has two generic inputs A and B (n-bit), one OP code input (3 bits)

4) The ALU has 1 generic n-bit output and a 3-bit flag output ONZ **(**make sure that you use the specific order, O is the MSB and Z is the LSB**)**

5) Build a testbench that verifies the functionality of the ALU.

1) The testbench has to check all possible functions of the ALU.

2) A skeleton for the ALU testbench is given in the file `ALU_tb.sv`

3) Use randomized inputs to test your design.

4) Create an automatic check to make sure that all functions are working correctly.

1.2 DELIVERABLES:

1) All your files describing the ALU design

2) All your files that implement your testbench