

16 June 2014 -- Computer Architectures -- part 2/2

Name, Student ID

Question 1

Considering the following processor architecture for a superscalar MIPS64 processor implemented with multiple-issue and speculation:

- issue 2 instructions per clock cycle
 - jump instructions require 1 issue
 - handle 2 instructions commit per clock cycle
 - timing facts for the following separate functional units:
 - i. 1 Memory address 1 clock cycle
 - ii. 1 Integer ALU 1 clock cycle
 - iii. 1 Jump unit 1 clock cycle
 - iv. 1 FP multiplier unit, which is pipelined: 12 stages
 - v. 1 FP divider unit, which is not pipelined: 12 clock cycles
 - vi. 1 FP Arithmetic unit, which is pipelined: 4 stages
 - Branch prediction is always correct
 - There are no cache misses
 - There are 2 CDB (Common Data Bus).
- Complete the table reported below showing the processor behavior for the 2 initial iterations of the reported loop-based program.

# iteration		Issue	EXE	MEM	CDB x2	COMMIT x2
1	l.d f1,v1(r1)	1	2m	3	4	5
1	l.d f2,v2(r1)	1	3m	4	5	6
1	div.d f4,f1,f2	2	6d		18	19
1	s.d f4,v4(r1)	2	4m			19
1	l.d f3,v3(r1)	3	5m	6	7	20
1	mul.d f5,f3,f4	3	19x		31	32
1	s.d f5,v5(r1)	4	6m			32
1	daddi r2,r2,-1	4	5i		6	33
1	add.d f6,f4,f5	5	32		36	37
1	s.d f6,v6(r1)	5	7m			37
1	daddui r1,r1,8	6	7i		8	38
1	bnez r2,loop	7	8j			38
2	l.d f1,v1(r1)	8	9m	10	11	39
2	l.d f2,v2(r1)	8	10m	11	12	39
2	div.d f4,f1,f2	9	18d		30	40
2	s.d f4,v4(r1)	9	11m			40
2	l.d f3,v3(r1)	10	12m	13	14	41
2	mul.d f5,f3,f4	10	31x		43	44
2	s.d f5,v5(r1)	11	13m			44
2	daddi r2,r2,-1	11	12i		13	45
2	add.d f6,f4,f5	12	44		48	49
2	s.d f6,v6(r1)	12	14m			49
2	daddui r1,r1,8	13	14i		15	50
2	bnez r2,loop	14	15j			50

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Question 2

Considering a (2,2) correlating predictor of 1K entries, and assuming that the processor executes the following code fragment, determine the BPU final state and calculate the final misprediction ratio in the presented case. The BPU initial state is indicated in the table.

General assumptions:

- R10 is the main loop control register and it is initialized to 100, then, the program iterates 100 times.
- R3 is the reference value, set to 1
- R2 is the input register
 - o the input value for R2 is the sequence of the first 100 even numbers starting from 0 in the first iteration, to 198 during the last iteration, i.e., [0,2,4,6,8,... 198]
- The initial value of the BPU 2-bit shift register is **11**
- The initial value of every predictor is provided in the table in the 2-bit predictors columns
- The grayed instructions in the program do not contain any branch or jump instruction

Address	Instruction	2-bit predictors				2-bit shift register	misprediction counting
		00	01	10	11		
0x0000	L0: ...	2	2	2	2		
...	; Reading input values in R2	2	2	2	2		
0x0020	AND R1, R2, R3	2	2	2	2		
0x0024	BEQZ R1, L1	2	2	2	2	11	
0x0028	...	2	2	2	2		
0x002C	L1: XOR R4, R1, R3	2	2	2	2		
0x0030	BEQZ R4, L2	2	2	2	23	10	1
0x0034	...	2	2	2	2		
0x0038	L2: AND R5, R1, R3	2	2	2	2		
0x003C	BEQZ R5, L3	2	2	21	23		
0x0040	L3: ...	2	2	2	2		
0x0050	DADDI R10, R10, #-1	2	2	2	2		
0x0054	BNEZ R10, L0	2	2	2	2		
	...	2	2	2	2		