UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
Engenharia de Computação
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Prof. Sergio Bampi
Alunas: Izadora Berti (275606) e Letícia dos Santos (275604)

APRESENTAÇÃO E ESPECIFICAÇÃO DO IP CORE

openMSP430

O openMSP430 é um microcontrolador de 16 bits sintetizável escrito em Verilog compatível com a família de microcontroladores MSP430 da Texas Instruments e que pode ser utilizado tanto em FPGA quanto em ASIC. Possui área pequena e 8k gates. É designado para baixo custo e baixo consumo de energia.

Características do core:

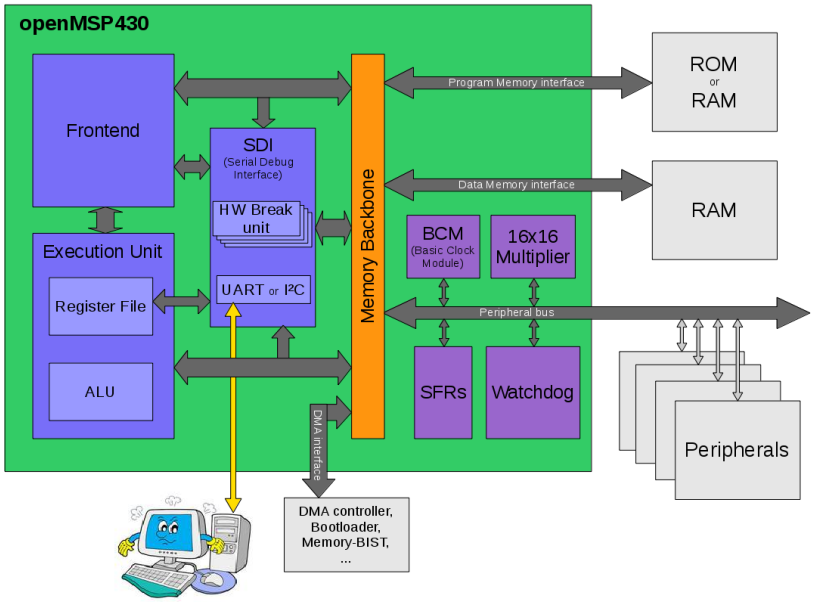
- Suporta todo instruction set.
- Interupções: IRQs (x14, x30 ou x62), NMI (x1).
- Baixo consumo de energia: Low Power Modes (LPMx).
- Suporta memória de instruções e dados separadas com tamanho configurável. Esses blocos NÃO estão contidos no projeto e devem ser adicionados com RAM e/ou ROM.
- Espaço de endereço para periféricos escalável.
- Interface DMA.
- Two-wire Serial Debug Interface (I^2C or UART based) com GDB support (Nexus class 3, w/o trace).
- Compatível com FPGA(opção para single clock domain, sem clock gate). • Compatível com ASIC(opções para full power e clock management support).
- Tamanho pequeno (Xilinx: 1650 LUTs / Altera: 1550 LEs / ASIC: 8k gates).

Periféricos utilizados:

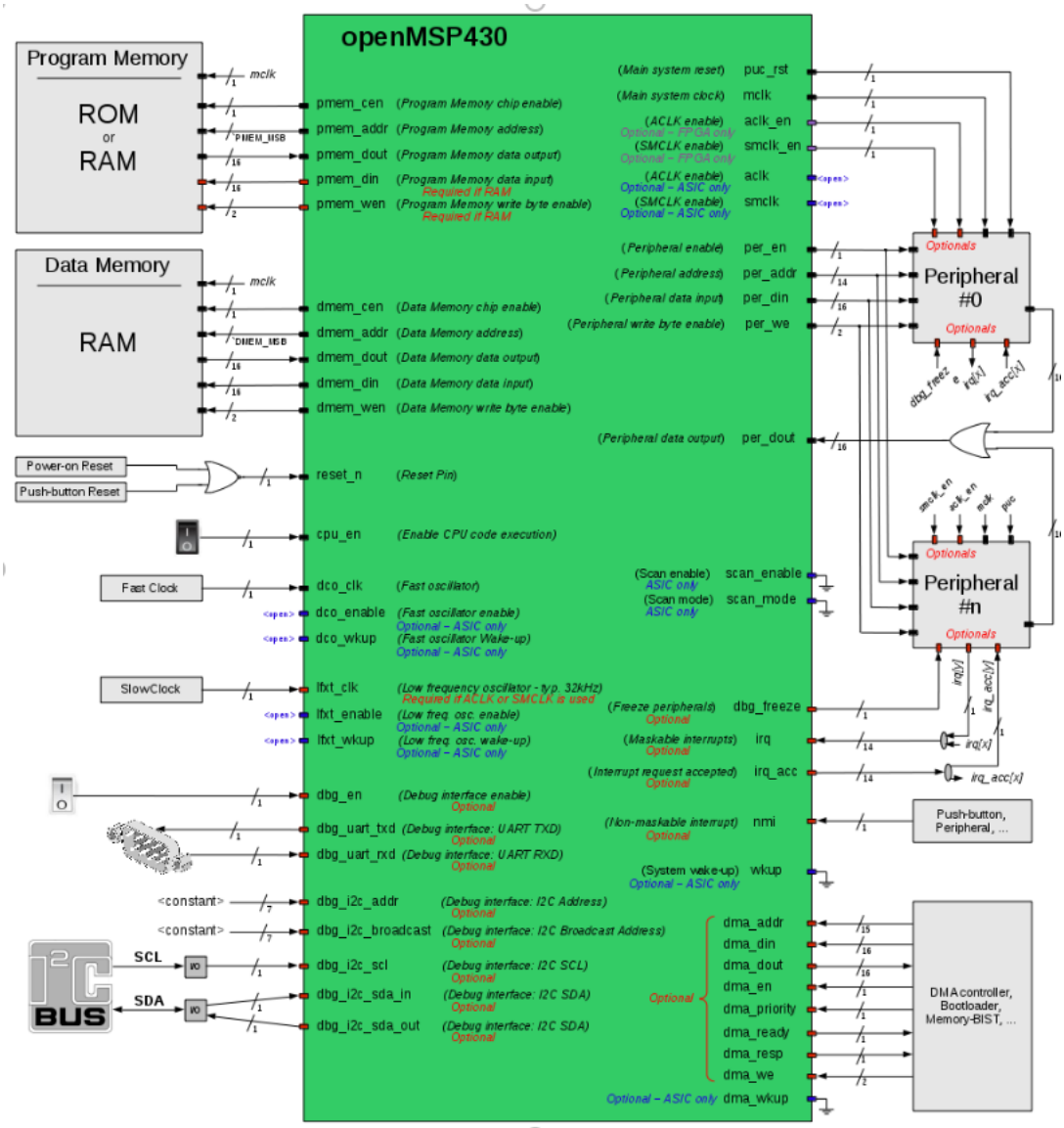
- 16x16 Hardware Multiplier.
- Basic Clock Module.
- Watchdog.
- Timer A (somente FPGA).
- GPIOs (somente FPGA).
- Templates para periféricos de 8 e 16 bits.
- Graphic Controller (openGFX430).

Limitações: não podem ser executadas instruções que estão na memória de dados.

Estrutura



Module



Descrição dos pinos:
The full pinout of the core is summarized in the following table.

Port Name	Direction	Width	Clock Domain	Description
Clocks				
cpu_en	Input	1	or mclk[4]	Enable CPU code execution (asynchronous and non-glitchy). Set to 1 if unused.
dco_clk	Input	1	-	Fast oscillator (fast clock)
lfxt_clk	Input	1	-	Low frequency oscillator (typ. 32kHz) Set to 0 if unused.
mclk	Output	1	-	Main system clock
aclk_en	Output	1	mclk	FPGA ONLY: ACLK enable
smclk_en	Output	1	mclk	FPGA ONLY: SMCLK enable
dco_enable	Output	1	dco_clk	ASIC ONLY: Fast oscillator enable
dco_wkup	Output	1		ASIC ONLY: Fast oscillator wakeup (asynchronous)
lfxt_enable	Output	1	lfxt_clk	ASIC ONLY: Low frequency oscillator enable
lfxt_wkup	Output	1		ASIC ONLY: Low frequency oscillator wakeup (asynchronous)
aclk	Output	1	-	ASIC ONLY: ACLK
smclk	Output	1	-	ASIC ONLY: SMCLK
wkup	Input	1		ASIC ONLY: System Wake-up (asynchronous and non-glitchy) Set to 0 if unused.
Resets				
puc_rst	Output	1	mclk	Main system reset
reset_n	Input	1		Reset Pin (active low, asynchronous and non-glitchy)
Program Memory interface				
pmem_addr	Output	`PMEM_AWIDTH[1]	mclk	Program Memory address
pmem_cen	Output	1	mclk	Program Memory chip enable (low active)
pmem_din	Output	16	mclk	Program Memory data input (optional [2])

pmem_dout	Input	16	mclk	Program Memory data output
pmem_wen	Output	2	mclk	Program Memory write byte enable (low active) (optional [2])
Data Memory interface				
dmem_addr	Output	`DMEM_AWIDTH[1]	mclk	Data Memory address
dmem_cen	Output	1	mclk	Data Memory chip enable (low active)
dmem_din	Output	16	mclk	Data Memory data input
dmem_dout	Input	16	mclk	Data Memory data output
dmem_wen	Output	2	mclk	Data Memory write byte enable (low active)
External Peripherals interface				
per_addr	Output	14	mclk	Peripheral address
per_din	Output	16	mclk	Peripheral data input
per_dout	Input	16	mclk	Peripheral data output
per_en	Output	1	mclk	Peripheral enable (high active)
per_we	Output	2	mclk	Peripheral write byte enable (high active)
Direct Memory Access interface				
dma_addr	Input	15	mclk	Direct Memory Access address
dma_din	Input	16	mclk	Direct Memory Access data input
dma_dout	Output	16	mclk	Direct Memory Access data output
dma_en	Input	1	mclk	Direct Memory Access enable (high active)
dma_priority	Input	1	mclk	Direct Memory Access priority (0:low / 1:high)
dma_ready	Output	1	mclk	Direct Memory Access is complete
dma_resp	Output	1	mclk	Direct Memory Access response (0:Okay / 1:Error)
dma_we	Input	2	mclk	Direct Memory Access write byte enable (high active)
dma_wkup	Input	1		ASIC ONLY: DMA Wake-up (asynchronous and non-glitchy)
Interrupts				
irq	Input	`IRQ_NR-2[1]	mclk	Maskable interrupts (one-hot signal)
nmi	Input	1	or mclk[4]	Non-maskable interrupt (asynchronous)

irq_acc	Output	`IRQ_NR-2[1]	mclk	Interrupt request accepted (one-hot signal)
Serial Debug interface				
dbg_en	Input	1	or mclk[4]	Debug interface enable (asynchronous) [3]
dbg_freeze	Output	1	mclk	Freeze peripherals
dbg_uart_txd	Output	1	mclk	Debug interface: UART TXD
dbg_uart_rxd	Input	1		Debug interface: UART RXD (asynchronous)
dbg_i2c_addr	Input	1	mclk	Debug interface: I2C Address
dbg_i2c_broadcast	Input	1	mclk	Debug interface: I2C Broadcast Address (for multicore only)
dbg_i2c_scl	Input	1		Debug interface: I2C SCL
dbg_i2c_sda_in	Input	1		Debug interface: I2C SDA input
dbg_i2c_sda_out	Output	1	mclk	Debug interface: I2C SDA output
Scan				
scan_enable	Input	1	dco_clk	ASIC ONLY: Scan enable (active during scan shifting)
scan_mode	Input	1		ASIC ONLY: Scan mode

1: This parameter is declared in the "openMSP430_defines.v" file and defines the RAM/ROM size or the number of interrupts vectors (16, 32 or 64).
2: These two optional ports can be connected whenever the program memory is a RAM. This will allow the user to load a program through the serial debug interface and to use software breakpoints.
3: When disabled, the debug interface is hold into reset (and clock gated in ASIC mode). As a consequence, the ***dbg_en*** port can be used to reset the debug interface without disrupting the CPU execution.
4: Clock domain is selectable through configuration in the "openMSP430_defines.v" file (see Advanced System Configuration).

Testbenches
• Testbench top level module: tb_openMSP430.v
• Testbench instruction decoder and ASCII chain generator for easy debugging: msp_debug.v

Obs: e tem as versões desses testbenches para xilinx_diligent_s3board, altera_de1_board e actel_m1a3pl_dev_kit

Benchmark que será utilizado e resultados anteriores que estão na documentação

2.9.1 Dhrystone (DMIPS/MHz)
Dhrystone is known for being susceptible to compiler optimizations, among other issues However, as it is still quite a popular metric,
some results are provided here (ranging from 0.30 to 0.45
DMIPS/MHz depending on the compiler version and options).

Dhrystone flavor	Compiler options / Compiler version	-Os	-O2	-O3
Dhrystone v2.1 (common version)	mspgcc v4.4.5	0.30	0.32	0.33
	mspgcc v4.6.3	0.37	0.39	0.40
Dhrystone v2.1 (MCU adapted)	mspgcc v4.4.5	0.30	0.30	0.31
	mspgcc v4.6.3	0.37	0.44	0.45

Como já estudados a teoria de processadores em várias outras cadeiras, achamos que sintetizar um processador em circuitos integrados pode nos ajudar a compreender melhor o funcionamento no mundo real e aproximar-nos ao que a indústria produz atualmente. Esse projeto foi escolhido porque, dentre os processadores, está muito bem documentado, é certificado pela Open Cores e possui muitas estrelas. Esperamos que a documentação nos ajude a resolver problemas futuramente.

Fontes: https://opencores.org/projects/openmsp430

Graphic Controller: https://opencores.org/projects/opengfx430