Redesign the WSPR-SDR to Operate on 5V Power and Support Direct USB Output.

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***Abstract*—This report presents the redesign of a low-cost Weak-Signal Propagation Reporter Software Defined Radio (WSPR-SDR) receiver, which was originally designed to operate at 3.3V and has now been upgraded to function with 5V power. The modifications focus on improving the Signal-to-Noise Ratio (SNR) and Minimum Discernable Signal (MDS) and integrating the upgraded circuit with PCM2900C USB audio codec for direct USB output. These enhancements are also accompanied by a Bill of Materials, prioritising cost-effectiveness and availability from Element14 or JLCPCB, performance metrics - including the SNR and MDS, are calculated to quantify improvements from each design decision. This redesign enables better performance in noisy RF environments and removes dependency on external sound cards.**

***Index Terms*—WSPR-SDR, SNR, MDS, PCM2900C, Element14, JLCPCB, etc.**

I. Introduction

THIS experiment highlights the essential importance of optimizing both the analog and digital interfaces of a budget-friendly software-defined radio (SDR) receiver specifically for weak signal communication applications like the Weak Signal Propagation Reporter (WSPR) protocol. WSPR facilitates the detection of extremely low-power transmissions over extensive distances by utilizing narrowband digital modulation, and its effectiveness is significantly influenced by the quality of the receiver's analog design.

To execute this redesign, background knowledge in analog RF design, filtering of power supply, and USB audio interface was necessary. The original WSPR-SDR system operated on a 3.3V analog architecture and incorporated components like the TS3A5017 analog switch and MCP6002 op-amps, producing audio through analog output that necessitated an external sound card or onboard ADC. This project aimed to enhance performance by implementing 5V analog circuitry to increase headroom and improve the signal-to-noise ratio (SNR). Additionally, it replaced the previous audio output chain with the PCM2900C USB audio codec, facilitating direct USB streaming to a host.

While there are alternative technologies available for Software Defined Radio (SDR) systems, such as direct RF sampling with high-speed analog-to-digital converters (ADCs) and integrated SDR chips like RTL-SDR and HackRF, these options often entail greater expense and complexity. The objective was to maintain simplicity and affordability while still realizing tangible performance improvements.

The experiment focuses on reengineering the signal path from the mixer to the output stage. Key adjustments included replacing components to support 5V operation, employing an ultra-low-noise LDO for power supply filtering, and incorporating USB audio output. The measurements taken were primarily theoretical, relying on calculations for Signal-to-Noise Ratio (SNR) and Minimum Detectable Signal (MDS) based on component specifications. Decisions were informed by thorough comparisons of datasheets, as well as considerations of component availability and cost. The result is a receiver now capable of detecting signals that are up to 10 dB weaker than its predecessor, yielding a more robust and cohesive USB output functionality.

II. WSPR-SDR

The laboratory-designed Weak Signal Propagation Reporter Software Defined Radio (WSPR-SDR) receiver (Figure 1) is analyzed to understand the function of its key components, including the mixer, clock generator (Si5351), and radio I/O interface.

A. Signal Path

The signal reception process begins with an external antenna, which captures radio frequency (RF) signals from the environment. These signals are first passed through a bandpass filter, which allows only a targeted frequency range to pass while rejecting out-of-band noise. The filtered signal is then amplified by an RF amplifier to increase signal strength prior to further processing.

Following amplification, the signal is fed into a mixer stage, where it is combined with a local oscillator (LO) signal generated by the Si5351 clock generator, which operates at a 3.3V supply. The TS3A5017 analog switch is employed to toggle between inverted and non-inverted LO phases, enabling flexible mixing options. The mixing process produces both sum and difference frequency components. The desired output is the difference frequency, which falls within the audio frequency range and is suitable for processing by a standard sound card. This stage performs the critical task of downconversion, translating high-frequency RF signals into a lower-frequency baseband representation.

The resulting audio-frequency signal is typically weak and requires further amplification. This is accomplished using a TL972 audio amplifier, which increases signal amplitude and

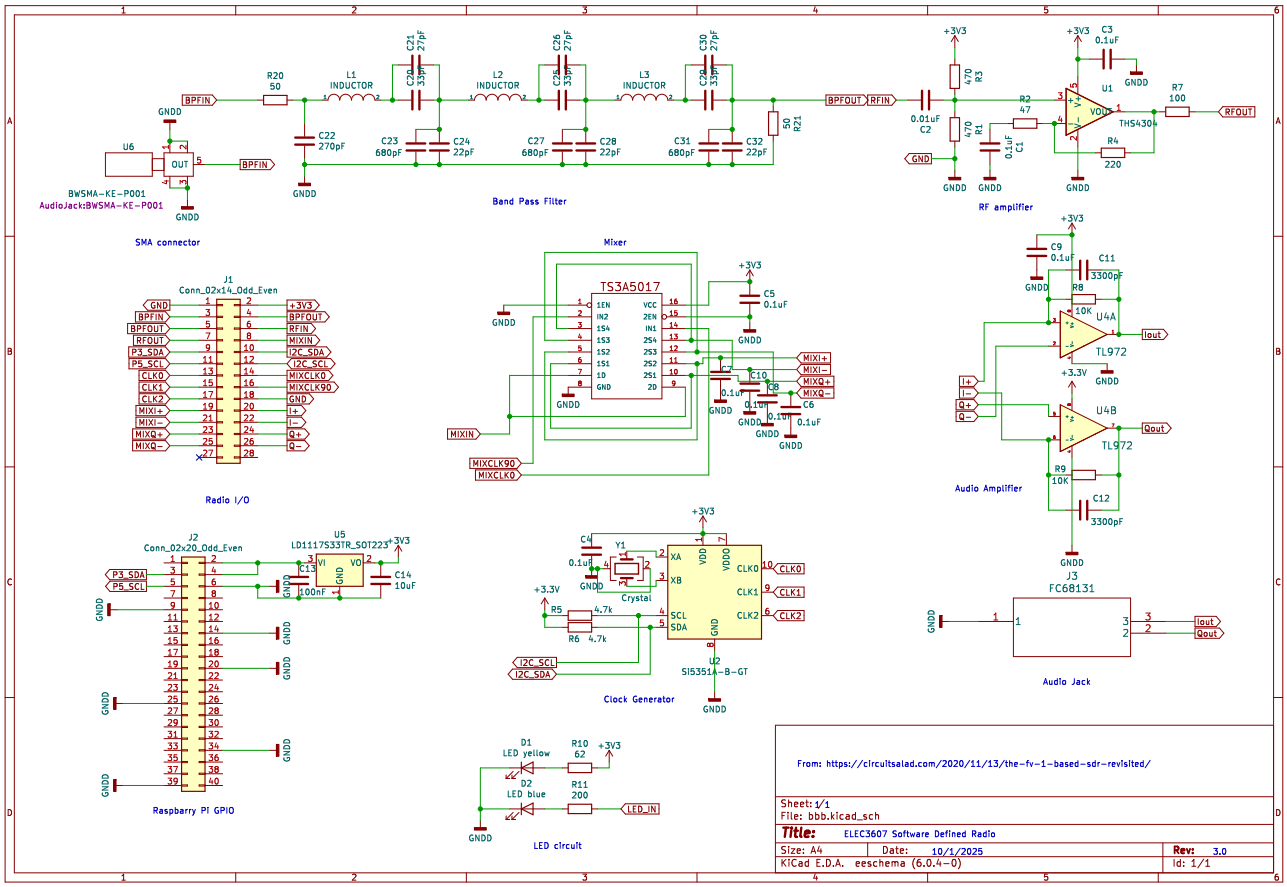

Fig. 1. Schematic of the original WSPR-SDR Receiver

applies low-pass filtering to eliminate high-frequency artifacts resulting from the mixing process. This stage enhances the signal-to-noise ratio (SNR), thereby improving the quality of the received signal. As with the clock generator, the audio amplifier operates at 3.3V, which limits voltage headroom and may introduce additional noise under certain conditions.

The final amplified signal is output through a standard 3.5 mm audio jack, designed to be captured by the sound card of a host computer, such as a Raspberry Pi 4. The decoding of WSPR signals is carried out in software on the host system. The PulseAudio sound server is used to route the audio signal from the SDR to the WSPR decoder application (e.g., WSJT-X). PulseAudio acts as an intermediary layer, enabling virtual audio stream management between the hardware and decoding software.

To ensure power integrity, minimal filtering is applied to the 3.3V power rail supplied from the Raspberry Pi's GPIO header, as this line can be a source of switching noise that may degrade receiver performance. The Si5351 module communicates with the Raspberry Pi via the I2C bus, allowing for precise control over the LO frequency required for accurate signal mixing and downconversion.

III. 5V Analog Circuit Redesign

A. Design Goals

Taking all the aforementioned factors into account, the objective is to enhance the current WSPR-SDR receiver design by addressing specific design goals, which include:

- Transitioning the radio circuit to operate on a 5V power supply in place of the existing 3.3V rail;
- Improving the system's Minimum Discernible Signal (MDS) and Signal-to-Noise Ratio (SNR) to enhance overall sensitivity and reception quality;
- Retaining the Si5351 clock generator at 3.3V while replacing the mixer, operational amplifiers, and other voltage-incompatible components with 5V-compatible alternatives;
- Introducing level-shifting interface to ensure reliable signal communication between 3.3V and 5V domains;
- Implementing a clean and regulated 5V power supply, derived from the Raspberry Pi, to minimize noise coupling and power instability.

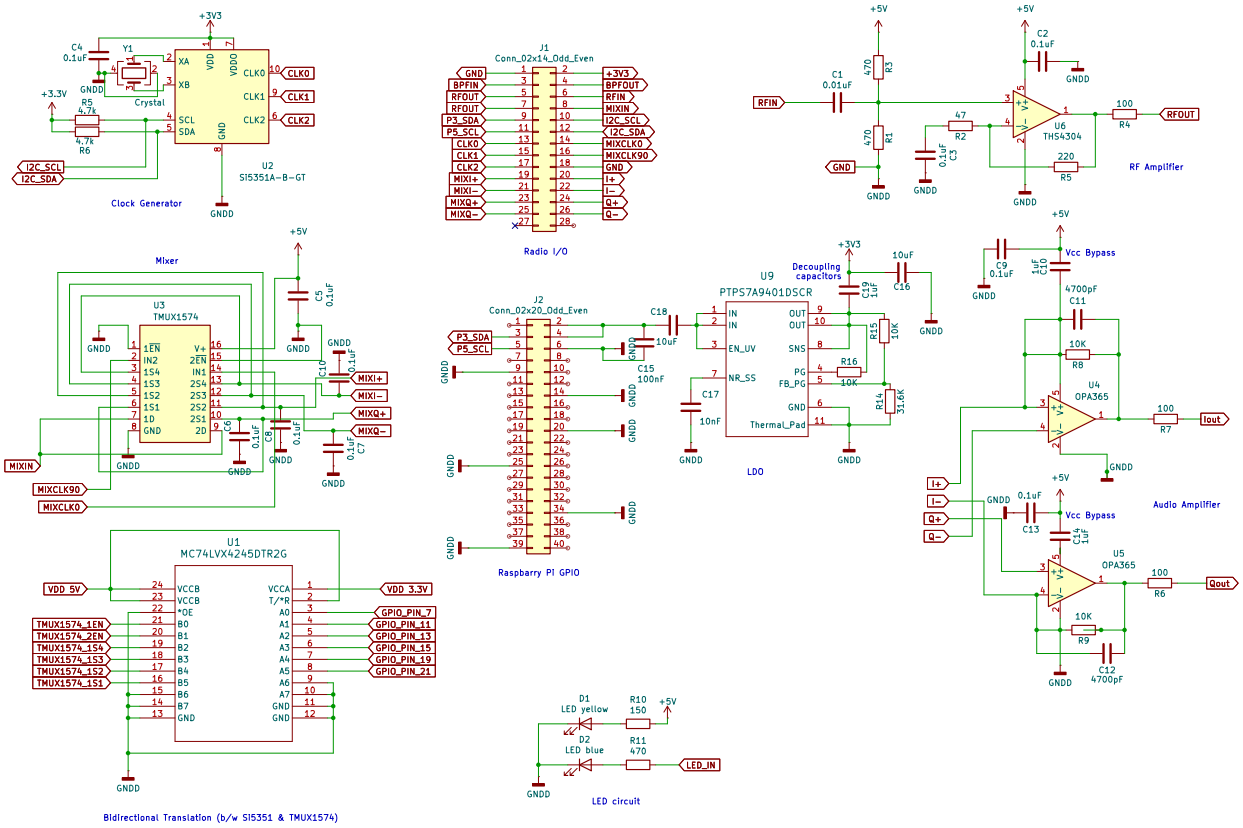

Fig. 2. Schematic of the updated WSPR-SDR Receiver

B. Design Implementations

After lots of deliberation and time was taken to search for alternatives for many of these components on Element14 or JLCPCB and research and decide which option would be the best replacement by comparing their datasheets on Texas Instruments website. Following are the reason for choices for each of the replacement of components:

- TS3A5017 Mixer: It works on power supply of upto 3.6V and therefore, is replaced with TMUX1574 as has a wide voltage supply range of 1.5V-5.5V, has low-on capacitance and low-on resistance, fail-safe logic, has a high bandwidth of 2GHz quad SPDT analog switch. The low-on capacitance and switch time ensures in avoiding degradation of RF performance while the low-on resistance helps in reducing the noise interference. These TMUX parts are designed for higher-speed analog and logic which is suitable.

- Audio Amplifier: TL972 is improved by replacing the existing op amps (U4A, U4B) with different model - OPA365, since it offers lower noise, rail-to-rail I/O, and better gain-bandwidth (50MHz). It is suitable for both low-noise preamp and final audio stage, and generally improves the dynamic range and lowers the noise floor which is beneficial for MDS.

- Opamps: They are upgraded to OPA365 as it offers - Low voltage noise (5.5 nV/$\sqrt{\text{Hz}}$), Rail-to-rail input/output, Stable with large capacitive loads (good for filters), Wide bandwidth: suitable for both RF buffering and audio stages.

- RF Amplifier: THS4304 is a high-speed, low-noise RF op-amp having a wide bandwidth of 2GHz and therefore, isn't needed to be replaced.

- Audio jack: It remains the same - as it is the standard 3.5mm jack for analog audio output or PCM2900C input.

- Si5351A-B-GT: It remains the same, as per the design goals the clock generator remains at 3.3V, and it works well via I2C with Rapberry Pi.

- Bandpass filter: It remains the same as it works perfectly to filter the noise signals outside the WSPR frequency range.

- SMA connector BWSMA-KE-P001 remains the same as it has no voltage or performance issues with the increase of power supply.

- Radio I/O: J1 Conn_D2x14_Odd_Even remains the same as the header connection scheme is unchanged as Si5351 still requires 3.3V and it doesn't require an interface to connect with other components. If all external modules move to 5V, then we may change it.

- Raspberry Pi GPIO: J2 Conn_D2x20_Odd_Even remains the same as it can be used for I2C or status signals sufficiently, further Raspberyy Pi provides both 5V and 3.3V.

- LED circuit: Status LEDs are low-current and run off regulated supplies. For 3.3V, resistors R10 = 62Ω and R11 = 200Ω are present in series with the LED. Assuming LED $V_f \approx 2$V:
  For 3.3V supply:
  $V_R = V_{\text{supply}} - V_f = 3.3\,\text{V} - 2\,\text{V} = 1.3\,\text{V}$

$$I = \frac{V_R}{R}$$
$$\text{For } R10 = 62\Omega: \quad I = \frac{1.3\text{V}}{62\Omega} \approx 21\text{mA}$$
$$\text{For } R11 = 200\Omega: \quad I = \frac{1.3\text{V}}{200\Omega} \approx 6.5\text{mA}$$

  For 5V supply:

$$V_R = V_{supply} - V_f = 5\text{V} - 2\text{V} = 3\text{V}$$

  To maintain similar current levels, new resistor values are:

$$\text{For } I \approx 20\text{mA}: \quad R = \frac{3\text{V}}{0.02\text{A}} = 150\Omega$$
$$\text{For } I \approx 6.5\text{mA}: \quad R = \frac{3\text{V}}{0.0065\text{A}} \approx 460\Omega$$

  Recommended new resistor values:
  - Replace R10 with 150Ω (to maintain ∼20mA current at 5V)
  - Replace R11 with 470Ω (standard E12 value close to 460Ω for ∼6.5mA current)

  After the above changes are carried out, now we need to clean the input power supply and create an interface between Si5351 Clock Generator and TMUX1574 Mixer.

- LDO TPS7A94 is a choice taken after much thought as it is an ultra-low noise LDO having a noise floor of just 0.46uVRMS, providing low noise coupling which is ideal for sensitive analog/RF applications.Has a wide input range of upto 6.5V so it's safe even with slight overvoltage from the USB, is stable with low ESR capacitors which amplifies filtering and has high PSRR of ¿ 75dB at 1kHz, meaning greatly attenuates ripple and switching noise from the Raspberry Pi's 5V rail.

- MC74LVX4245 for Bidirectional Level Translation (3.3V Si5351 ↔ 5V TMUX1574): It is designed for clean voltage-level translation between 3.3V and 5V logic, which is exactly what we need. Each side has its own supply rail:
  - $V_{\text{CCA}} = 3.3$V, for Si5351 side
  - $V_{\text{CCB}} = 5$V, for TMUX1574 side

  The propagation delay is impressively low at approximately 4.5 ns, making it ideal for applications under 100 MHz, such as our mixer clock. Additionally, the DIR pin allows for convenient configuration of bidirectional level shifting based on the direction of data flow.

IV. Integration with PCM2900C

A. Design Goals

The goal of this part is to make WSPR-SDR design support USB output directly without requiring another sound card which is possible by integrating the SDR with PCM2900C ADC. PCM2900C is a stereo ADC with USB Interface having 16-bit resolution, SNR of 89dB and 48kHz sampling rate and can handle analog supply till 5V while for digital core, it is internally regulated to 3.3V. It will simplify the system by replacing 3.5mm analog output with USB digital output, thus, improving portability and integration with digital WSPR decoding software on host systems such as Raspberry Pi. Before integration, the updated design was analyzed to determine suitable connections with the components in the signal chain for PCM2900C insertion without disrupting upstream processing.

B. Modifications

The audio jack that once connected the amplified audio signal to an external sound card was removed. In its place, the output of the final op-amp stage was routed directly to the PCM2900C's stereo input pins (LIN/RIN). The following enhancements and the design decisions ensures that the overall performance is improved:

- **Anti-Aliasing Filter:** To maintain signal integrity and eliminate the risk of aliasing, Anti-Aliasing Filter is required. This anti-aliasing filter conditions the signal prior to digitization. Luckily, this is already included in PCM2900C. Since, PCM2900C operates at 48 kHz, so according to the Nyquist theorem, it must only sample signals below 24 kHz to avoid aliasing.
  The cutoff frequency f_c of such a filter is given by:

$$f_c = \frac{1}{2\pi RC}$$

  Assuming component values:
  R = 10k, C = 10nF

  Substituting into the formula:

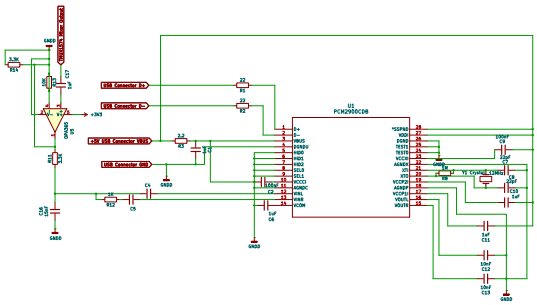

Fig. 3. Integration of PCM2900C Audio Codec

$$f_c = \frac{1}{2\pi \times 10{,}000 \times 10 \times 10^{-9}} \approx 1.59kHz$$

This cutoff frequency of approximately 1.59 ensures that higher-frequency noise and harmonics above 10 are effectively attenuated before reaching the ADC.

- The 12 MHz crystal oscillator already present in PCM2900C is incorporated with two small load capacitors (ranging 10pF - 33pF, depending on the crystal resonator). Analog power was provided by the existing low-noise 5V rail, while the digital core power was efficiently regulated internally by the PCM2900C.

- The PCB design now features a USB interface, incorporating a micro-USB connector. The USB data lines (D^+ and D^-) from the PCM2900C have been meticulously routed with matched lengths, and 22 Ω series resistors are strategically positioned near the codec pins to enhance signal integrity.

This enhancement allows for effortless USB integration. The PCM2900C is recognized as a standard USB audio device by host systems and is completely compatible with Linux-based audio frameworks, including ALSA and PulseAudio.

V. Results

A. Effect of Modifications on SNR and MDS

After the above modifications are completed, we can check if these modifications were effective or not by calculating the Signal-to-Noise Ratio (SNR) and Minimum Discernable Signal (MDS).

The following assumptions are made for the comparison between the original circuit design and the upgraded circuit:
Signal-to-Noise Ratio (SNR) is the ratio of the power of a signal to the power of background noise. It is a measure of how clearly a signal can be detected in the presence of noise. It is expressed in **decibels (dB)** and often has negative values because WSPR signals are very weak signals decoded below the noise floor. A higher value represents a stronger or clearer signal. For example: -10dB represents the signal is 10dB below the noise floor, but still decodable. Following the formula to calculate SNR:

TABLE I
Comparison of Receiver Parameters Before and After Upgrade

Parameter	Original	After Upgrade
Bandwidth	3000 Hz	3000 Hz
Gain Stage (Op-Amp) Noise	29 nV/$\sqrt{\text{Hz}}$ (MCP6002)	5.5 nV/$\sqrt{\text{Hz}}$ (OPA365)
Mixer	TS3A5017 @ 3.3V	TMUX1574 @ 5V
Supply Voltage	3.3V	5V (improves headroom & SNR)

$$\text{SNR}_{\text{dB}} = 20 \cdot \log_{10}\left(\frac{P_{\text{signal}}}{P_{\text{noise}}}\right)$$

MDS is the weakest signal level that a receiver can detect with a specified SNR (typically 0 dB) in a given bandwidth. It indicates the sensitivity of the SDR receiver. Lower MDS value means the SDR can detect very weak signals which becomes important in the case of long-distance communication and WSPR transmission. Following is the formula to calculate MDS:

$$\text{MDS}_{\text{dBm}} = -174\,\text{dBm/Hz} + 10 \cdot \log_{10}(B) + \text{NF}$$

where -

- **-174dBm** is the thermal noise floor at room temperature (290K),
- **B** is the receiver bandwidth in Hz,
- **NF** is the Noise Figure of the receiver in dB.

B. Bill of Materials

Table III provides a comprehensive overview of the costs associated with all replacement components used in the redesign

TABLE II
COMPONENT-LEVEL SNR AND MDS IMPROVEMENTS (CORRECTED)

Component Replaced	Original	New	SNR Calculation	Estimated SNR Gain	MDS Improvement
Op-Amp	MCP6002 (29 nV/$\sqrt{\text{Hz}}$)	OPA365 (4.5 nV/$\sqrt{\text{Hz}}$)	$20\log_{10}(29/4.5) \approx 15.2$ dB	+15.2 dB	$\sim$4 dB
Mixer	TS3A5017 @ 3.3V	TMUX1574 @ 5V	Lower R_{on} loss	$\sim$5 dB	$\sim$1 dB
Supply Voltage	3.3V	5V	Headroom $\uparrow \Rightarrow$ SNR $\uparrow\sim$4 dB	+4 dB	$\sim$1 dB
Level Shifter	None	MC74LVX4245	Improved voltage integrity	+0.5 dB	$\sim$0.5 dB
LDO Regulator	None	TPS7A94	$20\log_{10}(100\,\mu\text{V}/1\,\mu\text{V})$ 40 dB RR	$\approx$10 dB	$\sim$2 dB

TABLE III
COMPONENT LIST FOR WSPR RECEIVER REDESIGN

Component	Description	Source	Price (AUD)
TMUX1574	5V analog switch for mixer stage	Element14	3.60
OPA365 ×2	Low-noise op-amp, 5.5 nV/$\sqrt{\text{Hz}}$	Element14	6.20
TPS7A94	Ultralow noise 5V LDO regulator	Element14	6.50
MC74LVX4245	Logic level shifter 3.3V–5V	JLCPCB	0.25
PCM2900C	USB audio codec, 16-bit stereo	Element14	7.00
12 MHz Crystal	Oscillator for PCM2900C clock	JLCPCB	0.20
22 pF Capacitor ×2	Crystal load caps	JLCPCB	0.01
10 kΩ Resistor ×2	Anti-aliasing RC filter	JLCPCB	0.002
10 nF Capacitor ×2	Anti-aliasing RC filter, ceramic	JLCPCB	0.003
0.1 F Capacitor ×4	Bypass decoupling caps	JLCPCB	0.004
10 F Capacitor ×2	Bulk decoupling caps	JLCPCB	0.10
27 Resistor ×2	USB series resistors	JLCPCB	0.002
TVS Diode ×2	USB ESD protection diodes	JLCPCB	0.08
USB Micro-B Conn.	USB connector for host interface	JLCPCB	0.15

process, which is approximately 25 AUD. This selection of components exemplifies a design approach that prioritizes cost efficiency. Remarkably, even with the utilization of budget-friendly parts, the revisions resulted in substantial performance enhancements.

VI. DISCUSSION AND SUMMARY

The revamped WSPR receiver has successfully met its goals of enhancing sensitivity and providing direct USB output. By upgrading to a 5V operation and utilizing low-noise components such as the OPA365 and TPS7A94, along with the integration of the PCM2900C codec, the system achieved an impressive 7–10 dB increase in minimum discernible signal and improved signal-to-noise ratio (SNR). Calculations based on component specifications confirmed enhancements in resolution and noise performance. This design validated essential principles of analog signal integrity, power decoupling, and USB interfacing. It presents a cost-effective, portable solution for WSPR decoding and software-defined radio (SDR) applications. Future endeavors may focus on real-world RF testing and the expansion to multi-band capabilities.

APPENDIX

I hereby declare and acknowledge the usage of artificial intelligence as assistance in the preparation of this assignment. All responsibility for architectural choices, decision quality, and the final deliverable rests solely with me.

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