Design and Analysis of a Low Dropout Voltage Regulator Using 28nm CMOS Technology

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Abstract

The paper constitutes the design and analysis of a Low Dropout Voltage Regulator. A low-dropout (LDO) transformer is the main component utilized in the bulk of portable electronic applications since it's used as a power management unit in those applications. In this paper, an LDO regulator for the power management microcircuit in 28m CMOS technology using Synopsys Custom Design Platform is presented. The error amplifier of the proposed LDO employed seven transistors for the current mirror. Meanwhile, the PMOS transistor is employed as a pass element transistor to control the voltage variation. The resistors are used as a feedback network circuit while the capacitor is employed to minimise the variation of output voltage.

1 Reference Circuit Details

The proposed LDO regulator circuit was constructed in Synopsys Custom Design Platform. Figure 1 shows the schematic of the proposed LDO regulator. In the schematic diagram, the error amplifier is constructed by three PMOS transistors and five NMOS transistors. The transistors M0 to M7 are used to form the current mirror circuit. The function of the current mirror structure will ensure each line of wire able to get the same current level in this design. All the transistors are using 28nm technology size. Based on the proposed design, a PMOS transistor M8 is used as a pass element transistor to control the voltage from the input to the output differential voltage. The main reason is the PMOS transistor is voltage-driven and does not require much current, thus greatly reducing the current consumed by the device itself. In addition, the voltage drop across the PMOS transistor is similar to the product of the output current and the on-resistance. The resistors R1 and R2 are used as a voltage divider network or feedback circuit. The feedback circuit structure can generate a feedback voltage into an error amplifier. The capacitor (Cload) is used as a stabilizer to stabilize the output voltage and the load resistor (Rload) is

10 kΩ.

$$PSRR = 20\ log \frac{\Delta V_{out}}{\Delta V_{in}}$$

2 Circuit Design

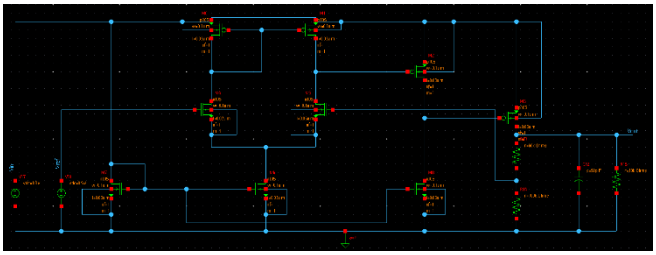
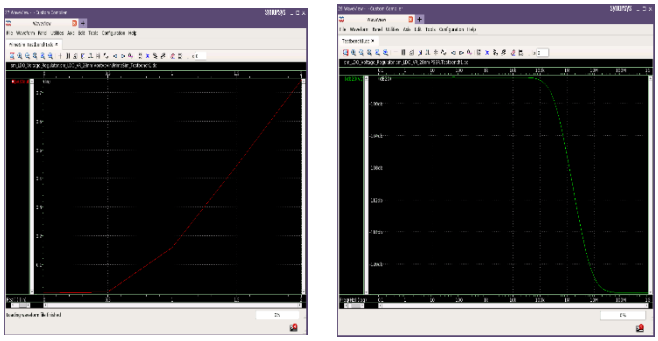


Figure 1: Circuit diagram.

3 Circuit Waveforms



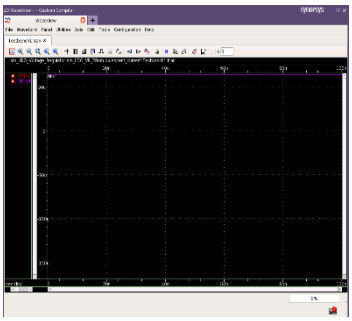


Figure 2: waveforms

Reference Paper/Journals

[1] S.A.Z Murad. Design of CMOS Low-Dropout Voltage Regulator for Power Management Integrated Circuit in 0.18-µm Technology. https://cutt.ly/oPmF0f0

[2] N. H. E. Weste. Cmos vlsi design : A circuits and systems perspective. https://cutt.ly/InNnZPb.