PERFORMANCE ANALYSIS OF FULL ADDER BASED ON DOMINO LOGIC TECHNIQUE

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ABSTRACT

In modern VLSI area efficient devices are most used because most of the devices are becoming portable. The Domino logic technique is often employed in designing the area efficient and high-speed devices. In this research paper. one- bit full adder circuit using CMO S based logic and domino- based logic on Cadence Virtuoso has been designed based on 90nm technology having the supply voltage of 1.8V. This research paper is mainly centralized on the design of area efficient and fast speed devices. This work evaluates the performance CMO S and Domino logic based on full adder circuit in terms of delay and power consumption. It was found that Domino logic based one - bit full adder circuit occupied lesser area and introduces less delay as comparison to one -bit full adder circuit. based on CMO S logic.

Keywords— CMOS, Domino, Full adder, Performance Parameters.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

In the fast-growing VLSI industry, transistor density is increasing with rapid rate day-by-day. According to Moore's law transistor density will get doubled itself after every eighteen months. As the number of transistors will increase, correspondingly area, delay and power consumption of the device will also increase. So, a technology is required by which the area can be reduced and increase the performance of the device. From the past few decades CMOS technology is being used for designing the chips in semiconductor industry, but as the number of transistors are increasing, area of the device and delay both are increasing. So, it requires to switch to a technology, which uses lesser area and smaller delay. Hence, the Domino logic is used for designing the one-bit full adder and compared the various performance parameter like area, delay, and power consumption in both technologies.

1.2 Objective

CMOS Logic- CMOS is abbreviation of "Complement Metal Oxide Semiconductor". CMOS logic uses the p-MOS and n-MOS transistors as shown in Fig.1.1, and they work as a pull up and a pull-down transistor respectively. When input will be low then p-MOS will be on and it will charge the output node to Vdd, and when input will be high n-MOS will turn on and charge stored at the output node get a conducting path between output node and ground. CMOS logic design has various numbers of advantages as compared to the other logics which were used before. In this both the transistors are connected in complementary form i.e., if one transistor will be on, other will be off and vice versa. The main advantages of the CMOS logic are that high noise margin, low power dissipation and the output are pretty much rail-to-rail. There are also some disadvantages in CMOS logic like, it required large area and speed of operation is slow. So, for the circuit which uses large number of transistors it requires very large area and speed of operation becomes slow. That's why there is a need to move on to another technology which require a smaller number of transistors and provide high speed of operation.

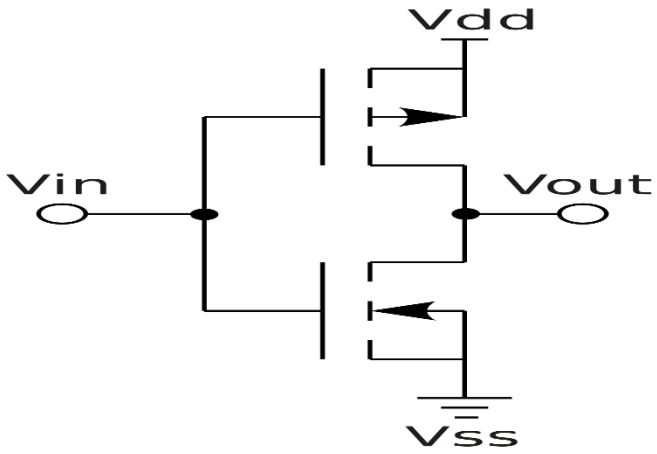

Fig. 1.2.1. CMOS inverter

Domino logic- Domino logic family find a wide variety of application, where less transistor count and high speed of operation such as microprocessor, dynamic memory, digital signal processors etc. are required. Domino logic is an evolution in CMOS based dynamic logic techniques which use either p-MOS or n-MOS for the pull down or pull up network. The methodology of designing full adder by using Domino logic employs lesser no. of transistors as if compared to conventional CMOS logic and provides high performance device.

The Domino logic is an improvement in dynamic logic which has a drawback when one gate is cascaded too next. In domino logic. A static inverter is used between the two stages for removing the drawback of dynamic logic. There are various advantages of Domino logic like they have a smaller area unlike conventional CMOS logic, parasitic capacitance is smaller in domino logic, so it provides high speed of operation and result is glitch free because each gate makes only one transition.

Domino logic consists of two- stages of operation in which first stage is pre-charging, and another stage is evaluation. When clock ‘clk’ is equal to zero or low p-MOS will be on, and it pre-charged the output node to Vdd. When the clk goes to high, p-MOS will be off, and the evaluation phase will start. In this phase output will depend on the input’s configuration. Output node may discharge if inputs have a direct conducting path to ground otherwise it will remain high. So, the output of circuit is obtained by which it has been intended to design in evaluation

phase only. In pre-charge phase, it will provide low output because we used an inverter in this logic style for cascading the next stage.

Adders

As the name suggests, Adder is used to add binary numbers. Adder circuit is basically a combinational logic circuit. It is a memory less circuit and performs an operation assigned to it logically by a Boolean expression. The output depends upon the present input at any given time.

Adder is used in the processor to increment and decrement operator operators, calculate addresses and to perform Arithmetic and logical operation in ALU.

Classification of Adders

Adders are broadly classified into two types. They are:

- Half Adder
- Full Adder
- Multi-bit Adder

Half Adder

Half Adder is a combinational arithmetic circuit that adds two binary numbers and produces sum bit(S) and carry bit(C) as the output. It is used to add 2 single-bit binary numbers.

Full Adder

It is a combinational arithmetic circuit constructed by combining two Half Adder circuits. It is used to add 3 one-bit binary numbers.

Multi-bit Adder

Multi-bit Adders are constructed using Full Adders either serially or in Parallel known as

- Serial Adder
- Parallel Adder

Serial Adder

Serial Adder is constructed using Full Adder. It has three single bit inputs and two single bit outputs. It is a circuit that performs binary addition bit by bit for every clock (CLK) pulse. It is a sequential logic circuit.

Parallel Adder

Several Full-Adders are cascaded to perform binary addition faster. The circuit is used to find the sum of 2 binary numbers greater than one bit in length. It is a combinational logic circuit.

For every clock pulse the bits are added simultaneously. These are different types of Parallel Adders. They are:

- Ripple Carry Adder
- Carry Look Ahead Adder
- Cary Save Adder
- Carry Increment Adder
- Carry Skip Adder
- Carry Select Adder
- Carry Bypass Adder

Applications of Adder

- A Full Adder's circuit can be used as a part of many other larger circuits like Ripple Carry Adder which adds n-bits simultaneously.
- The dedicated multiplication circuits use Full Adder's circuit to perform Carryout Multiplication.
- Full Adders are used in ALU- Arithmetic Logic Unit.
- To generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of Full Adders.
- Full Adders are a part of Graphics Processing Unit for graphics related applications.

Ripple Carry Adder:

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay here. Similarly, the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal.

Carry Look-ahead Adder:

A carry look-ahead adder reduces the propagation delay by introducing more complex hardware. In this design, the ripple carry design is suitably transformed such that the carry logic over fixed groups of bits of the adder is reduced to two-level logic. The carry out bit of the last adder doesn't wait bits of previous adder. Here, all the carry bits of each adder are produced at the same time. Hence, the propagation delay reduces compared to Ripple Carry Adder.

Carry Save Adder:

A carry-save adder is a type of digital adder, used to efficiently compute the sum of three or more binary numbers. It differs from other digital adders in that it outputs two (or more) numbers, and the answer of the original summation can be achieved by adding these outputs together. A carry save adder is typically used in a binary multiplier, since a binary multiplier involves addition of more than two binary numbers after multiplication. A big adder

implemented using this technique will usually be much faster than conventional addition of those numbers.

Carry Save Adder:

A Carry Select adder is also a type of digital adder, used to compare the entire process for carry bits of both 1 and 0. Later the required outputs of sum and carry bits are selected through Mux.

Carry Skip Adder:

A Carry Skip adder comes under the category of digital adders. In this logic AND gate is used for every stage of adder to check whether the carry is present or not. If not, the carry bit is directly fed to the last stage of adder. By this, the carry need not to propagate through all the stages of adders in every sequence of inputs.

1.2 Literature Survey

Gaetano Palumbo, Melita Pennisi, Massimo Alioto, "A simple approach to reduce delay variation in Domino logic Gates", IEEE transaction on Circuits and System, Vol. 59, pp. 10-14, October 2012.

In this paper, a simple approach to reduce delay variations in domino logic gates is proposed. Previous analysis by the same authors showed that delay variations in domino logic are mainly due to the feedback loop implemented by the keeper transistor and the output inverter gate. Accordingly, the proposed strategy aims at reducing the loop gain associated with this feedback loop, and hence its impact on delay variations. In particular, a simple modified keeper is proposed to reduce the loop gain while keeping the same silicon area, noise margin, and nominal performance. The resulting delay variations associated with keeper insertion are shown to be lowered by approximately 50%. The proposed approach is assessed by means of simulations in 65-nm and 90-nm commercial CMOS technologies.

Summary: From the analysis of this paper, we learned that loop of feedback impacts on delay variations.

Thakur, R., Dadoria, A. K., & Gupta, T. K, "Comparative analysis of various Domino logic circuits for better performance", International Conference on Advancesin Electronics, Computers and Communications (ICAECC), pp. 1-6, 2019

In this paper, basically the delay and the noise margin parameter associated in the circuit has been analyzed. The paper gives a better approach for the reduction in delay variation and compares the result with different-different types of domino logic circuits. The other domino logic circuits used to discriminate the result of proposed circuit are footed domino logic circuit, footless domino logic circuit, high speed domino logic circuit and conditional keeper domino logic circuit. The simulation process here has been done in 65nm CMOS technology using Cadence Virtuoso at 270 C operating temperature and 0.8 V supply voltage. In this paper the

parameters like delay, average power, no. of transistors and UNG has been calculated and after simulation it is found that the proposed paper gives better output if it is compared with the other circuits.

F. Frustaci M. Lanuzza P. Zicari S. Perri and P. Corsonello, "Low-power split-path data-driven dynamic logic," IET Circuits Devices Syst., Vol. 3, Iss. 6, pp. 303-312, 2009

Data-pre-charged dynamic logic, also known as data-driven dynamic logic (D3L), is very efficient when low-power constraints are mandatory. Differently from conventional dynamic domino logic, which exploits a clock signal, D3L uses a subset of the input data signals for pre-charging the dynamic node, thus avoiding the clock distribution network. Power consumption is significantly reduced, but the pre-charge propagation path delay affects the speed performances and limits the energy–delay product (EDP) improvements. This study presents a new dynamic logic named split-path D3L (SPD3L) that overcomes the speed limitations of D3L. When applied to a 16 16 bit Booth multiplier realised with STMicroelectronics 65 nm 1V CMOS technology, the proposed technique leads to an EDP 25 and 30% lower than standard dynamic domino logic and conventional D3L counterparts, respectively.

Zhiyu Liu, Volkan Kursun, "PMOS-Only Sleep Switch Dual-Threshold Voltage Domino Logic in Sub-65-nm CMOSTechnologies", IEEE Trans. Very Large-Scale Integration (VLSI) Systems,vol. 15, no. 12, DEC. 2007.

A circuit technique is proposed in this paper for simultaneously reducing the subthreshold and gate oxide leakage power consumption in domino logic circuits. Only p–channel sleep transistors and a dual-threshold voltage CMOS technology are utilized to place an idle domino logic circuit into a low leakage state. Sleep transistors are added to the dynamic nodes in order to reduce the subthreshold leakage current by strongly turning off all of the high-threshold voltage transistors. Similarly, the sleep switches added to the output nodes suppress the voltages across the gate insulating layers of the transistors in the fan-out gates, thereby minimizing the gate tunneling current. The proposed circuit technique lowers the total leakage power by up to 77% and 97% as

compared to the standard dual-threshold voltage domino logic circuits at the high and low die temperatures, respectively. Similarly, a 22% to 44% reduction in the total leakage power is observed as compared to a previously published sleep switch scheme in a 45-nm CMOS technology. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by providing a net savings in total energy consumption during short idle periods.

Zhiyu Liu, Volkan Kursun, "Leakage Power Characteristics of Dynamic Circuits in Nanometer CMOS Technologies", IEEE Trans. Circuits and Systems-II, vol. 53, no. 8, 2006.

Temperature-dependent subthreshold and gate-oxide leakage power characteristics of domino logic circuits under the influence of process parameter variations are evaluated in this paper. Preferred input vectors and node voltage states that minimize the total leakage power consumption are identified at the lower and upper extremes of a typical die temperature spectrum. New low-leakage circuit design guidelines are presented based on the results. Significantly increased gate dielectric tunneling current, as described in this paper, dramatically changes the leakage power characteristics of dynamic circuits in deeply scaled nanometer CMOS technologies. Contrary to the previously published techniques, a charged dynamic-node voltage state with low inputs is preferred for reducing the total leakage power consumption in the most widely used types of single- and dual-threshold voltage domino gates, particularly at low die temperatures. Furthermore, leakage power savings provided by the dual-threshold voltage domino logic circuit techniques based on input gating are all together reduced due to the significance of gate dielectric tunneling in sub-45-nm CMOS technologies.

Sharroush, S. M., Abdalla, Y. S., Dessouki, A. A. El-Badawy, E. S. A., "A novel low-power and high-speed dynamic CMOS logic circuit technique" IEEE conference In Radio Science Conference, National pp. 1-8, 2009.

Domino CMOS logic finds a wide variety of applications due to their high speed and low device count. In conventional CMOS domino logic, either the dynamic-node capacitor, CL is precharged to VDD during the precharge phase or predischarged to 0 V. The first precharging scheme is more suitable when logic "0" occurrence is more probable at the output due to the large saving in power consumption. On the other hand, the second predischarging scheme is more suitable when logic "1" is more probable at the output. In this paper, we will propose a novel technique to speed up the operation and minimize power consumption when there is an equal probability of occurrence of logic "0" and logic" 1". This technique depends on precharging the dynamic node to VDD/2 instead of VDD during the precharge phase. Then, during the evaluation phase, the dynamic-node voltage will be either increased to VDD or decreased to 0 V depending on the state of the inputs. This, of course, saves much of the time and power consumption because discharging the dynamic node from VDD/2 to 0 V is much faster and consumes less power consumption than discharging it from VDD to 0 V. Also, the discharging process and noise margin will be enhanced by virtue of the fact that the time interval during which the keeper combats the discharging process is relatively very small. The proposed technique will be simulated for the 0.13 urn technology with VDD=1.2 V. Simulation results show that about 75% was shaved from the cycle time for the case of "0" and "1" outputs at the expense of an additional silicon area.

D.Shete and A.Askhedkar. "Design of Low Power Full Adder Circuits Using CMOS Technique",2019 3rd International Conference on Recent Development in Control, Automation & Power Engineering (RDCAPE), 2019 , pp. 293-296.

1-bit different full adder circuits are designed using CMOS technique for low power consumption and less delay. These are implemented using Cadence Virtuoso at 180nm technology for 1.8V supply voltage. The parametric constraints such as power consumption, delay, area are compared with designed different full adder circuits and commented on which

design gives best performance parameter. Power Delay Product defines the efficiency of the circuit. As low power design is the main research in VLSI, hence design the circuits which require low power, less area, less delay. The performance of complete design appertains to the performance of full adder circuit design.

CHAPTER 2: TECHNOLOGY

Two design techniques will be used for the analysis of full - adder circuit, namely CMOS based logic style and domino-based logic and provided their comparative results. An adder is a digital circuit that is used for performing the addition of numbers. In calculator and computers, adders are used in arithmetic and logic units. This combinational circuit takes three inputs which are one-bit each, named as A, B and C. It has two outputs named as the sum and the carry as shown in Fig. 2.1.

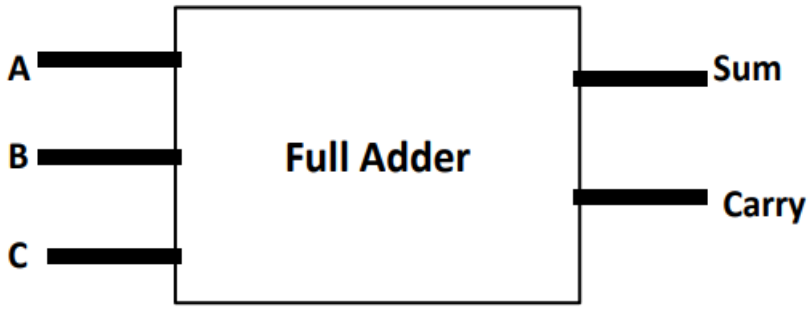

Fig. 2.1. Block diagram of one- bit full adder

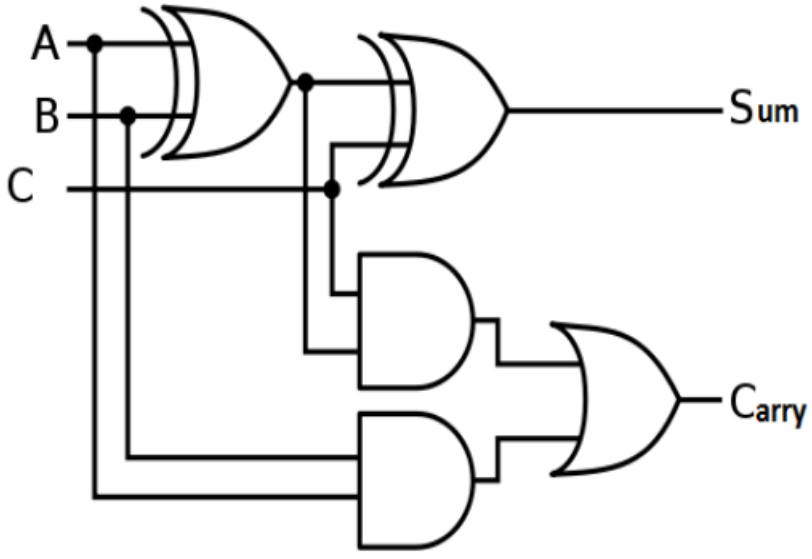

Fig. 2.2. Logic diagram of one-bit full adder

The gate level logical diagram of one- bit full adder has been shown in Fig.2.2 which uses the two X-OR gate for the sum, two AND gate and one OR gate for carry. The output of the two AND gate is used as an input of OR gate and the output of OR gate is providing the carry of one-bit full adder. Table I shows the truth table for full adder designed using CMOS based logic.

TABLE 2. FULL ADDER TRUTH TABLE

Inputs			Outputs	
A	**B**	**C**	**Sum**	**Carry**
Low	*Low*	*Low*	*Low*	*Low*
Low	*Low*	*High*	*High*	*Low*
Low	*High*	*Low*	*High*	*Low*
Low	*High*	*High*	*Low*	*High*
High	*Low*	*Low*	*High*	*Low*
High	*Low*	*High*	*Low*	*High*
High	*High*	*Low*	*Low*	*High*
High	*High*	*High*	*High*	*High*

Designing of one- bit full adder based on CMOS logic. This circuit uses the 14 p-MOS transistors which are used for charging the output capacitance and 14 n-MOS transistors for discharging the output node according to value of inputs.

So, there is total 28 number of transistors used in designing of one- bit full adder which uses the CMOS logic style. It is very difficult and complex to design one- bit full adder as it consists large number of transistors. There are large number of wires used for providing the connection between the transistors which introduce large delay in the circuit.

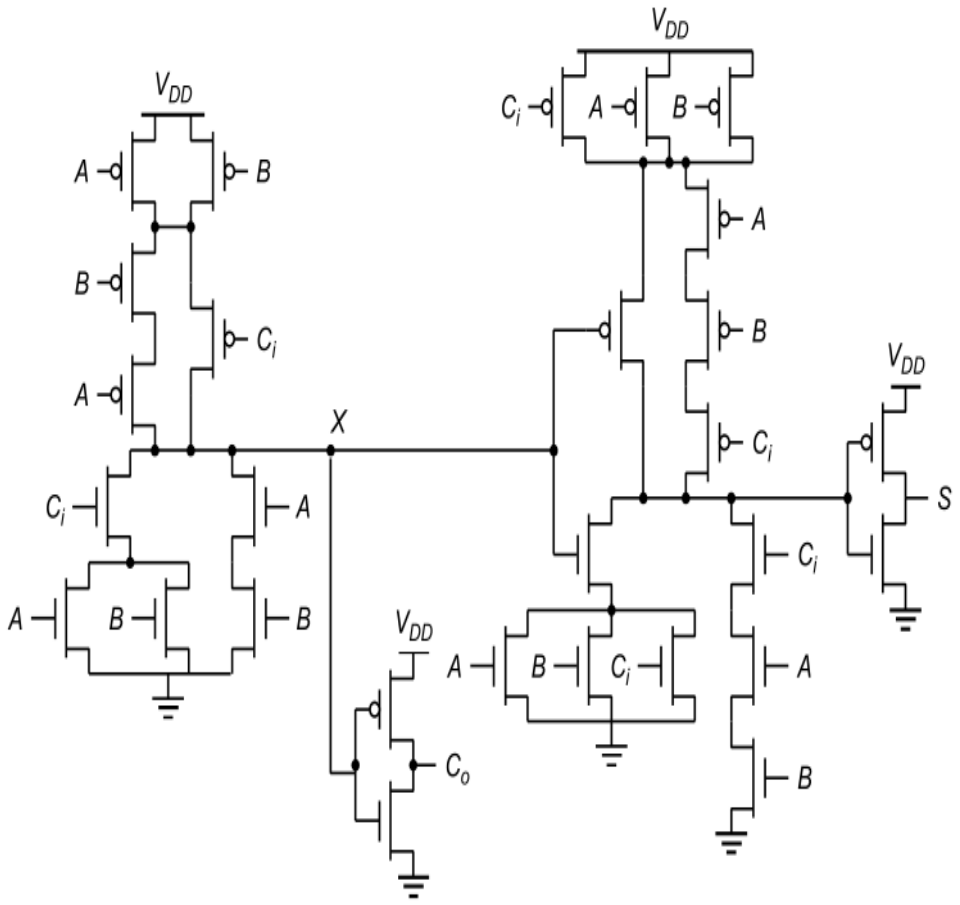

Fig. 2.3. One-bit full adder using 28 Transistors

CHAPTER 3: CHALLENGES

3.1 Disadvantages

- More number of transistors due to CMOS technology.
- Large delay
- More Power Consumption

CHAPTER 4: SOLUTIONS

4.1 Proposed System

The domino logic is an improvement in dynamic logic which has a drawback when one gate is cascaded to next in domino logic. A static inverter is used between the two stages for removing the drawback of dynamic logic. There are various advantages of Domino logic like they have a smaller area unlike conventional CMOS logic, parasitic capacitance are smaller in domino logic so it provide high speed of operation and result is glitch free because each gate makes only one transition.

Domino logic style is generally used for designing a high-performance circuit, rather than a static logic style. For arithmetic operations full adder acts as a basic element for parity checker, comparator, and multiplier, hence it receives a lot of attention by the researchers.

For designing a full adder there are two logic approaches first is static and the second is dynamic. A dynamic full adder is faster and more compact, consumes less silicon area, but it consumes more power and more sensitive to noise as compared to static full adder. To design an efficient full adder, there are lots of constraints, i.e. power consumption, performance of the circuit, transistor count, area, noise immunity and good driving ability. There are three major contributions to power consumption in CMOS circuits. One is the active power due to discharging and charging of the circuit capacitances during switching and the other is leakage power due to leakage current and the third is short circuit currents that flow directly from the supply to ground when the n-subnetwork and the p-subnetwork of a CMOS gate both conduct simultaneously.

Domino logic consists of two- stages of operation in which first stage is pre-charging, and another stage is evaluation. When clock ‘clk’ is equal to zero or low p-MOS will be on, and it pre-charged the output node to Vdd. When the clk goes to high, p-MOS will be off, and the evaluation phase will start. In this phase output will depend on the input’s configuration. Output

node may discharge if inputs have a direct conducting path to ground otherwise it will remain high. So, the output of circuit is obtained by which it has been intended to design in evaluation phase only. In pre-charge phase, it will provide low output because we used an inverter in this logic style for cascading the next stage.

Domino logic family find a wide variety of applications where less transistor count and high speed of operation such as microprocessor, dynamic memory, digital signal processor etc. are required. Domino logic is an evolution in CMOS based dynamic logic techniques which use either p-MOS or n-MOS for the pull down or pull up network. The methodology of designing full adder by using Domino logic employs lesser no. of transistors as if compared to conventional CMOS logic and provides high performance device.

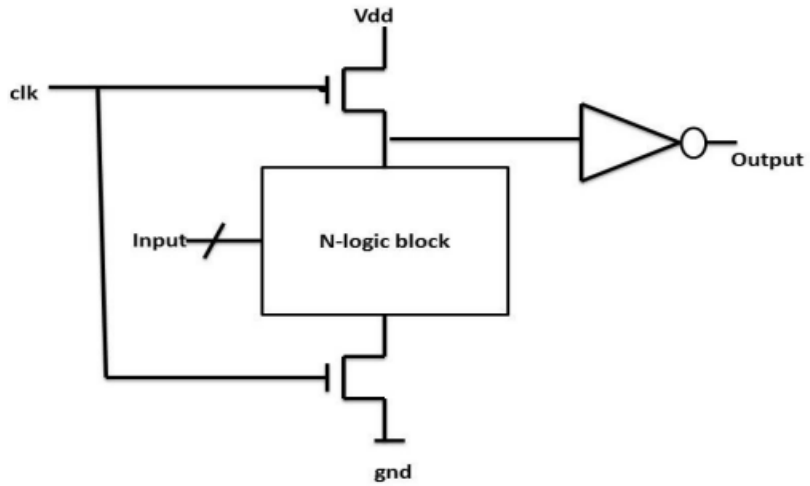

Fig. 4.1. Domino logic

Design of one- bit full adder using Domino logic- The one-bit full adder schematic using Domino logic is shown in Fig. 6. For designing the one-bit full adder by using domino logic we use the p-MOS transistors for the pre-charge phase and inverter, rest we used the n-MOS transistors for evaluation phase.

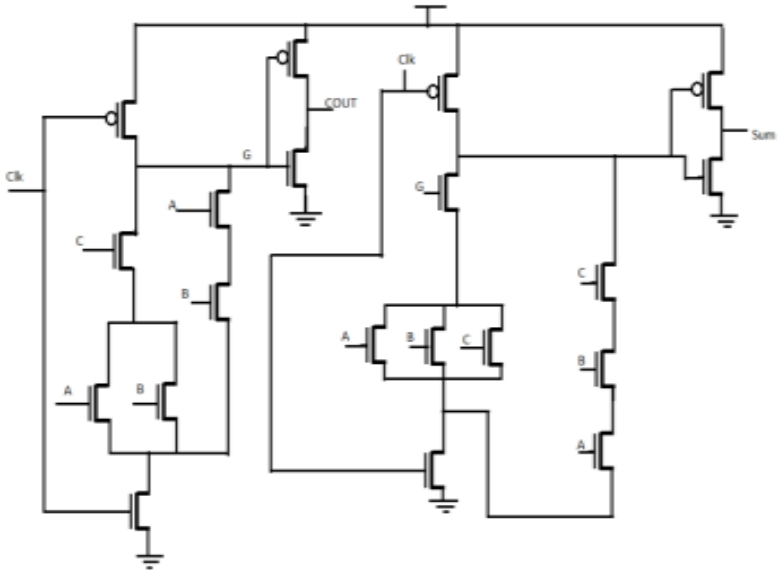

Fig. 4.2. One-bit full adder using 20 Transistors

In this logic style we have used 4 p-MOS transistors and 16 n-MOS transistors. So, there are a total 20 transistors being used in designing the adder circuit by using Domino logic.

4.2 Advantages

- Less number of transistors is required as only nmos logic is used
- Less delay is achieved due to domino logic
- Less power consumption

4.3 Results

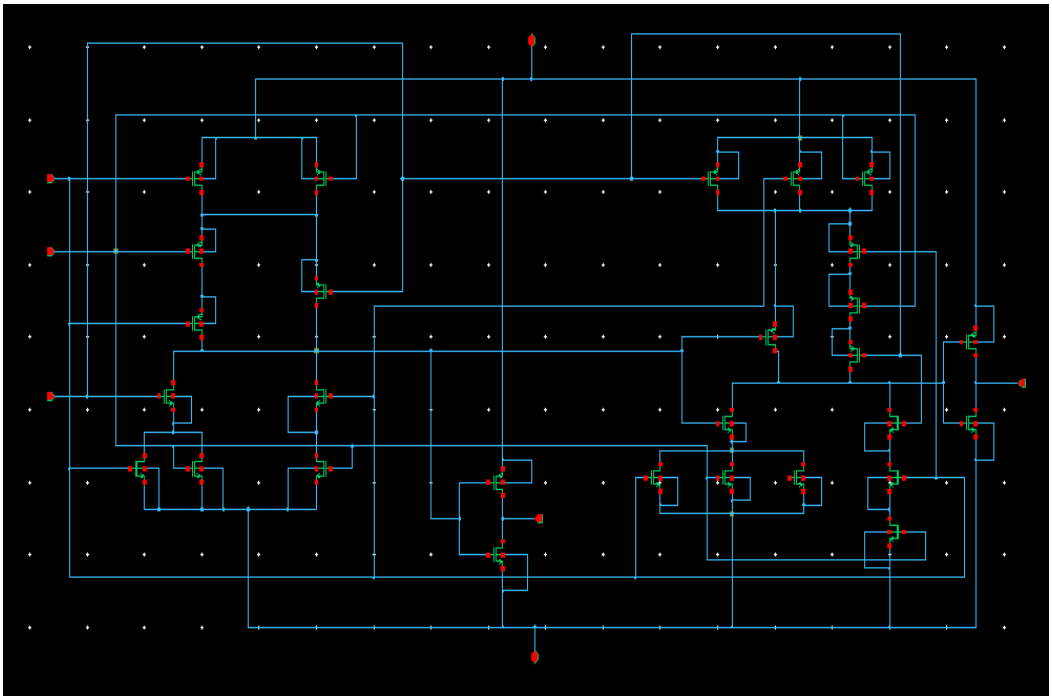

Fig. 4.3.1. Schematic of one-bit full adder using 28T based on CMOS logic

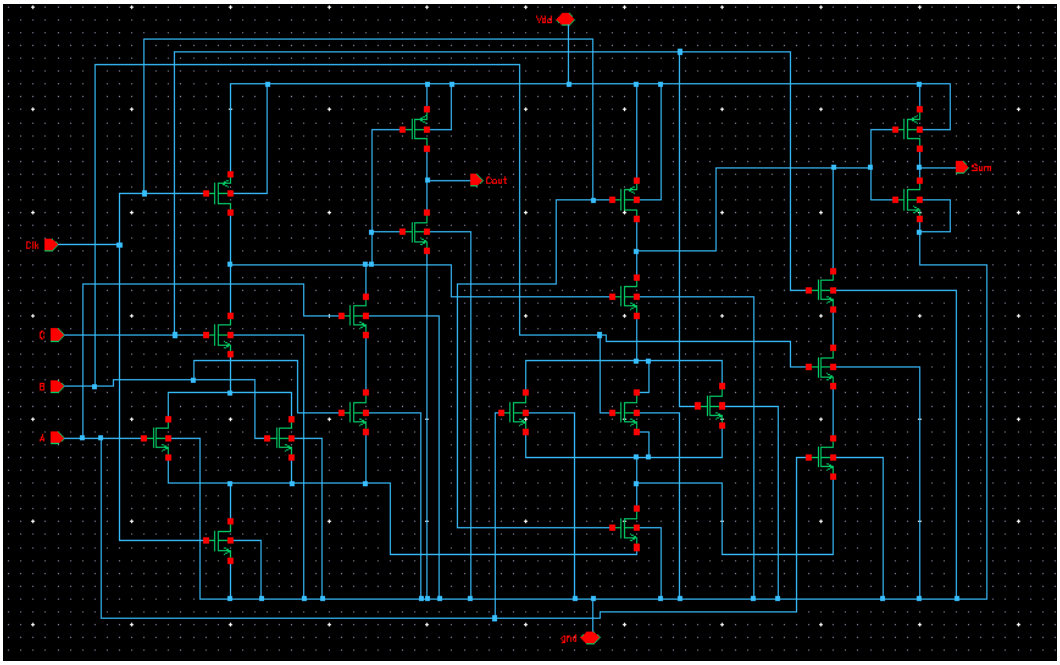

Fig. 4.3.2. Schematic of Domino full adder using 20T

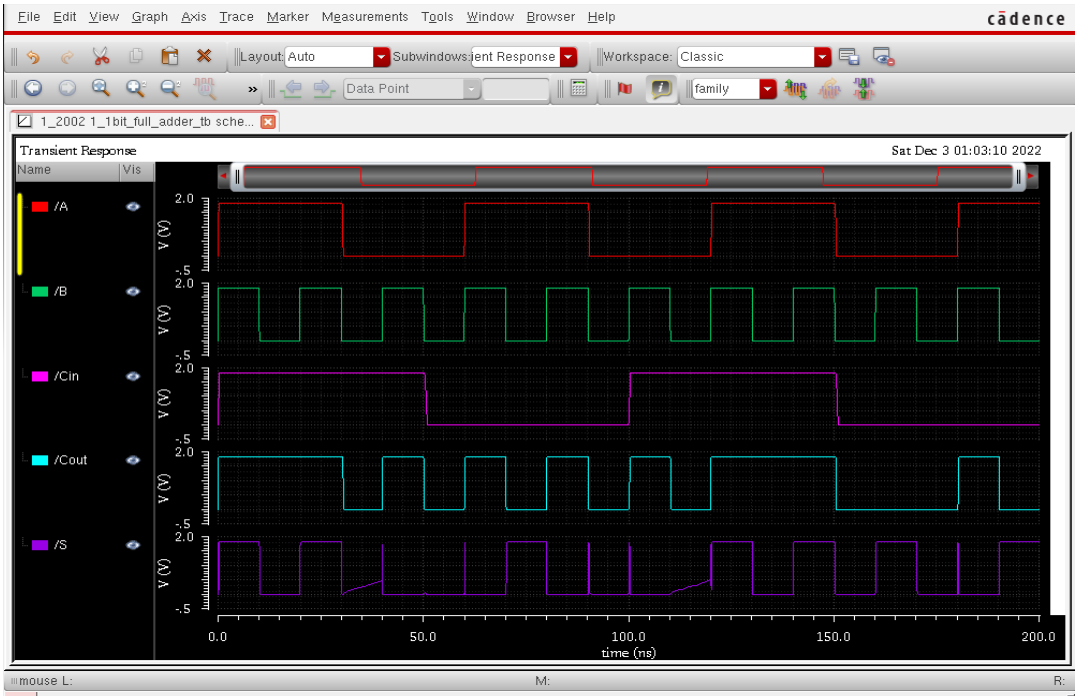

Fig. 4.3.3. Simulated result of FA based on CMOS logic

Fig. 4.3.4. Simulated result of FA using 20T based on domino logic

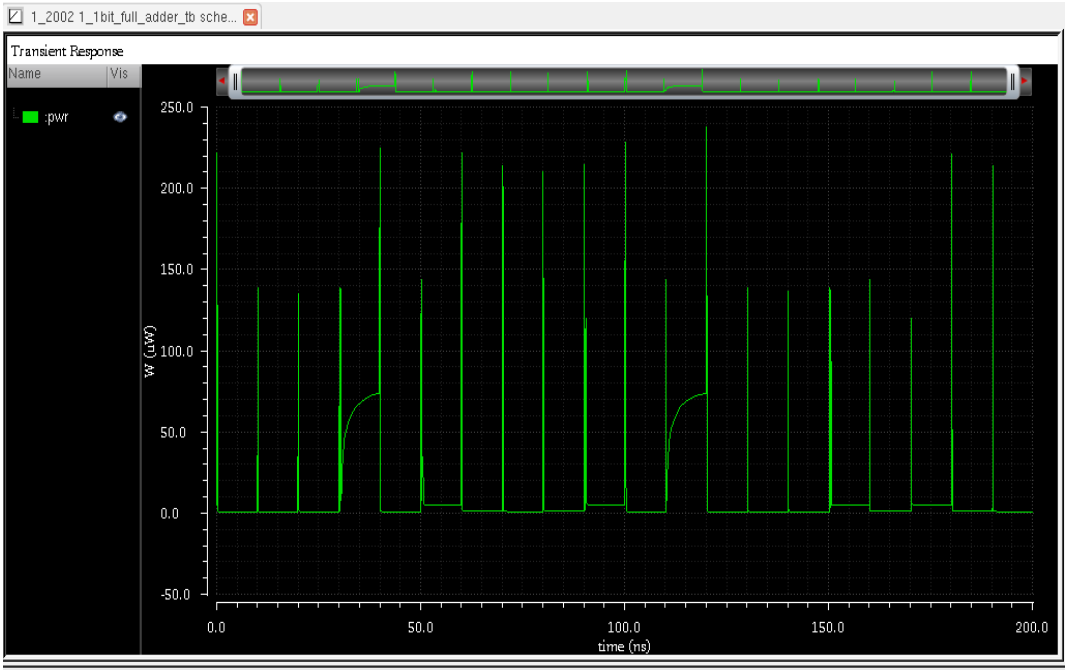

Fig. 4.3.5. Simulated power analysis result of FA based on CMOS logic

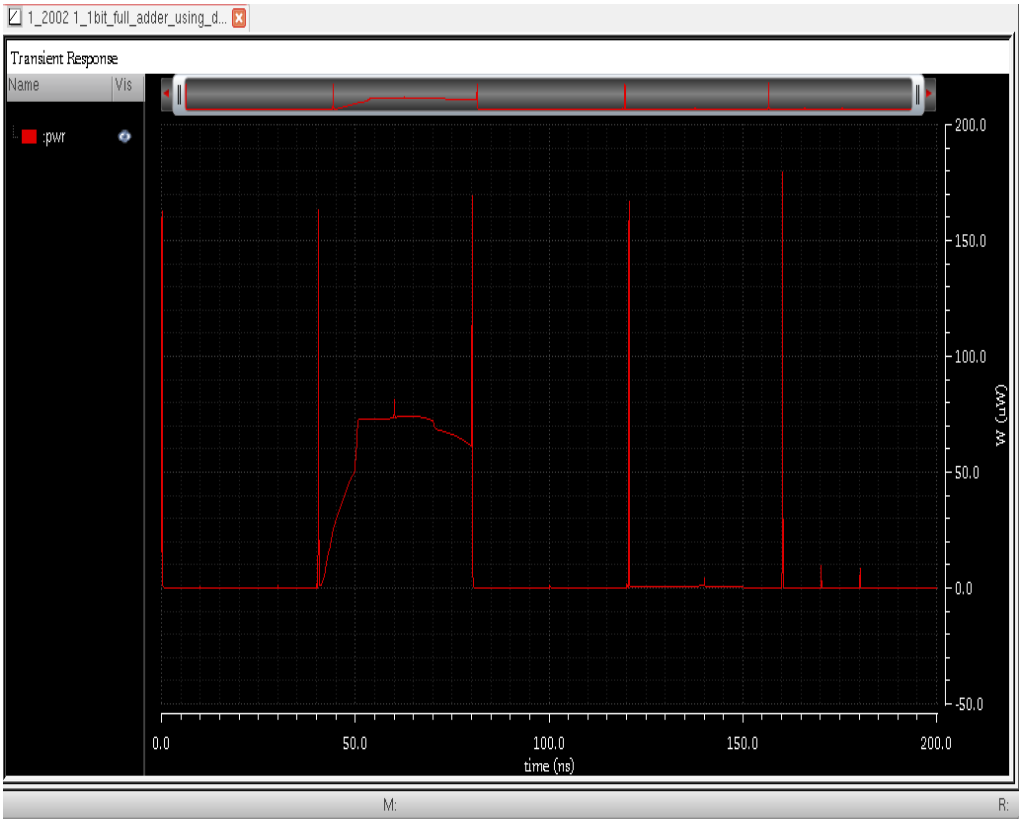

Fig. 4.3.6. Simulated power analysis result of FA using 20T based on domino logic

TABLE 4. Comparison of CMOS Full adder and Domino Full Adder in terms of Power , Area and Delay

Design	Area	Average Power	Average Delay
CMOS Full Adder	**28 transistors**	**9.83 µW**	
Domino Full Adder	**20 transistors**	**12.88 µW**	

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 Conclusion:

In this paper designing of full adder circuit using the CMOS logic and Domino logic has been done. We used Cadence Virtuoso software, 90nm technology for analyzing the full adder circuit. It was found that Domino logic gives us very accurate results with a smaller number of transistors and minimum delay as compare to the CMOS design logic. There are almost no glitches in Domino logic transient analysis. Further there is a decrease in chip area and delay in Domino logic as compared to CMOS logic. Further, as shown in the power graph of CMOS logic and Domino logic it was observe that instantaneous power is more in CMOS based logic as compared to the Domino logic so there are more chances of device failure in CMOS logic as compared to the Domino logic

5.2 Future Scope:

To extend this concept, we may change the different configurations of Full adders using PTL, Transmission Gate, GDI by using Domino logic.

CHAPTER 6: REFERENCES

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