HKN ECE 110 Review Session Exam 3

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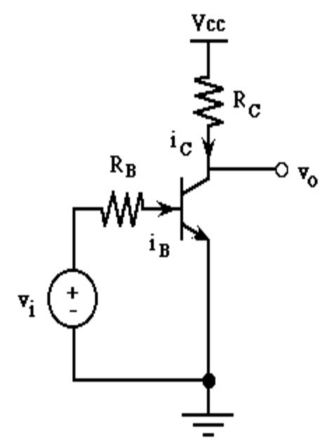
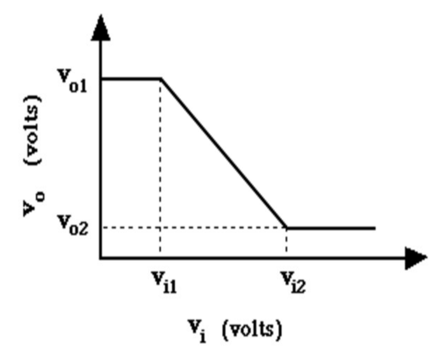
Quick Announcement

- HKN PHYS 212 Exam 3 Review Session
  - Sunday, 4/22, 2-4pm in ECEB 1013

BJT Transfer Characteristic

- The transfer characteristic of a BJT relates the output voltage, $V_{CE} = V_o$, to its input voltage, V_i.
- We can deduce the regions of operation and thus the important values from the graph
- $V_{o1} = V_{CC}$
- $V_{o2} = V_{CE,SAT}$
- $V_{i1} = V_{BE,ON}$
- $V_{i2} = V_i^* =$ minimum input to enter saturation
- Gain $= G = -\frac{\beta R_C}{R_B} =$ slope in active region





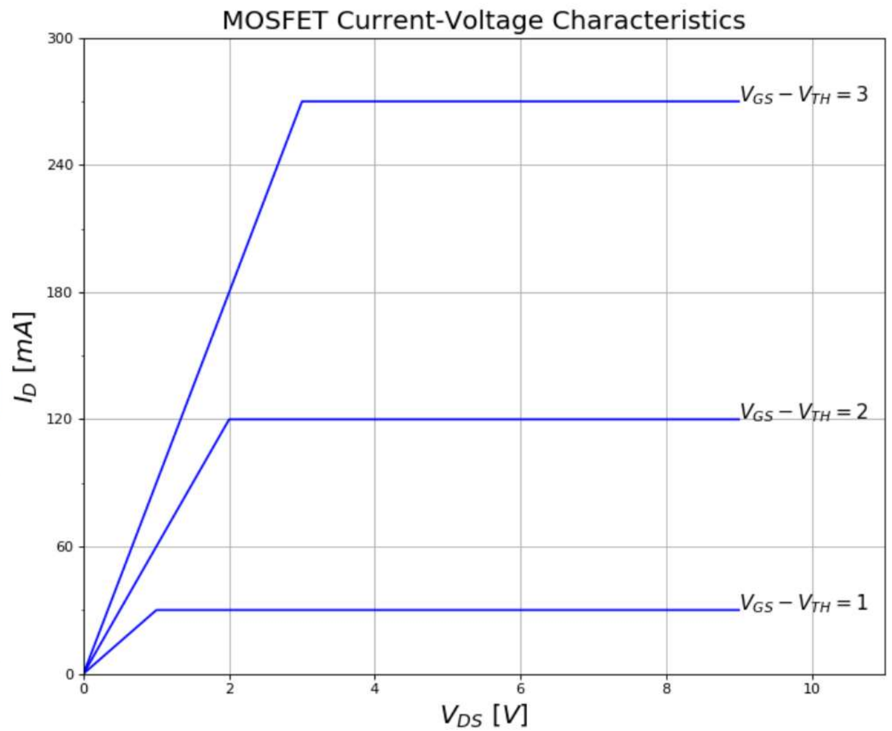
BJT Power

- In order to calculate the power of a BJT, we consider the power contributed by each junction we analyze: Base-Emitter and Collector-Emitter
- $P_{BJT} = V_{BE,ON} I_B + V_{CE} I_C$
- If the BJT is off, power is zero.
- We must check to see if the transistor is in the active or saturated region as usual
- Notice that the Base-Emitter (1st) term is typically much smaller than the Collector-Emitter (2nd) term since $I_C \gg I_B$ due to β

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

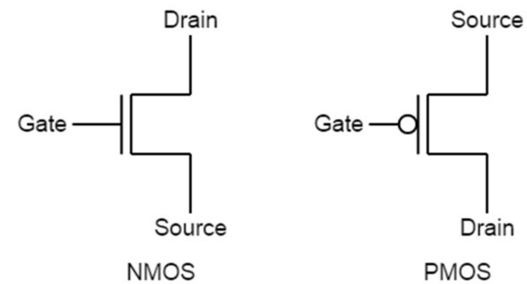
- Three terminal device: gate, source, drain
- Comes in two flavors, nMOS and pMOS
- V_{TH} is a property of the specific MOSFET
- Be comfortable interpreting I-V Characteristic of MOSFET

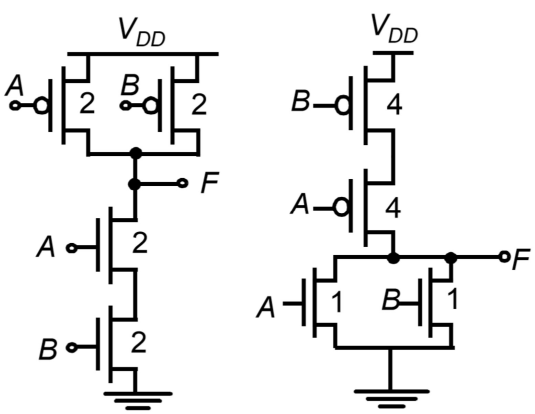
Conditions	Mode	Behavior under Linear Model
$V_{GS} < V_{TH}$	OFF	$I_D = 0$
$V_{GS} > V_{TH}$ $V_{DS} > V_{GS} - V_{TH}$	ACTIVE	$I_D = k(V_{GS} - V_{TH})^2$
$V_{GS} > V_{TH}$ $V_{DS} < V_{GS} - V_{TH}$	OHMIC	$I_D = k(V_{GS} - V_{TH})V_{DS}$



Complementary MOS Logic (cMOS)

- Combine NMOS and PMOS transistors in order to perform a logical operation
  - i.e. AND, NOR, NOT
- NMOS and PMOS are biased differently
  - NMOS, source connects to ground; PMOS, source connects to V_{DD}

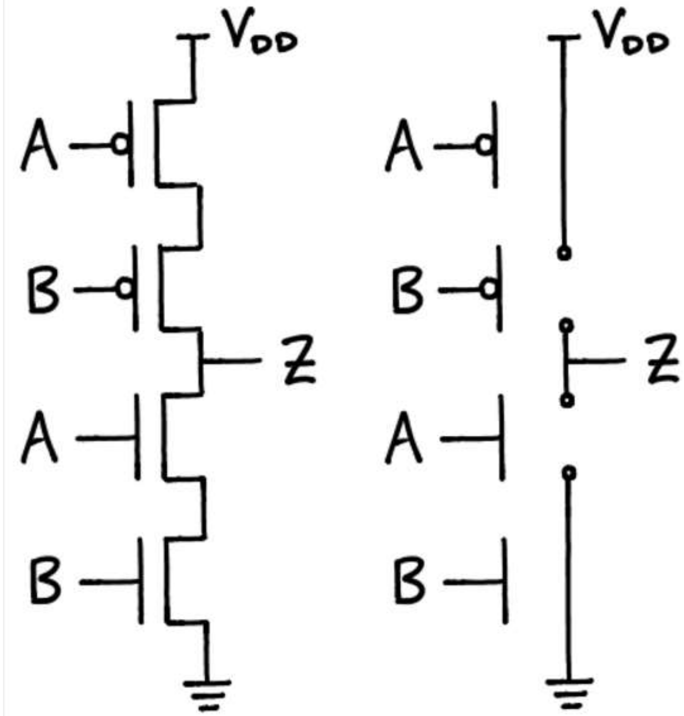




Input (@ Gate)	nMOS	pMOS
0	Non-Conducting	Conducting
1	Conducting	Non-Conducting

Improper CMOS

- A CMOS circuit is considered *proper* if:
  - The output can only be connected to one of V_{DD} **or** Ground at a time
- A CMOS circuit is considered *improper* if:
  - The output can be connected to both V_{DD} **and** Ground simultaneously by some input combination
  - The output can be connected to neither V_{DD} **nor** Ground simultaneously by some input combination



CMOS Power

$$P = nafCV_{DD}{}^{2}$$

- n = number of capacitors/transistors
- a = activity factor
- f = frequency
- C = capacitance
- V_{DD} = supplied voltage

Signal-to-Noise Ratio (SNR)

- Signal-to-Noise Ratio gives us an understanding of the amount of noise distortion in a system
- $SNR = \frac{P_{signal}}{P_{noise}}$
- Remember that the average power for a time-varying signal requires V_{rms}
- $P_{avg} = \frac{V_{rms}^2}{R},\ V_{rms}(sine) = \frac{A}{\sqrt{2}},\ V_{rms}(sq.wave) = A\sqrt{Duty\ Cycle}$
- We can also express SNR as follows
- $SNR = \frac{P_{signal}}{P_{noise}} = \frac{\frac{V_{rms,signal}^2}{R}}{\frac{V_{rms,noise}^2}{R}} = \left(\frac{V_{rms,signal}}{V_{rms,noise}}\right)^2$

Sampling

- When we convert from a continuous-time analog signal (function of time) to a discrete-time digital signal (function of n), we are performing sampling, or Analog/Digital (A/D) conversion

- We relate the sampled (digital) signal to the original (analog) signal by:

$$x[n] = x(nT_s)$$

- n is the index for the “nth” sample, T_s is the sampling period

Wise Words to Make your Score Soar

- Use your note sheet more like a study tool
- Spend your time showing what you know
- Make sure to get through the whole exam
- Take the time to relax before your exam