UNITED INTERNATIONAL UNIVERSITY (UIU)

Dept. of Computer Science & Engineering

Trimester: Summer 2023

Final Exam

Course No: CSE 1326 Title: DLD LAB

Section: D

Time: 20 minutes **Marks: 25**

Name		**ID**	

(Just Put a single tick mark on the right option in the MCQ Question, if you double tick in any MCQ Question, you will get zero in that question) [MCQ: 6×2.5=15 marks]

1). If output of X-NOR gate is 1, what are the inputs?

a) A = 0, B = 1
b) A = 1, B = 0
c) A' = 0, B = 0
d) A = 0, B = 0

2). For a sequence recognizer to detect a bit pattern of **"0010"**, the states are s0, s1, s2 & s3. If the value of input x = 0 for state s2, what will be output and next state?

a) output 0, state: s3
b) output 1, state: s3
c) output 0, state: s2
d) output 1, state: s2

3). What are the inputs of a 4-bit full adder if the carry-in is '1' and output is '10010'?

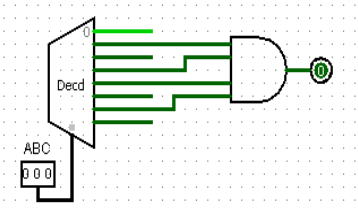
a) 1011 & 0111
b) 1010 & 1000
c) 1111 & 1110
d) 0110 & 1011

4). Suppose, you're designing a data transmission system where you need to choose between 8 different data sources based on a control signal. Which digital component would allow you to select one of the 8 data sources with how much selection bit?

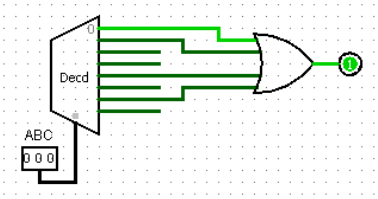
a) Multiplexer, number of selection bit: 3
b) Decoder, number of selection bit:3
c) Multiplexer, number of selection bit: 2
d) Decoder, number of selection bit:2

5). What will be logic diagram for F = m2+m3+m5+m7 by using 3-to-8 line active low decoder? **(Right answer: C)**

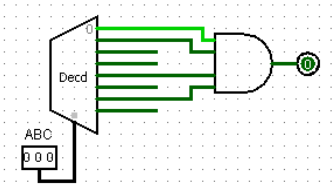
a)



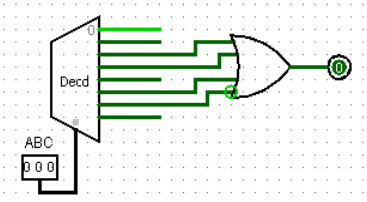
b)



c)



d



6). What is the simplification for the following Boolean expression, F = AB + A'B + AB'.

a) A + B
b) AB' + B
c) A'B + A

d) A’ + B

[Written: 2×5=10 marks]

7) Draw the state diagram for a sequence recognizer that can detect the pattern 010 considering the overlapping pattern.

8) Draw the circuit diagram of a counter using negative edge D Flipflop that has the following sequence: 1, 2, 3, 4, ……31, 0, 1, 2, …..