**REQUIREMENTS NOT MET**

<insert any requirements not met, if applicable (if not applicable, write “N/A”)>

**PROBLEMS ENCOUNTERED**

<insert a brief summary of *all* problems encountered>

**FUTURE WORK/APPLICATIONS**

<insert a brief paragraph describing how the topics covered in this lab could potentially be used for other applications>

THE ABOVE SHOULD BE LIMITED TO THE FIRST PAGE, AND NOTHING ELSE SHOULD BE INCLUDED, WHICH ALSO IMPLIES THAT THIS SENTENCE OF TEXT SHOULD BE REMOVED.

**PRE-LAB EXERCISES**

**i. Which configuration register allows the utilization of an I/O port pin configured as an input? Which configuration registers allow the utilization of an I/O port pin configured as an output?**

**The “in” register of a port allows you to read the port as input.  
 The “out” register of a port allows you to output vales at certain pins.  
 The “outset” register writes a “high” signal to whichever bits are set to “1”  
 The “outclr” register writes a “low” signal to whichever bits are set to "1”  
 The “outtgl” register toggles a signal to whichever bits are set to "1”**

**ii. What is the purpose of the SET/CLR/TGL variants of the DIR and OUT registers?**

**The purpose is to allow you to adjust the signal levels of individual pins without   
Affecting other pins**

**iii. Are the LEDs on the OOTB Switch & LED Backpack active-high, or active-low? Draw a schematic diagram for a single LED circuit with the same activation level used on the backpack, as well as one with the opposite activation level. Also, draw a schematic diagram for a single-pole, single-throw (SPST) switch circuit, using the same pull-up or pull-down resistor condition utilized on the backpack, as well as another switch circuit using the opposite configuration.**

**Led’s are active-low.  
A picture containing sketch, drawing, line art, diagram

Description automatically generated**

**iv. Which I/O ports are utilized for the DIP switches and LEDs on the OOTB Switch & LED Backpack?**

**The led circuits utilize port C  
 The switch circuit utilizes port A**

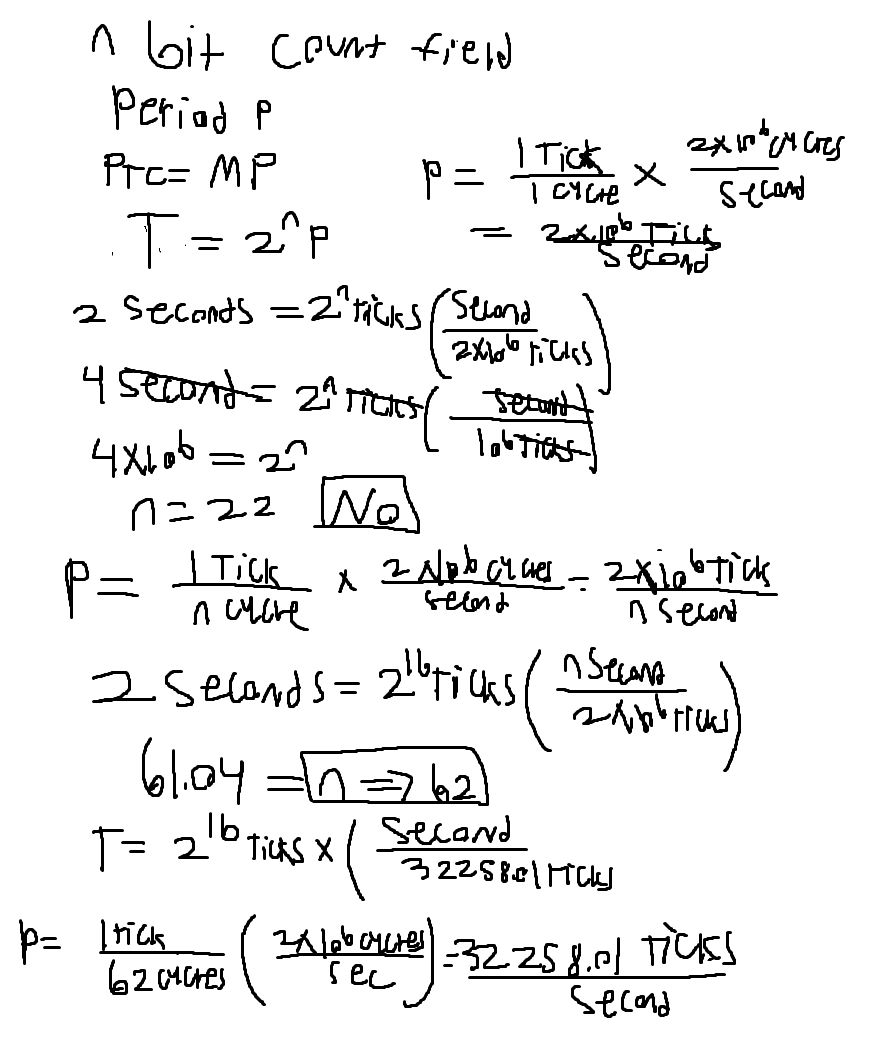
**v. Would it be possible to interface the OOTB µPAD with an external input device consisting of 24 inputs? If so, describe how many I/O ports would be necessary. If not, explain why.**

**The OOTB has 3 ports with 8 pins each. All ports are configurable as inputs. Therefore, it should  
be possible to connect a 24-pin input device.**

**vi. Assuming a system clock frequency of 2 MHz, a prescaler value of 8, and a desired period of 72 ms, calculate a theoretically-corresponding timer/counter period value two separate times: once using a form of dimensional analysis, providing explanation(s) when appropriate, and another time using the general formula provided within The Most Common Use Case for Timer/Counters.  
A picture containing text, handwriting, font, calligraphy

Description automatically generated**

**vii. Assuming a system clock frequency of 2 MHz, is a period of two seconds achievable when using a 16-bit timer/counter prescaler value of one? If not, determine if there exists any prescaler value that allows for this period under the assumed circumstances, and if there does, list such a value.**

****

**viii. What is the maximum time value (to the nearest millisecond) representable by a timer/counter, if the relevant system clock frequency is 2 MHz? What about for a system clock frequency of 32.768 kHz?**

A picture containing text, handwriting, font, calligraphy

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**PSEUDOCODE/FLOWCHARTS**

**SECTION 1**

A diagram of a flowchart

Description automatically generated with low confidence **Figure 1:Flowchart for “lab2\_1.asm”. This copies  
the switch circuit register values to the   
output registers for the LED’s**

**SECTION 2**

**A diagram of a flowchart

Description automatically generated with low confidence  
Figure 2: Flowchart for “lab2\_2.asm” with “delay\_10ms” being the only subroutine.  
This toggles pin 0 of port C every 10ms, giving us a 10ms PWM signal.**

**A diagram of a flowchart

Description automatically generated with low confidence  
Figure 3: Flowchart for “delay\_10ms” subroutine.  
“FAUS” creates a delay of 250us by executing 500 single cycle instructions.  
 “ONEKUS” creates a 1000us delay by running “FAUS” 4 times.  
“TENMS” creates a 10000us delay by running “ONEKUS” 10 times.  
Giving us a delay of 10ms.**

**A picture containing text, diagram, screenshot, line

Description automatically generated  
Figure 4: Flowchart for “delay\_X\_10ms”.  
R21 is the multiple of 10ms delays.**

**PROGRAM CODE**

**SECTION 1**

;Lab 2, Section 1

;Name: Steven Miller

;Class #: 11318

;PI Name: Anthony Stross

;Description: Allows control of LED's through switch circuit

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.include "ATxmega128a1udef.inc"

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.EQU INPUT = 0B00000000

.EQU OUTPUT = 0B11111111

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*MEMORY CONFIGURATION\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*END OF MEMORY CONFIGURATION\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.CSEG

.org 0x0100

MAIN:

;set port directions

LDI R16, INPUT

STS PORTA\_DIR , R16

LDI R16, OUTPUT

STS PORTC\_DIR , R16

;loop for actual led and switch circuits

LOOP:

;copy load value from switch registers into led registers

LDS R16, PORTA\_IN

STS PORTC\_OUT,R16

RJMP LOOP

;\*\*\*\*\*\*\*\*\*\*\*END MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**Section 2  
Original code to create software delay of 10ms**

;Lab 2, Section 2

;Name: Steven Miller

;Class #: 11318

;PI Name: Anthony Stross

;Description: Implements software delays

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.include "ATxmega128a1udef.inc"

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.EQU sramend = 0x3fff ;top of stack

.EQU srambegin = 0x2000 ;bottom of stack

.EQU input = 0b00000000

.EQU output = 0b11111111

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.DEF ms\_r16 = r16

.DEF us\_r17 = r17

.DEF zero\_r18 = r18

.DEF one\_r19 = r19

.DEF four\_r20 = r20

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.CSEG

.org 0x0100

MAIN:

;initialize stack pointer

ldi r16, low(sramend)

out CPU\_SPL, r16

ldi r16, high(sramend)

out CPU\_SPH, r16

;set port directions

LDI R22, output

STS PORTC\_DIR , R22

;initialize registers

ldi zero\_r18,0

ldi one\_r19,1

ldi four\_r20,4

;loop to call subroutine

LOOP:

rcall delay\_10ms

STS PORTC\_OUTTGL,R22

RJMP LOOP

;\*\*\*\*\*\*\*\*\*\*\*END MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*SUBROUTINES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Subroutine Name: delay\_10ms

; performs a series of instructions for 10ms

; Inputs: none

; Ouputs: none

; Affected: r16, r17,r19,r20

delay\_10ms:

ldi ms\_r16,0

ldi us\_r17,0

tenms:

ldi four\_r20, 0

;1ms

onekus:

ldi us\_r17,0

;250us

faus:

add us\_r17,one\_r19

cpi us\_r17,250

brne faus

add four\_r20,one\_r19

cpi four\_r20,4

;branch if 1ms

brne onekus

add ms\_r16,one\_r19

;branch if 10 ms

cpi ms\_r16,10

brne tenms

ret

**Code after adjustment**

;Lab 2, Section 2

;Name: Steven Miller

;Class #: 11318

;PI Name: Anthony Stross

;Description: Implements software delays

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.include "ATxmega128a1udef.inc"

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.EQU sramend = 0x3fff ;top of stack

.EQU srambegin = 0x2000 ;bottom of stack

.EQU input = 0b00000000

.EQU output = 0b11111111

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.DEF ms\_r16 = r16

.DEF us\_r17 = r17

.DEF zero\_r18 = r18

.DEF one\_r19 = r19

.DEF four\_r20 = r20

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.CSEG

.org 0x0100

MAIN:

;initialize stack pointer

ldi r16, low(sramend)

out CPU\_SPL, r16

ldi r16, high(sramend)

out CPU\_SPH, r16

;set port directions

LDI R22, output

STS PORTC\_DIR , R22

;initialize registers

ldi zero\_r18,0

ldi one\_r19,1

ldi four\_r20,4

;loop to call subroutine

LOOP:

rcall delay\_10ms

STS PORTC\_OUTTGL,R22

RJMP LOOP

;\*\*\*\*\*\*\*\*\*\*\*END MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*SUBROUTINES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Subroutine Name: delay\_10ms

; performs a series of instructions for 10ms

; Inputs: none

; Ouputs: none

; Affected: r16, r17,r19,r20

delay\_10ms:

ldi ms\_r16,0

ldi us\_r17,0

tenms:

ldi four\_r20, 0

;1ms

onekus:

ldi us\_r17,0

;250us

faus:

add us\_r17,one\_r19

cpi us\_r17,253

brne faus

add four\_r20,one\_r19

cpi four\_r20,2

;branch if 1ms

brne onekus

add ms\_r16,one\_r19

;branch if 10 ms

cpi ms\_r16,10

brne tenms

ret

**Including “delay\_x\_10ms” subroutine. Delays for .04s.**

;Lab 2, Section 2

;Name: Steven Miller

;Class #: 11318

;PI Name: Anthony Stross

;Description: Implements software delays

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.include "ATxmega128a1udef.inc"

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF INCLUDES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.EQU sramend = 0x3fff ;top of stack

.EQU srambegin = 0x2000 ;bottom of stack

.EQU input = 0b00000000

.EQU output = 0b11111111

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF EQUATES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.DEF ms\_r16 = r16

.DEF us\_r17 = r17

.DEF zero\_r18 = r18

.DEF one\_r19 = r19

.DEF four\_r20 = r20

.DEF multiple\_r21 = r21

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*END OF DEFS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.CSEG

.org 0x0100

MAIN:

;initialize stack pointer

ldi r16, low(sramend)

out CPU\_SPL, r16

ldi r16, high(sramend)

out CPU\_SPH, r16

;set port directions

LDI R22, output

STS PORTC\_DIR , R22

;initialize registers

ldi zero\_r18,0

ldi one\_r19,1

ldi four\_r20,4

ldi multiple\_r21,4

;loop to call subroutine

LOOP:

rcall delay\_x\_10ms

STS PORTC\_OUTTGL,R22

RJMP LOOP

;\*\*\*\*\*\*\*\*\*\*\*END MAIN PROGRAM\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*SUBROUTINES\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Subroutine Name: delay\_10ms

; performs a series of instructions for 10ms

; Inputs: none

; Ouputs: none

; Affected: r16, r17,r19,r20

delay\_10ms:

ldi ms\_r16,0

ldi us\_r17,0

tenms:

ldi four\_r20, 0

;1ms

onekus:

ldi us\_r17,0

;250us

faus:

add us\_r17,one\_r19

cpi us\_r17,253

brne faus

add four\_r20,one\_r19

cpi four\_r20,2

;branch if 1ms

brne onekus

add ms\_r16,one\_r19

;branch if 10 ms

cpi ms\_r16,10

brne tenms

ret

; Subroutine Name: delay\_x\_10ms

; delays a select multiple of 10ms

; Inputs: r21

; Ouputs: none

; Affected: r16,r17,r19,r20,r21

delay\_x\_10ms:

push r21

loopx:

cpi multiple\_r21,0

breq exit

call delay\_10ms

dec multiple\_r21

rjmp loopx

exit:

pop r21

ret

**APPENDIX**

**A screen shot of a graph

Description automatically generated with medium confidence  
Figure x: Software Delay without adjustment. The red underlined is the length of the delay.**

**A screen shot of a graph

Description automatically generated with low confidence  
Figure X: Software Delay after reducing number of times “ONEKUS” runs “FAUS” from 4 to 2**

**A screen shot of a graph

Description automatically generated with medium confidence  
Figure X: Software Delay after reducing number of times “ONEKUS” runs “FAUS” from 4 to 2, while also increasing number of times “FAUS” iterates from 250 to 253.**

**A screen shot of a graph

Description automatically generated with low confidence  
Figure X: .04 second delay**