**REQUIREMENTS NOT MET**

N/A

**PROBLEMS ENCOUNTERED**

N/A

**FUTURE WORK/APPLICATIONS**

<insert a brief paragraph describing how the topics covered in this lab could potentially be used for other applications>

THE ABOVE SHOULD BE LIMITED TO THE FIRST PAGE, AND NOTHING ELSE SHOULD BE INCLUDED, WHICH ALSO IMPLIES THAT THIS SENTENCE OF TEXT SHOULD BE REMOVED.

**PRE-LAB EXERCISES**

**i. For each SRAM configuration within the EBI system of the ATxmega128A1U microcontroller, to which address lines do you have external, physical access? Additionally, for the SRAM 3-PORT ALE1 configuration, is it possible to have external, physical access to any address lines above A15? Why or why not?**

**Normal SRAM Configuration:  
  
 No multiplexing:**

**Address lines 0 through 21**

**Multiplexing byte 0 and 1:**

**If ALE 1 is false, address lines 0 through 7 along with address lines 16 through 19.**

**If ALE 1 is true, address lines 0 through 15 along with 16 through 19 are available.**

**Multiplexing byte 0 and 2:**

**If ALE2 is false, address lines 0 through 15.**

**If ALE2 is true, address lines 0 through 23 are available.**

**Multiplexing byte 0,1 and 2:**

**If both ALE1 and ALE2 are false, address lines 0 through 7 are available.**

**If ALE1 is true and ALE2 is false, address lines 0 through 15 are available.**

**If ALE1 is true and ALE2 is true, address lines 0 through 23 are available.**

**LPC SRAM Configuration:**

**Multiplexing byte 0:**

**If ALE1 is false, address lines 8 through 19 are available.**

**Multiplexing byte 0 and 1:**

**If ALE1 and ALE2 are false, address lines 16 through 19 are available.**

**If ALE1 is true and ALE2 is false, address lines 0 through 7 along with 16 through 19**

**are available.**

**If ALE1 and ALE2 are true, address lines 0 through 19 are available to you.**

**It is possible to access address lines above A15, but only if at least 1 chip select line isn’t used.**

**ii. Describe what performing full address decoding and partial address decoding signifies. Provide examples of both types for [1] an SRAM chip and [2] either an input port or output port.**

**An address consists of two parts:  
 1.Actual memory address  
 2.Chip select lines  
 Full address decoding means you use all of the chip select lines.  
 Partial address decoding means you use a portion of the chip select lines  
   
 SRAM example:  
 You have a 10 bit address that you use to load/store data in a 1k byte SRAM. The SRAM is split into four smaller SRAM’s that are 250 bytes each.  
 With full address decoding, you would allocate the first 2 bits to select the SRAM chip, then you would use the rest of the bits to select the specific byte in the SRAM chip.  
 With partial address decoding, where you aren’t allowed to access the lower two chips, you would ignore the 9th bit, and use the 8th bit to address the SRAM chip. You would then use the rest of the bits to address the specific byte.  
   
 GPIO example:**

**iii. In theory, how many 8-bit I/O ports could be mapped to the external data memory space of an ATxmega128A1U microcontroller, assuming that at most one port utilizes any particular address range? Explain your answer, utilizing your response from Exercise ii.**

**16 million I/O ports could be mapped.**

**The EBI can support up to 16MB of SRAM.  
The address size for the EBI can go up to 24 bits.  
However, the first 16k addresses are reserved for internal SRAM  
that’s 0xFFFFFF – 0x004000 = 0xFFBFFF(16,760,831) possible ports**

**iv. Assume that an SRAM component with the same size as the one on the OOTB Memory Base has to be added to a different computing system containing an ATxmega128A1U but no OOTB Memory Base (i.e., this is not the OOTB µPAD computing system), with the first address of the SRAM starting at address 0x42 4000, instead of the address specified in the “Lab 4 – Hardware Expansion” quiz. Design, on paper, a hardware expansion for this new system, utilizing the same structure of steps laid out in this quiz. Use the same “overall” memory-mapping constraints presented within the quiz.** A picture containing text, sketch, handwriting, drawing

Description automatically generated **Figure 1: EBI expansion with address starting at 0x424000.  
The SRAM needs to be split because the 32k SRAM is bigger than the boundary.**

**v. Assume that some external 128 KB SRAM must be fully mapped to the data memory space of the ATxmega128A1U, with the first memory location of the SRAM corresponding to data memory address 0x7A 0000. Design, on paper, a hardware expansion for this new system, utilizing the same structure of steps laid out in the relevant pre-lab quiz. Use the same “overall” memory-mapping constraints presented within this quiz. Hint: Consider how many address signals are needed to make the SRAM fully addressable, and then consider how you will gain access to all these signals.**

A picture containing text, handwriting, sketch, diagram

Description automatically generated **Figure 2: EBI expansion with address starting at 0x7A0000.  
This version requires 17 address bits, so an extra latch is needed**

**vi. Assume that some 8-bit input port should be accessible via the 256 consecutive addresses starting at 0x23 A000 within the ATxmega128A1U data memory space. Design, on paper, a hardware expansion for this port, utilizing the same structure of steps laid out in the relevant pre-lab quiz. Use the same “overall” memory-mapping constraints presented within this quiz.**A picture containing text, handwriting, sketch, diagram

Description automatically generated **Figure 3: EBI expansion starting at address 0x23A000.**

**vii. Assume that some external 1 MB SRAM must be fully mapped to the data memory space of the ATxmega128A1U, with the first memory location of the SRAM corresponding to data memory address 0x60 0000. Design, on paper, a hardware expansion for this new system, utilizing the same structure of steps laid out in the relevant pre-lab quiz. Use the same “overall” memory-mapping constraints presented within this quiz, except that which is concerning the usage of the SRAM 3-PORT ALE1 EBI configuration. Hint: you might consider the use of some other EBI configuration.**

A picture containing text, sketch, diagram, plan

Description automatically generated **Figure 4: 1 MB SRAM expansion. This configuration uses 4 port no ALE. Allowing ALE1 and ALE2 to be used as address lines 16 and 17, and CS0 and CS1 to be used as address 18 and address 19.**

**viii. How would one go about utilizing the SRAM 4PORT NOALE mode? (Note: Looking at the Alternate Pin Functions only ports H, J, and K by default can be used with the EBI system. How can the other port be activated)?**

**(Tell him what values get loaded into what registers)**

**PSEUDOCODE/FLOWCHARTS**

**SECTION 2**

A picture containing text, screenshot, diagram, parallel

Description automatically generated **Figure 5: Flowchart for “lab4\_2.asm”**

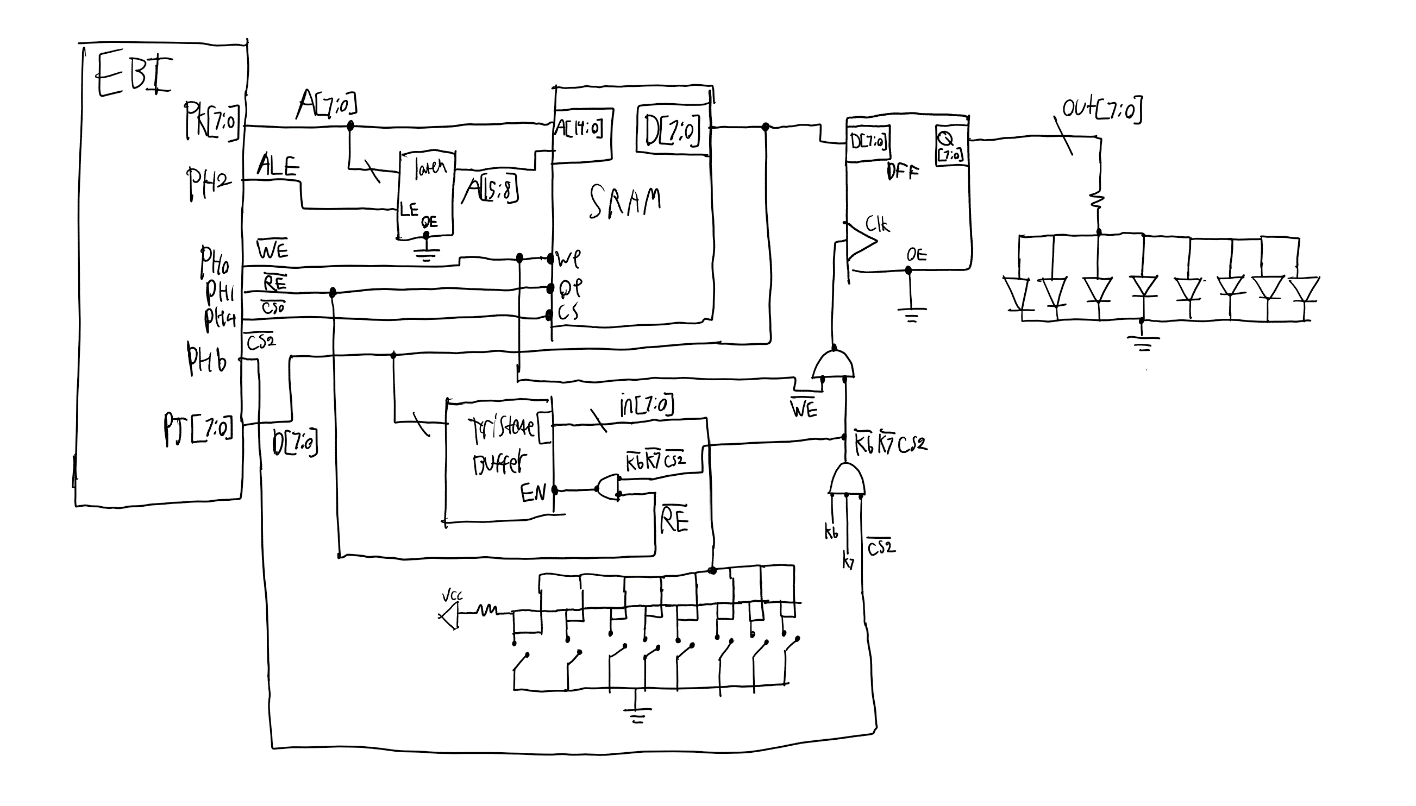
**PROGRAM CODE**

**SECTION X (1, 2, etc.)**

<insert copy of all required *main* program code, clearly distinguishing between each part of the lab (write “N/A” if there are none)>

THE ABOVE SHOULD BE FOLLOWED BY A PAGE BREAK (ALREADY INCLUDED), AND THIS SENTENCE OF TEXT SHOULD BE REMOVED.

**APPENDIX**

**  
Figure 1: SRAM EBI Extension Schematic.**