**REQUIREMENTS NOT MET**

N/A

**PROBLEMS ENCOUNTERED**

N/A

**FUTURE WORK/APPLICATIONS**

<insert a brief paragraph describing how the topics covered in this lab could potentially be used for other applications>

THE ABOVE SHOULD BE LIMITED TO THE FIRST PAGE, AND NOTHING ELSE SHOULD BE INCLUDED, WHICH ALSO IMPLIES THAT THIS SENTENCE OF TEXT SHOULD BE REMOVED.

**PRE-LAB EXERCISES**

**i. In regard to SPI communication that is to exist between the relevant ATxmega128A1U and IMU chips, answer each of the questions within the previously given bulleted list**

**Which device(s) should be given the role of master and which device(s) should be given the role of student?**

**The IMU should be the slave, and the ATX should be the master**

**How will the student device(s) be enabled? If a student select is utilized, rather than just have the device(s) be permanently enabled, which pin(s) will be used?**

**The slave will be enabled using its chip select.  
 The chip select of the slave (pin 12) will be connected to the slave select of the ATX(port F pin 5).**

**What is the order of data transmission? Is the MSb or LSb transmitted first?**

**The IMU transmits data MSB first.  
 The ATX can transmit data either LSB or MSB first**

**In regard to the relevant clock signal, should data be latched on a rising edge or on a falling edge?**

**The IMU transmits and receives data on a rising clock edge. So the data should be latched then.**

**What is the maximum serial clock frequency that can be utilized by the relevant devices?**

**The ATX can transmit/receive data at a max rate of 1MHZ.  
 However, the IMU can transmit at a max rate of 10MHZ  
 Therefore, the ATX will need to receive at its max frequency of 1MHZ**

**PSEUDOCODE/FLOWCHARTS**

**SECTION X (1, 2, etc.)**

<insert easily readable pseudocode/flowcharts, when applicable, clearly distinguishing between each part of the lab (write “N/A” if there are none)>

THE ABOVE SHOULD BE FOLLOWED BY A PAGE BREAK (ALREADY INCLUDED), AND THIS SENTENCE OF TEXT SHOULD BE REMOVED.

**PROGRAM CODE**

**SECTION X (1, 2, etc.)**

<insert copy of all required *main* program code, clearly distinguishing between each part of the lab (write “N/A” if there are none)>

THE ABOVE SHOULD BE FOLLOWED BY A PAGE BREAK (ALREADY INCLUDED), AND THIS SENTENCE OF TEXT SHOULD BE REMOVED.

**APPENDIX**

<insert copy of all *supporting* ASM or C program code, e.g., header files referenced within your programs, as well as any other relevant information, e.g., screenshots (with meaningful captions), when applicable (if not applicable, write “N/A”)>