$$y(k) = \sum_{n=0}^{N-1} a(n)x(k-n) \qquad k = 0, 1, \ldots$$

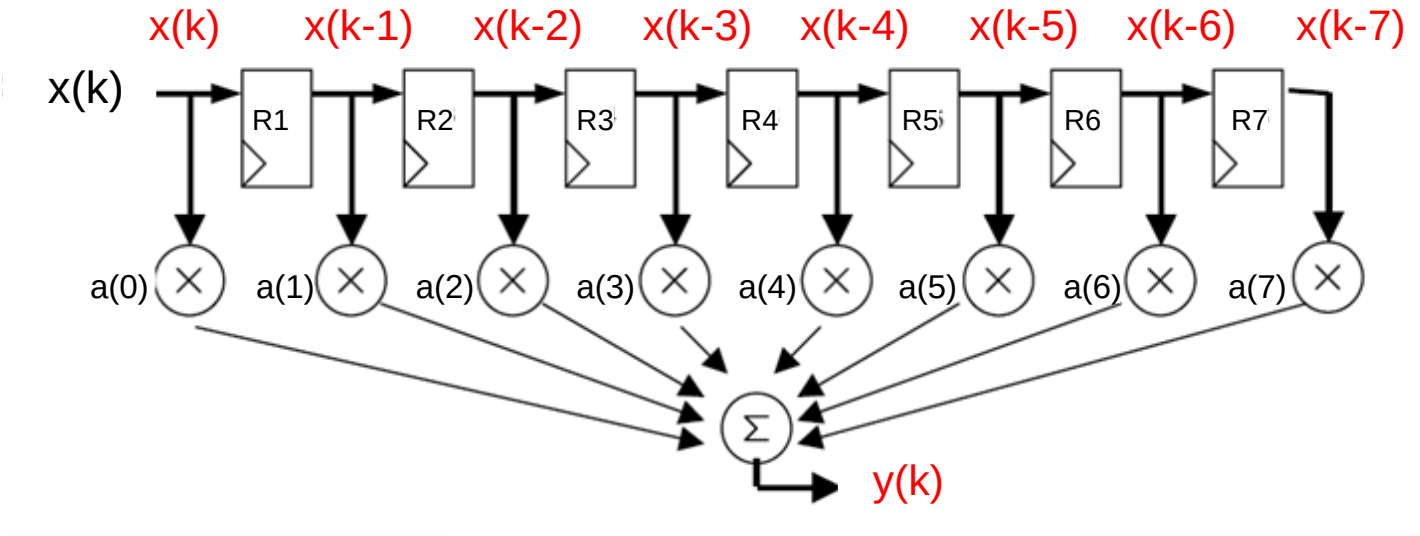
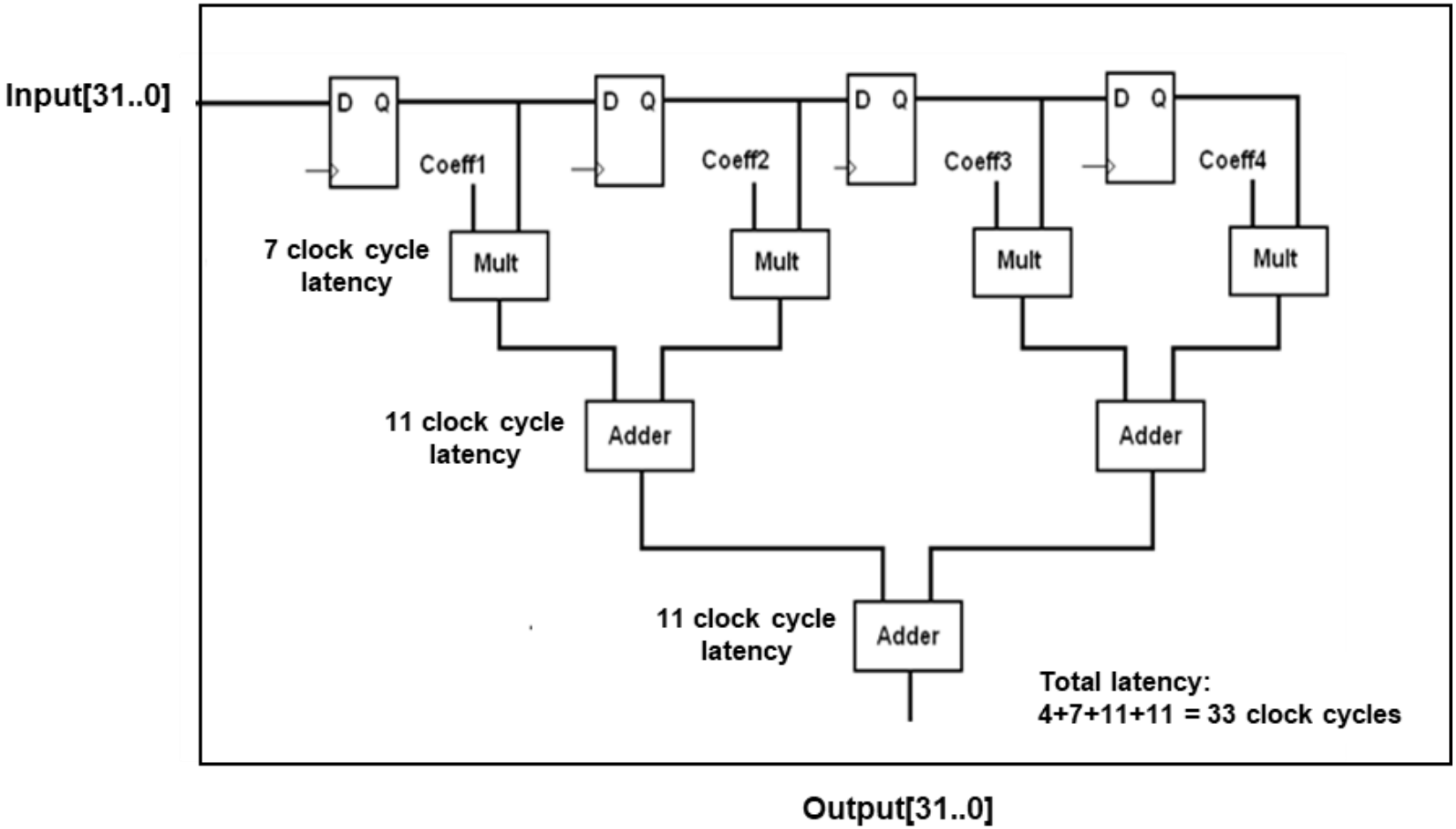


Figure 1. An 8-tap FIR filter

N = 8

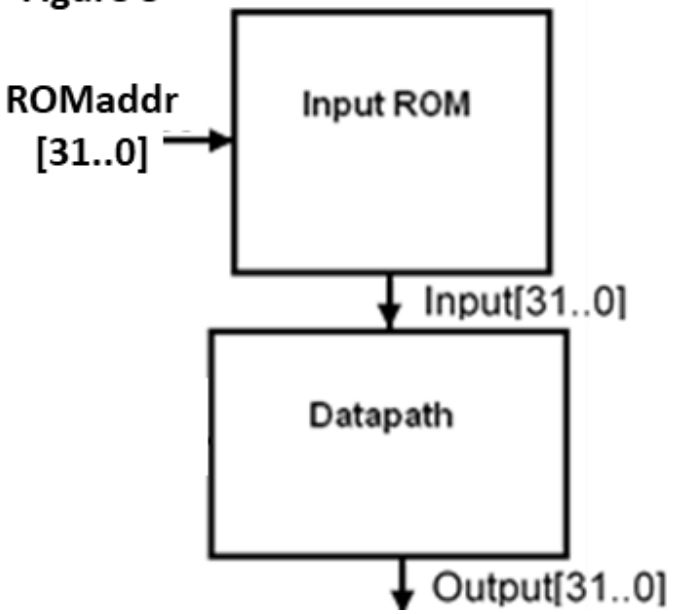
Part 1 **Datapath** Figure 2. Block diagram of a 4-tap FIR filter with pipelining



Generate a **32-bit floating-point multiplier** in the Quatus IP Catalog: Library -> Basic Functions -> Arithmetic -> FP_FUNCTIONS Intel FPGA IP.

Generate the **32-bit floating-point adder** in the Quatus IP Catalog: Library -> Basic Functions -> Arithmetic -> FP_FUNCTIONS Intel FPGA IP.

Figure 3



Part 1

Create the top-level entity (Figure 3) – Use the **ROM: 1-PORT** function in the Quatus IP Catalog: Library -> Basic Functions -> On Chip Memory -> ROM: 1-PORT to create the Input ROM

For this lab, the following filter coefficients for a 8-tap filter (in decimal) are used:

[0.068556404040904, 0.111805808555109, 0.149037722285938, 0.170581276322676, 0.170581276322676, 0.149037722285938, 0.111805808555109, 0.068556404040904]

- You need to convert them into the IEEE single-precision floating point (32 bit) format (e.g., use converter at: http://babbage.cs.qc.cuny.edu/IEEE-754/)

sign bit [31] exponent [30..23] fractional [22..0]

IEEE 754 FP Format

To convert: http://babbage.cs.qc.cuny.edu/IEEE-754

Single Precision (32 bits)

31	30 - 23	22 - 0

- **Bit 31: sign bit** (0 positive; 1 negative)
- **Bits 30 – 23: exponent** (with a bias of 127 decimal)
- **Bits 22 – 0: mantissa** (with an implied '1')

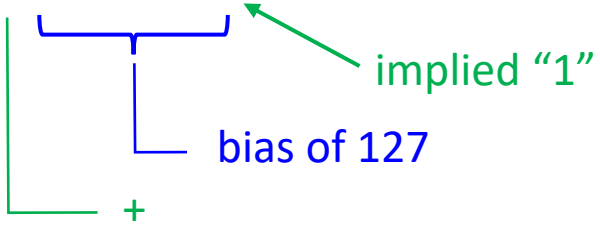
Example 1: +5.0

+5.0 = +101.000 in binary

= +1.01 X 2^2

In IEEE FP single-precision format

0 10000001 010 0000 0000 0000 0000 0000



Example 2: -5.0 1 10000001 010 0000 0000 0000 0000 0000

Example 3: +2.75 0 10000000 011 0000 0000 0000 0000 0000

Example 4: -115.875 1 10000101 110 0111 1100 0000 0000 0000

Part 2

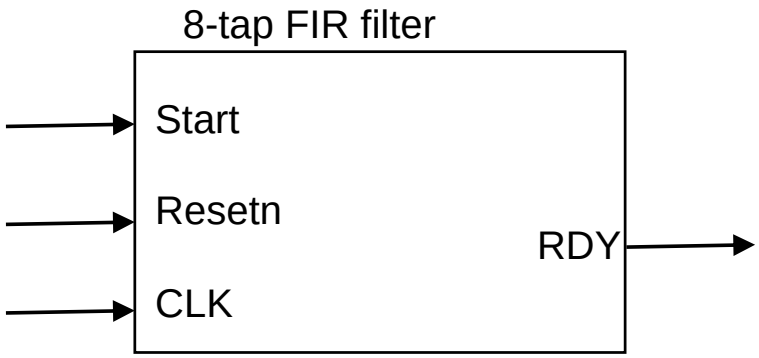


Figure 4. Complete FIR filter

Resetn: Active low reset signal that initializes the FIR filter to the initial state.

Start (active high): The FIR filter wait for this signal to be true before it begins its operation.

CLK: Clock input for the FIR filter.

RDY: Ready (active high), indicates that the FIR filter is finished and is ready for a new operation.

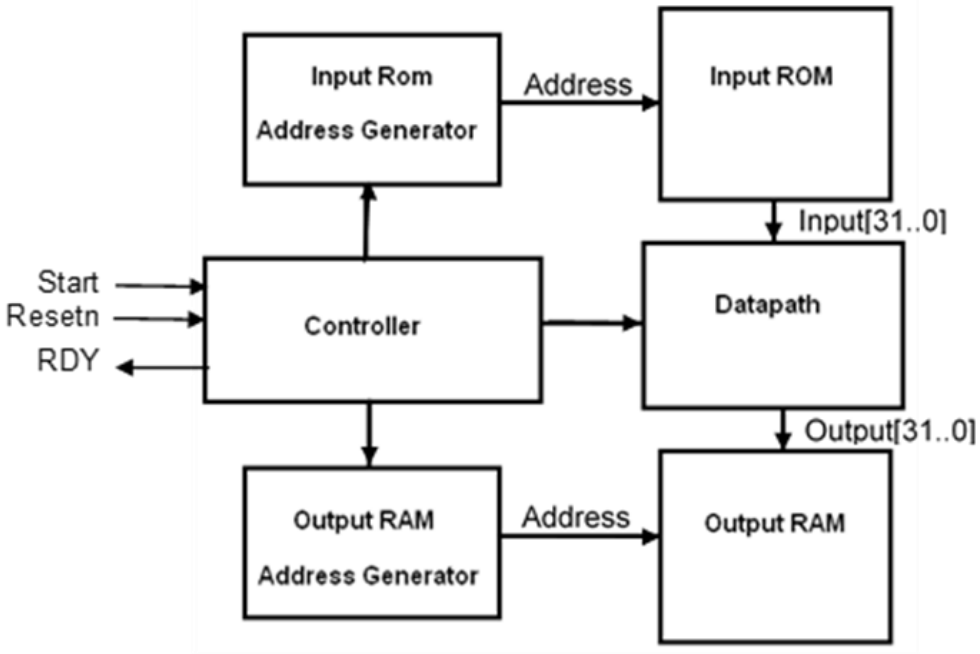


Figure 5. Block diagram design of FIR filter