

/p3/modelsim/clkdiv/lab4_p3_clkdiv

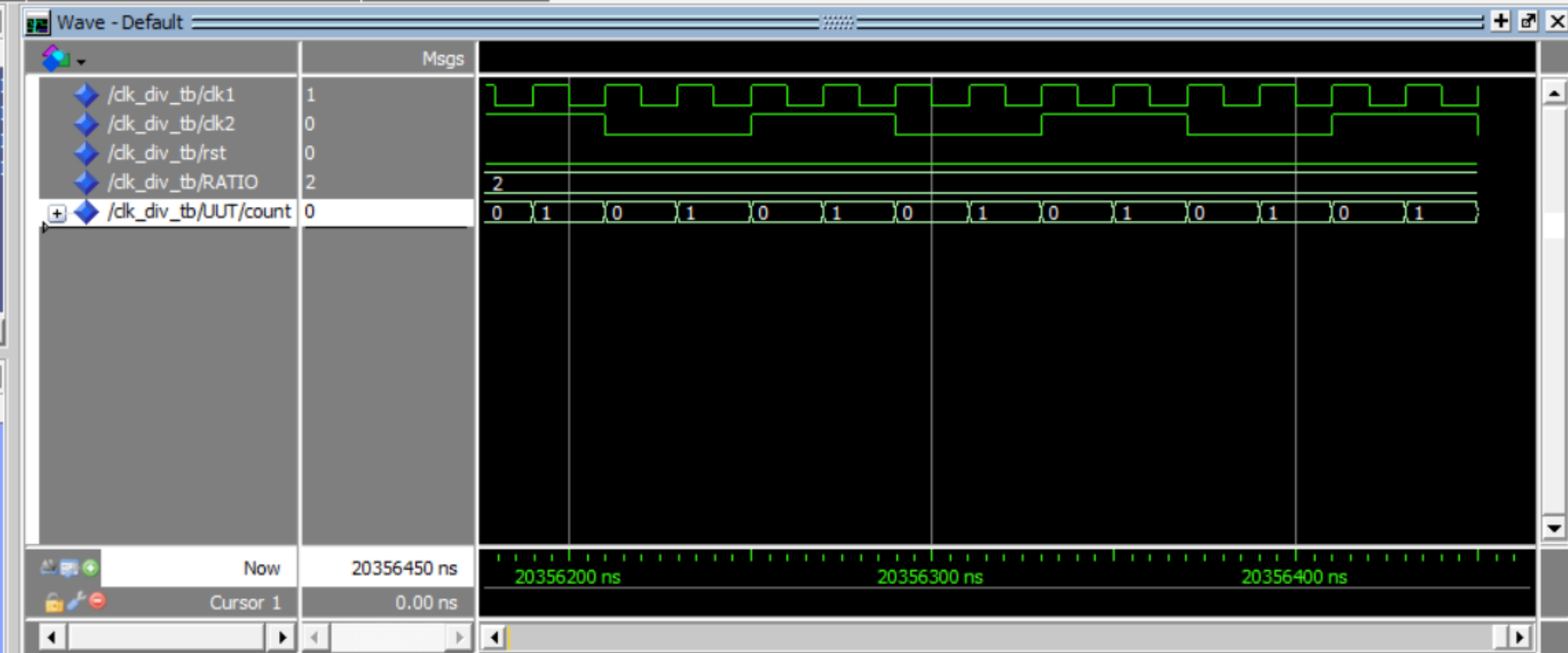
Name	Status
clk_div_tb.vhd	✓
clk_div.vhd	✓

Objects

Name	Value	Type
clk1	1	Signal
clk2	0	Signal
rst	0	Signal
RATIO	2	Con...

Processes (Active)

Name	Type (filtered)



Library Project sim

Transcript

```
#
# Compile of clk_div.vhd was successful.
# Compile of clk_div_tb.vhd was successful.
# 2 compiles, 0 failed with no errors.
VSIM 55> restart -f
# ** Note: (vsim-12125) Error and warning message counts have been reset to '0' because of 'restart'.
# Loading work.clk_div_tb(tb)
# Loading work.clk_div/arch)
VSIM 56> run -all
# GetModuleFileName: The specified module could not be found.
#
#
VSIM 57>
```

20356176755 ps to 2035646438: Project : lab4_p3_clkdiv Now: 20,356,450 ns Delta: 3 sim:/clk_div_tb

