3-8 Line Decoder

Project Summary | Schematic | Desing.v

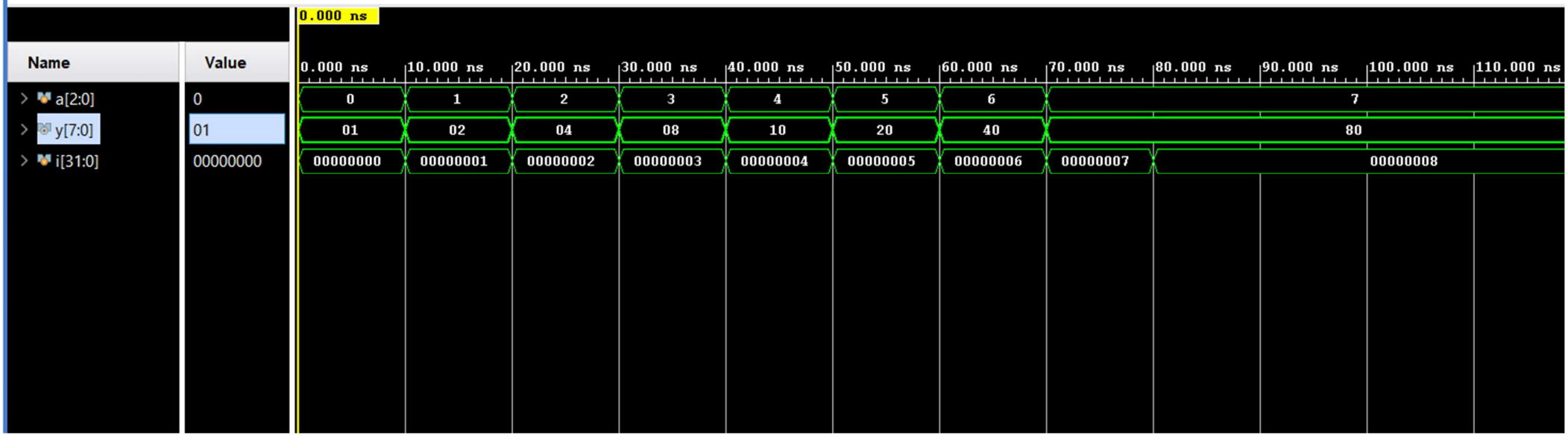
D:/Vivado/2_1_Mux/2_1_Mux.srcs/sources_1/new/Desing.v

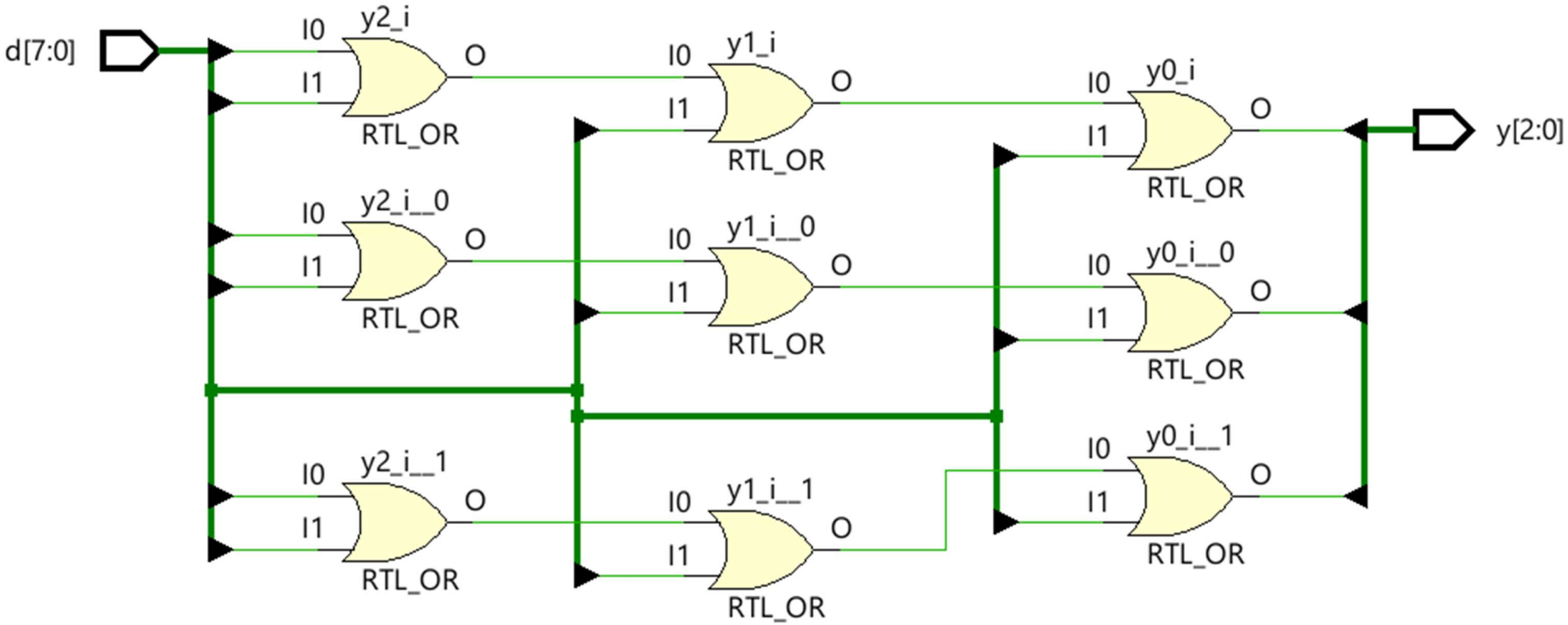
```
1  //3 to 8 line decoder design code
2  module decoder(a,y);
3    input [2:0]a;
4    output reg[7:0]y;
5    always@(*)
6      begin
7        case(a)
8          3'b000: y=8'b00000001;
9          3'b001: y=8'b00000010;
10         3'b010: y=8'b00000100;
11         3'b011: y=8'b00001000;
12         3'b100: y=8'b00010000;
13         3'b101: y=8'b00100000;
14         3'b110: y=8'b01000000;
15         3'b111: y=8'b10000000;
16        default: y=8'bxxxxxxxx;
17       endcase
18     end
19 endmodule
20
```

...ux.srcs/sim_1/new/testbench.v

```
1  // 3 to 8 line decoder test bench
2  module tb;
3    reg[2:0]a;
4    wire[7:0]y;
5    integer i;
6    decoder u1(.y(y),.a(a));
7    initial
8      begin
9        $monitor("a=%d,y=%b",a,y);
10       for (i=0;i<8;i=i+1)
11         begin
12           a=i;
13           #10;
14         end
15     end
16 endmodule
17
18
```

Desing.v | testbench.v | Untitled 1





OUTPUT

```
# KERNEL: a=0,y=00000001
# KERNEL: a=1,y=00000010
# KERNEL: a=2,y=00000100
# KERNEL: a=3,y=00001000
# KERNEL: a=4,y=00010000
# KERNEL: a=5,y=00100000
# KERNEL: a=6,y=01000000
# KERNEL: a=7,y=10000000
# KERNEL: Simulation has finished.
```

A **3-to-8 line decoder** is a combinational circuit that takes three binary input signals and decodes them into eight unique output signals. It is commonly used in digital electronics for tasks like memory addressing, signal demultiplexing, and control signal generation.

Functionality

- **Inputs:** The decoder has three input lines, typically labeled A2*A*2, A1*A*1, and A0*A*0, representing a 3-bit binary number.
- **Outputs:** There are eight output lines (Y0*Y*0 to Y7*Y*7), with only one output active at a time based on the binary combination of the inputs.
- **Enable Pins:** The decoder includes enable pins to activate or deactivate its functionality. When the enable pin is inactive, all outputs remain deactivated.

Truth Table

The truth table for a 3-to-8 decoder is as follows:

Inputs (*A*2,*A*1,*A*0)	Active Output
000	Y0
001	Y1
010	Y2
011	Y3
100	Y4
101	Y5
110	Y6
111	Y7

Implementation

A 3-to-8 decoder can be implemented using basic logic gates or by combining two lower-order decoders (e.g., two 2-to-4 decoders). For example:

- The three input lines (A2,A1,A0*A*2,*A*1,*A*0) are decoded into eight outputs (Y0*Y*0 to Y7*Y*7).
- Enable pins control whether the outputs correspond to lower or higher minterms.

Applications

1. **Binary-to-Octal Conversion:** Converts binary inputs into octal outputs for applications requiring octal representation.
2. **Memory Address Decoding:** Used to select specific memory locations in computer systems.
3. **Signal Demultiplexing:** Routes signals to specific channels based on the binary input.
4. **Control Systems:** Enables control of multiple devices or sensors in systems like security setups or keypad interfaces.

Popular IC Example

The **74LS138** and **SN74LVC138A** are common ICs used for implementing 3-to-8 decoders. These ICs feature:

- Three input pins
- Eight output pins
- Enable pins for activation
- High-speed operation suitable for memory decoding and signal routing[135].