8-1 Mux

Schematic | Project Summary | Design.v

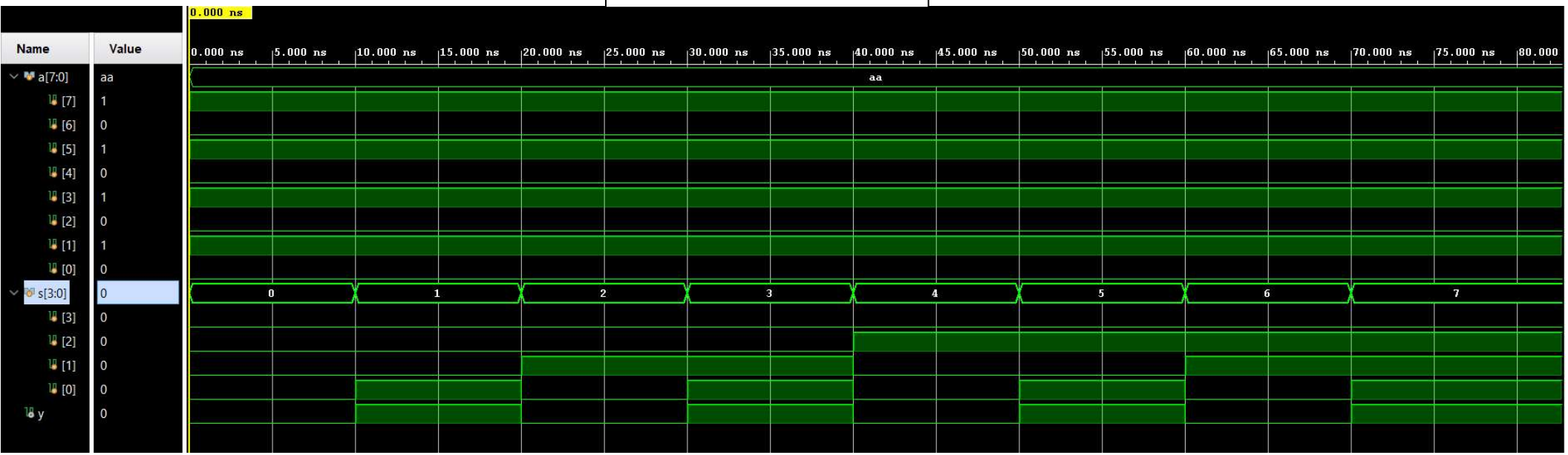
D:/Vivado/Mux 8-1/Mux 8-1.srcs/sources_1/new/Design.v

```
1  //Design 8-1 Mux
2  module mux(input [7:0]a,input [3:0]s,output reg y);
3    always@(s or a) begin
4      case(s)
5        3'b000: y=a[0];
6        3'b001: y=a[1];
7        3'b010: y=a[2];
8        3'b011: y=a[3];
9        3'b100: y=a[4];
10       3'b101: y=a[5];
11       3'b110: y=a[6];
12       3'b111: y=a[7];
13       default: y=1'bx;
14     endcase
15   end
16 endmodule
```

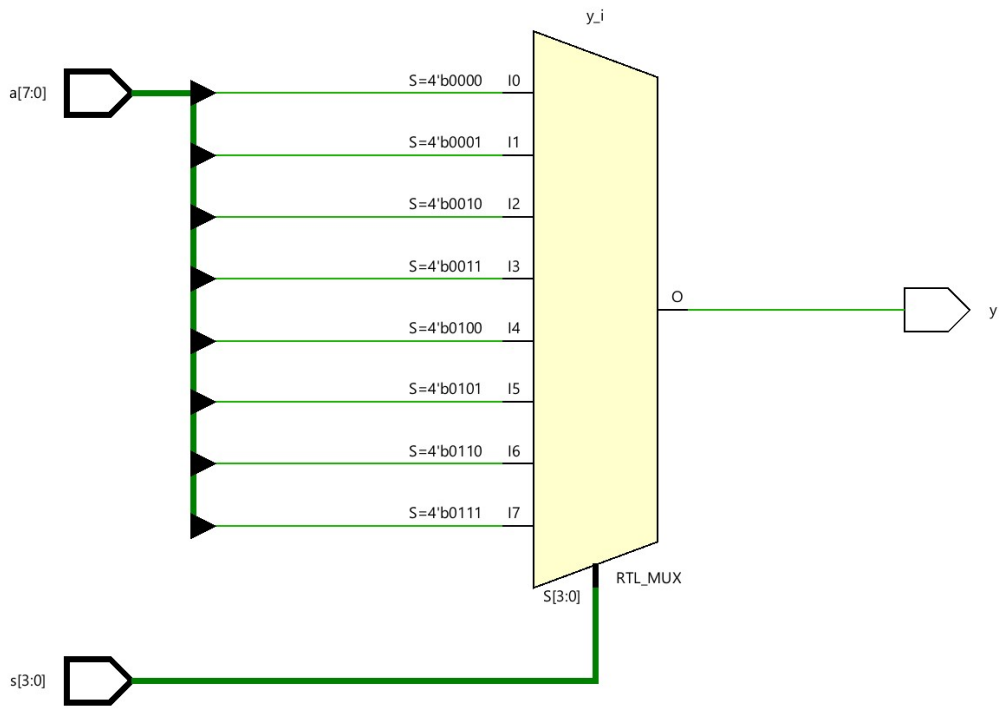
Mux 8-1/Mux 8-1.srcs/sim_1/new/Testbench.v

```
1  //Testbench 8-1 Mux
2  module tb_mux;
3  reg [7:0]a;
4  reg [3:0]s;
5  wire y;
6  mux u1(.y(y),.s(s),.a(a));
7  initial begin
8    $monitor("s=%0b,y=%0b",s,y);
9    a=8'b10101010;
10   s=3'b000;#10;
11   s=3'b001;#10;
12   s=3'b010;#10;
13   s=3'b011;#10;
14   s=3'b100;#10;
15   s=3'b101;#10;
16   s=3'b110;#10;
17   s=3'b111;#10;
18 end
19 endmodule
```

Timing Digram



Digram



OUTPUT

```
# KERNEL: s=0,y=0
# KERNEL: s=1,y=1
# KERNEL: s=10,y=0
# KERNEL: s=11,y=1
# KERNEL: s=100,y=0
# KERNEL: s=101,y=1
# KERNEL: s=110,y=0
# KERNEL: s=111,y=1
```

An **8-to-1 multiplexer (8:1 MUX)** is a digital combinational circuit that allows one of eight input data lines to be routed to a single output line. It functions as a data selector, where only one input is connected to the output at any given time, depending on the values of the selection inputs. The multiplexer has **eight data inputs** (D0 to D7), **three select lines** (S2, S1, S0), and **one output** (Y). The select lines are used to choose which one of the eight inputs is passed through to the output. Since there are three selection lines, they can represent $2^3 = 8$ different combinations, allowing selection of all eight inputs.

Multiplexers are essential in digital electronics and computer systems for efficiently handling multiple data lines and minimizing wiring complexity. They are commonly used in communication systems, data routing, arithmetic logic units, and more.

The operation of an 8:1 multiplexer is described by the following truth table:

S2	S1	S0	Output Y
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

In this table, the binary value formed by the select lines (S2 S1 S0) determines which data input (D0 to D7) is connected to the output Y. For instance, if the select lines are 101, the fifth data input (D5) is routed to the output. The 8:1 multiplexer is often built using basic logic gates or can be implemented using higher-level hardware description languages for use in programmable devices like FPGAs.