Half Adder

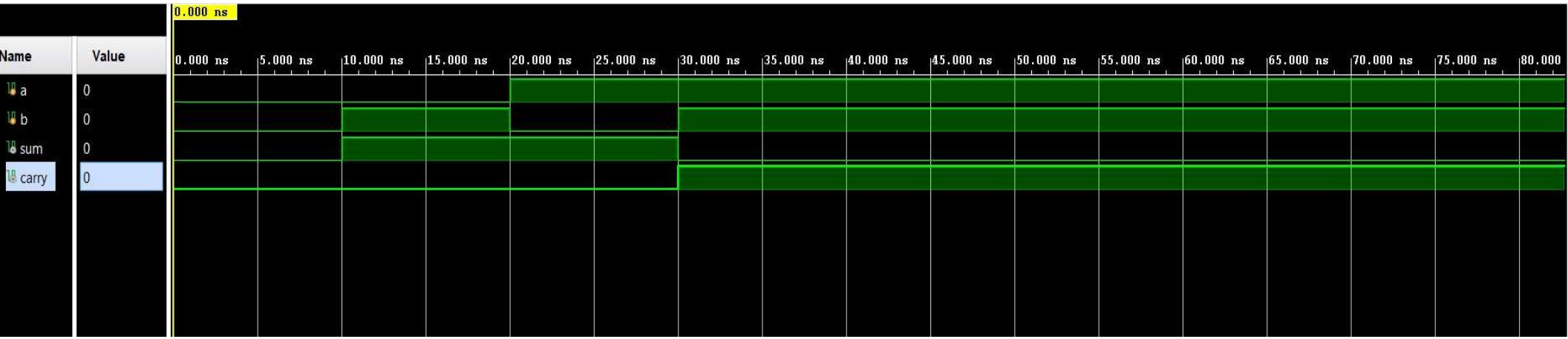
ado/Half Adder/Half Adder.srcs/sources_1/new/Design.v

```
// Code your design here
module ha(
  input a,b,
  output sum,carry
);
  assign sum = (a^b);
  assign carry = (a*b);
endmodule
```

D:/Vivado/Half Adder/Half Adder.srcs/sim_1/new/Testbench.v

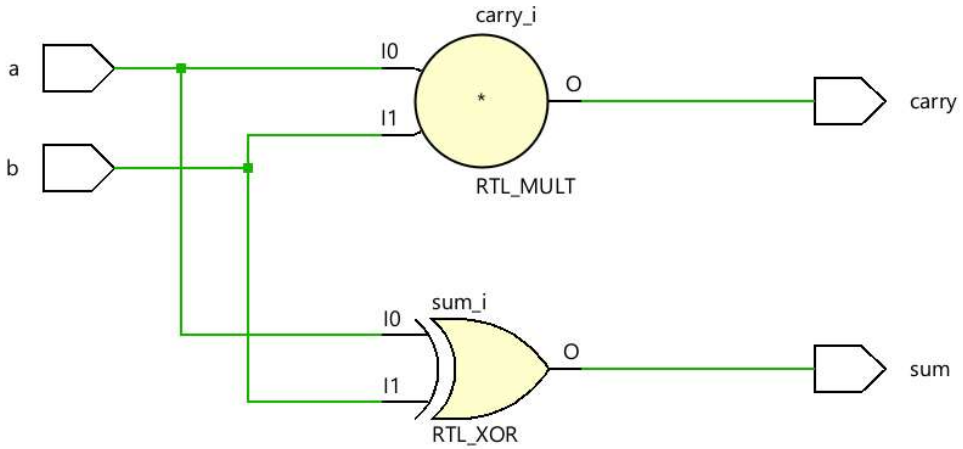
```
1  // Code your testbench here
2  // or browse Examples
3  module ha_tb;
4    reg a,b;
5    wire sum,carry;
6    ha u1(.a(a),.b(b),.sum(sum),.carry(carry));
7    initial begin
8      $monitor("a=%b,b=%b,   ,sum=%b,carry=%b",a,b,sum,carry);
9      a=1'b0;b=1'b0;#10;
10     a=1'b0;b=1'b1;#10;
11     a=1'b1;b=1'b0;#10;
12     a=1'b1;b=1'b1;#10;
13   end
14 endmodule
15
16
```

Timing Digram



Digram

e



OUTPUT

```
# KERNEL: a=0,b=0,   ,sum=0,carry=0
# KERNEL: a=0,b=1,   ,sum=1,carry=0
# KERNEL: a=1,b=0,   ,sum=1,carry=0
# KERNEL: a=1,b=1,   ,sum=0,carry=1
```

A **Half Adder** is a basic combinational logic circuit designed to add two single-bit binary numbers. It produces two outputs: the **sum** and the **carry**.

Inputs and Outputs

- **Inputs:** Two single-bit binary digits, usually labeled A and B.
- **Outputs:**
  - **Sum (S):** The least significant bit of the addition result.

- **Carry (C):** The carry-out bit, which is generated when both inputs are 1.

How It Works

The half adder adds the two input bits according to binary addition rules:

- 0 + 0 = Sum 0, Carry 0
- 0 + 1 = Sum 1, Carry 0
- 1 + 0 = Sum 1, Carry 0
- 1 + 1 = Sum 0, Carry 1 (since 1 + 1 = 10 in binary)

Logic Gates Used

- The **Sum (S)** output is obtained using an **XOR gate** because the sum is 1 only when the inputs differ.
- The **Carry (C)** output is obtained using an **AND gate** because carry is 1 only when both inputs are 1.

Truth Table

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0

A	B	Sum (S)	Carry (C)
1	1	0	1

Boolean Expressions

- Sum: $S=A \oplus B$
- Carry: $C=A \cdot B$

Circuit Diagram

The half adder circuit consists of one XOR gate for the sum and one AND gate for the carry, connected to the two inputs A and B.

Limitations

- The half adder cannot handle a carry input from a previous addition, so it cannot be used alone for multi-bit binary addition.
- For multi-bit addition, **full adders** (which include carry-in inputs) are used, often constructed by combining two half adders and an OR gate.

Applications

- Used as a fundamental building block in digital circuits.
- Forms the basis for constructing full adders.
- Used in arithmetic logic units (ALUs), binary counters, and other digital arithmetic circuits.

In summary, the half adder is a simple yet essential digital circuit that adds two single-bit binary numbers and provides the sum and carry outputs using XOR and AND gates respectively