



1. Description

1.1. Project

Project Name	MicroMouse_main2
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	08/01/2022

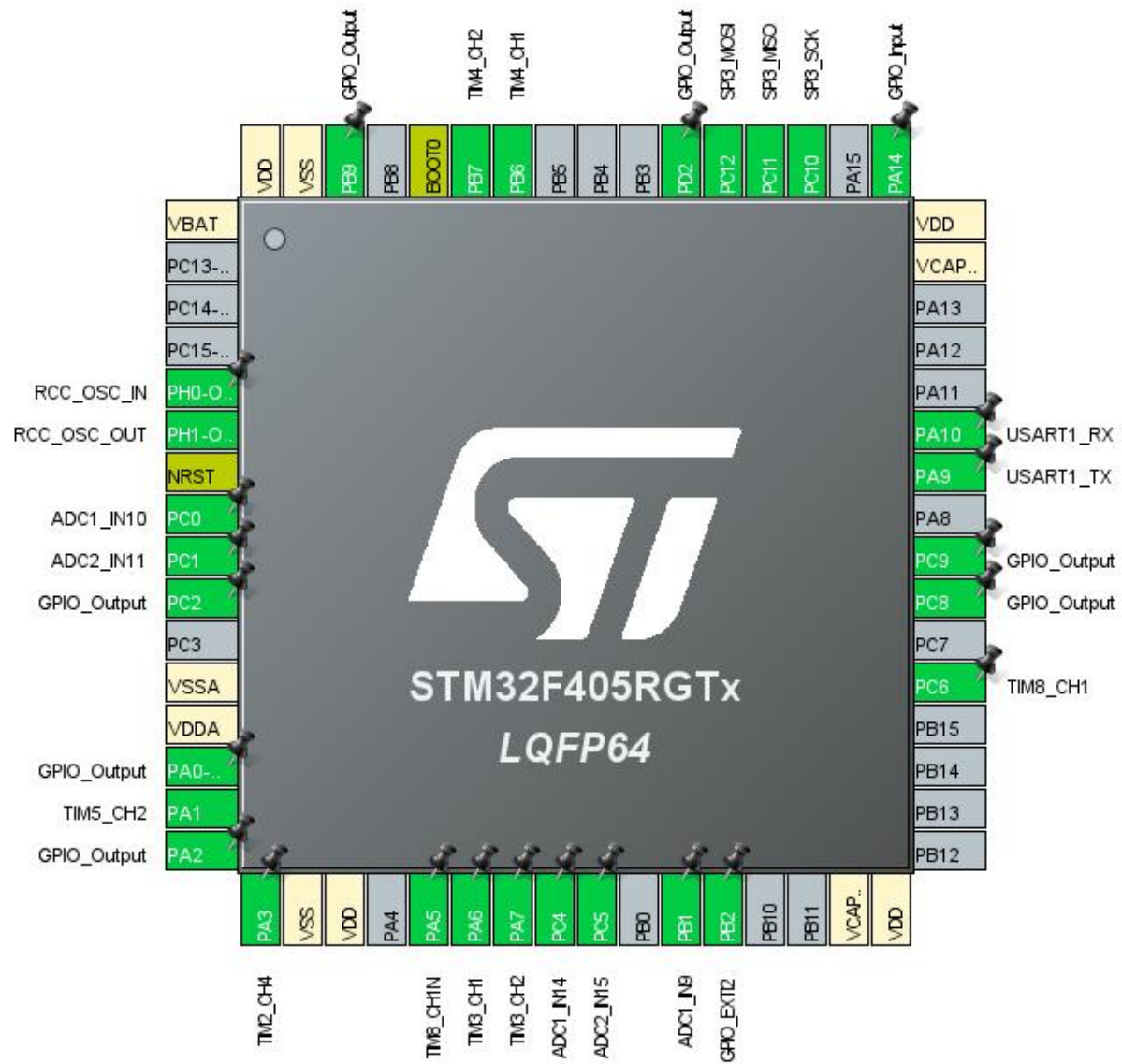
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



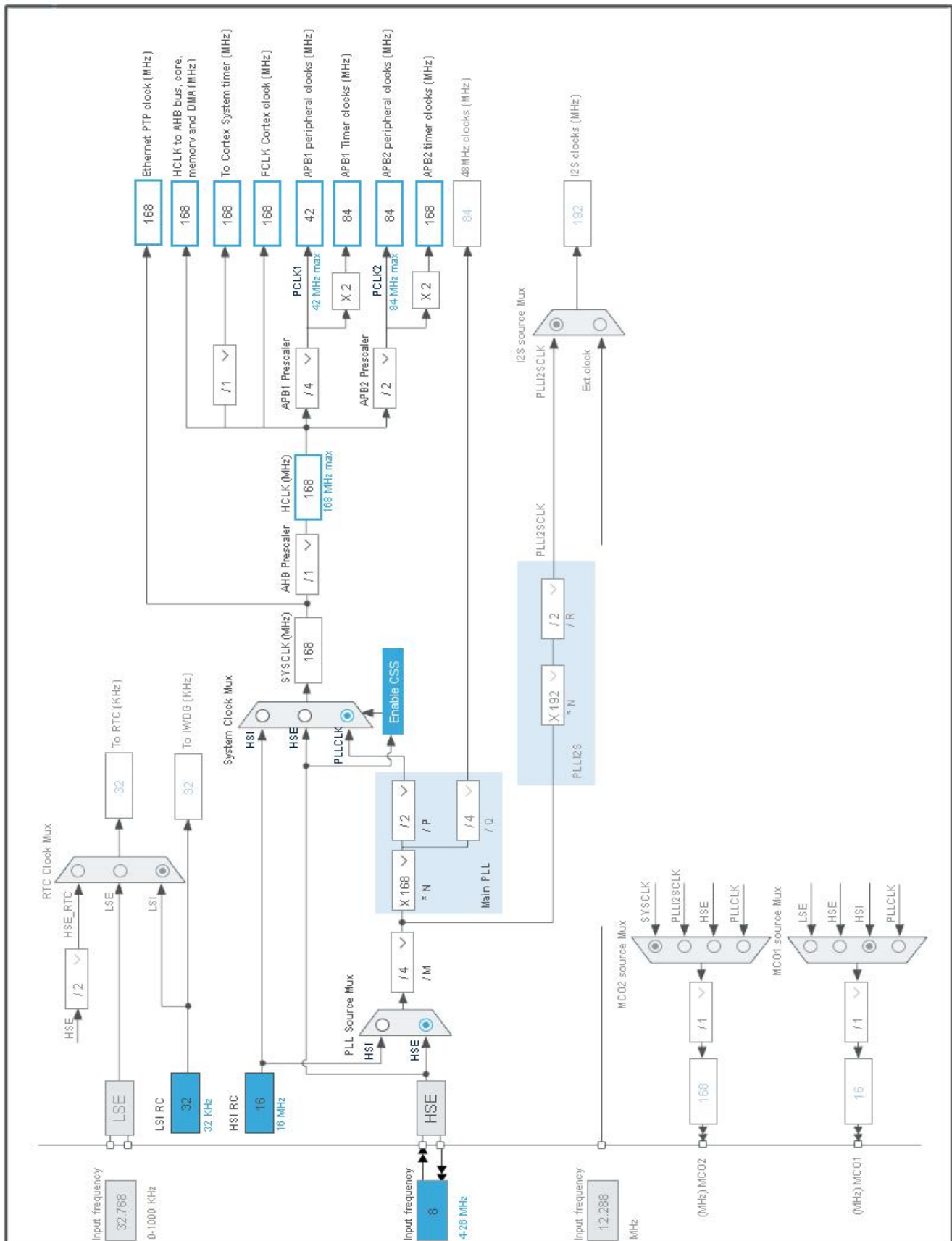
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	
9	PC1	I/O	ADC2_IN11	
10	PC2 *	I/O	GPIO_Output	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP *	I/O	GPIO_Output	
15	PA1	I/O	TIM5_CH2	
16	PA2 *	I/O	GPIO_Output	
17	PA3	I/O	TIM2_CH4	
18	VSS	Power		
19	VDD	Power		
21	PA5	I/O	TIM8_CH1N	
22	PA6	I/O	TIM3_CH1	
23	PA7	I/O	TIM3_CH2	
24	PC4	I/O	ADC1_IN14	
25	PC5	I/O	ADC2_IN15	
27	PB1	I/O	ADC1_IN9	
28	PB2	I/O	GPIO_EXTI2	
31	VCAP_1	Power		
32	VDD	Power		
37	PC6	I/O	TIM8_CH1	
39	PC8 *	I/O	GPIO_Output	
40	PC9 *	I/O	GPIO_Output	
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14 *	I/O	GPIO_Input	
51	PC10	I/O	SPI3_SCK	
52	PC11	I/O	SPI3_MISO	
53	PC12	I/O	SPI3_MOSI	
54	PD2 *	I/O	GPIO_Output	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
62	PB9 *	I/O	GPIO_Output	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MicroMouse_main2
Project Folder	C:\Users\leopi\mousestest\micromouse
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_TIM3_Init	TIM3
7	MX_TIM2_Init	TIM2
8	MX_SPI3_Init	SPI3
9	MX_USART1_UART_Init	USART1
10	MX_TIM5_Init	TIM5
11	MX_TIM4_Init	TIM4

Rank	Function Name	Peripheral Instance Name
12	MX_TIM8_Init	TIM8
13	MX_TIM1_Init	TIM1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

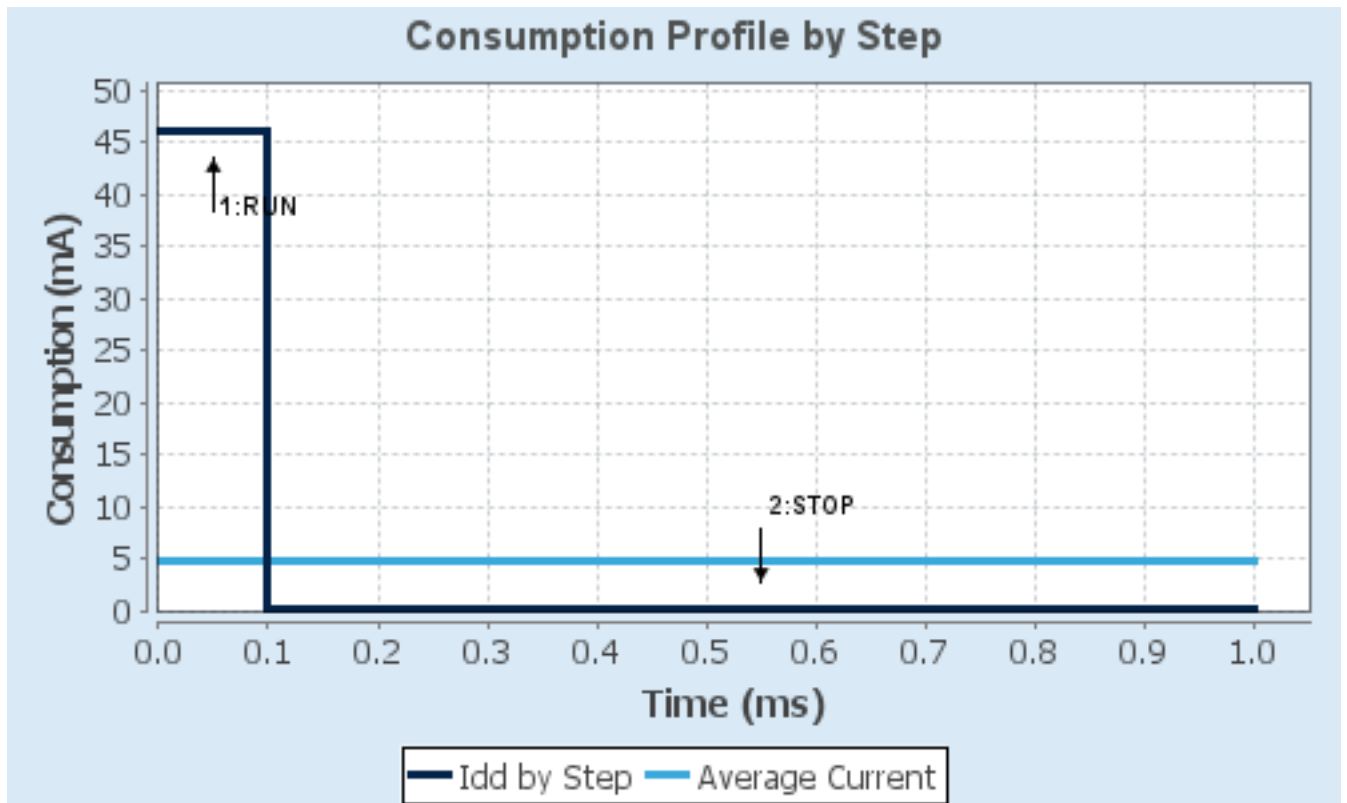
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μ A
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.02	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN9

mode: IN10

mode: IN14

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler **PCLK2 divided by 6 ***

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion **3 ***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel **Channel 10 ***

Sampling Time **56 Cycles ***

Rank **2 ***

Channel **Channel 14 ***

Sampling Time **56 Cycles ***

Rank **3 ***

Channel Channel 9

Sampling Time **56 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. ADC2

mode: IN11

mode: IN15

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler

PCLK2 divided by 6 *

Resolution

12 bits (15 ADC Clock cycles)

Data Alignment

Right alignment

Scan Conversion Mode

Enabled

Continuous Conversion Mode

Enabled *

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

Enabled *

End Of Conversion Selection

EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion

2 *

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 11

Sampling Time

56 Cycles *

Rank

2 *

Channel

Channel 15 *

Sampling Time

56 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions

0

WatchDog:

Enable Analog WatchDog Mode

false

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.4. SPI3

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	64 *
Baud Rate	656.25 KBits/s *
Clock Polarity (CPOL)	High *
Clock Phase (CPHA)	2 Edge *

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.5. SYS

Timebase Source: SysTick

7.6. TIM1

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	168-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.7. TIM2

Clock Source : Internal Clock

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4200-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM3

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	60000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode

Encoder Mode TI1 and TI2 *

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

____ Parameters for Channel 2 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.9. TIM4

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	60000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode

Encoder Mode TI1 and TI2 *

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

____ Parameters for Channel 2 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.10. TIM5

mode: Clock Source

Channel2: PWM Generation CH2

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4200-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.11. TIM8

Clock Source : Internal Clock

Channel1: Output Compare CH1 CH1N

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	168-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	50-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Output Compare Channel 1 and 1N:

Mode	Toggle on match *
Pulse (16 bits value)	25-1 *
Output compare preload	Enable *
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.12. USART1

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
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Over Sampling

16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC1	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
TIM2	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PA5	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
ADC2	DMA2_Stream2	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

ADC2: DMA2_Stream2 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line2 interrupt	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	1	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
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Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line2 interrupt	false	true	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	TIM1 ✓	SPI3 ✓			
GPIO ✓	ADC2 ✓	TIM2 ✓	USART1 ✓			
IVVIC ✓		TIM3 ✓				
RCC ✓		TIM4 ✓				
SYS ✓		TIM5 ✓				
		TIM8 ✓				

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note http://www.st.com/resource/en/application_note/DM00536349.pdf