Summary – Getting Started with Digital VLSI SoC Design and Planning

1. Specification in C Model

Before RTL coding, a C-based model (e.g., RISC-V with GCC) is developed.
Used to validate the specification and system functionality.

2. RTL Design

RTL code (typically in Verilog) is written to match the specification.
Verified using testbenches to ensure correctness.

3. SoC Design Flow

RTL is divided into:

- **Processor core** (synthesizable).
- **Peripheral IPs** (macros, analog IP like PLL, etc.).

IPs are synthesized into gates/flip-flops, while analog IPs are designed at the transistor level.

4. SoC Integration

Processor, peripherals, and macros are integrated.
Interconnected with GPIOs, buses, and on-chip interconnects.

5. Physical Design

Floorplanning → Placement → CTS (Clock Tree Synthesis) → Routing.
Final **GDSII** file is generated.

6. Sign-off & Fabrication

DRC/LVS checks performed on GDSII.
Clean design is sent for fabrication (**Tapeout/Tapein**).

BY : S S JHOTHEESHWAR