CM6206

High Integrated USB Audio I/O Controller

DESCRIPTION

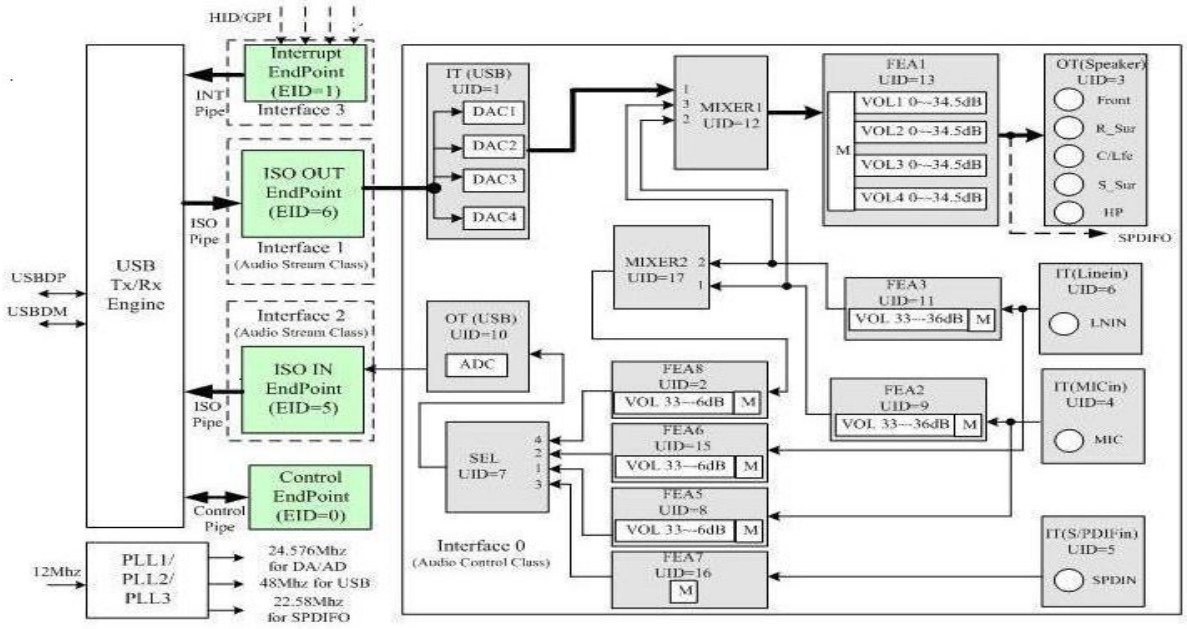
CM6206 is a highly integrated single chip USB audio solution. All essential analog modules are embedded in CM6206, including 8CH DAC and earphone buffer, 2CH ADC, microphone gain, PLL, regulator, and USB transceiver. It is very suitable for high end USB external audio box, USB multi-channel headphone or USB audio interface multi-channel speaker set application.

Many features are programmable with external EEPROM and MCU interface. In addition, MCU/EEPROM/GPIO control can easily via HID software interface. Better yet, CM6206 support stereo MIC, phone jack sense, S/PDIF I/O 48 KHz sampling rate. Moreover, unique patent driver can support world's first SPEAKER SHIFTER, Karaoke and Dolby AC-3 real-time encoder functions.

FEATURES

- USB spec. 2.0 full speed compliant
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- IEC60958 spec. compliant (consumer format S/PDIF input and output with loop-back support)
- SCMS (Serial Copy Management System) compliant
- Dolby® digital audio streaming via S/PDIF output interface
- USB remote wake-up support
- 8 channel DAC output with 16 bit resolution
- 3.1 Vpp (1.1 Vrms) biased at 2.25V output swing
- Volume control and mute function
- Earphone buffer
- Self power / Bus power selectable (by EEPROM)
- 2X interpolator for digital playback data to improve quality
- 2 channel ADC input with 16 bit resolution

BLOCK DIAGRAM



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1 Description and Overview

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- 3.1 Vpp (1.1 Vrms) biased at 2.25V output swing
- Volume control and mute function
- Earphone buffer
- 2X interpolator for digital playback data to improve quality
- 2 channel ADC input with 16 bit resolution
- 3.2 Vpp (or 4.0 Vpp programmed by vendor driver) biased at 2.25V input swing
- Volume control and mute function
- Additional headphone output with selectable source and phone jack sense
- Isochronous transfer using adaptive synchronization with internal PLL
- Stereo MIC support with 33dB maximum capability
- Recording source select from S/PDIF, MIC, Line-in and summation of MIC, Line-in and front channel
- MIC, Line-in monitor from front channel (all channels optional) with volume control and mute function
- Master volume control by default; per-channel volume control by C-Media driver
- Playback with soft-mute function
- Support 48 / 44.1 KHz sampling rate for both playback and recording
- MCU support with two-wire serial interface
- Serial EEPROM support for customized VID/PID

- MCU / EEPROM / GPIO control via HID software interface
- Volume up / volume down / playback mute HID button
- LED indicator pins: operation / recording mute / SCMS protection
- C-Media value added software (multi-channel positional 3D sound, AC-3 encoder, etc.)
- Embedded USB transceiver and power on reset circuit
- Microsoft Vista Premium Level Compliant
- Single 12MHz crystal input with embedded PLL
- Single 5V power supply with embedded 5V to 3.3V regulator
- Industry standard LQFP-48 package
- C-Media value added patent software driver:

  Xear 3D sound

  Earphone Plus

  SPEAKER SHIFTER

  Environment sound effects

  Room Size Mode

  Graphic Equalizer

  Karaoke Function

  Dolby Digital Real-Time Content Encoder (Optional)

3 Pin Descriptions

3.1 CM6206 LQFP 48Pin Table

PIN #	Signal Name	PIN #	Signal Name	PIN #	Signal Name
1	PDSW	17	DW	33	RSOL
2	XI	18	USBDP	34	RSOR
3	XO	19	USBDM	35	FROL
4	DVSS1	20	REGV	36	FROR
5	SDAT	21	DVDD1	37	AVDD2
6	SCLK	22	AVSS3	38	SSOL
7	TEST	23	MICL	39	SSOR
8	MCLK	24	MICR	40	CENO
9	MINT	25	LINL	41	LFEO
10	GPIO1	26	LINR	42	AVSS2
11	LEDO	27	AVDD1	43	VOLUP
12	LEDR	28	VREF	44	VOLDN
13	PHONES	29	VBIAS	45	SPDIFI
14	CS	30	AVSS1	46	MUTER
15	SK	31	HPOL	47	MUTEP
16	DR	32	HPOR	48	SPDIFO

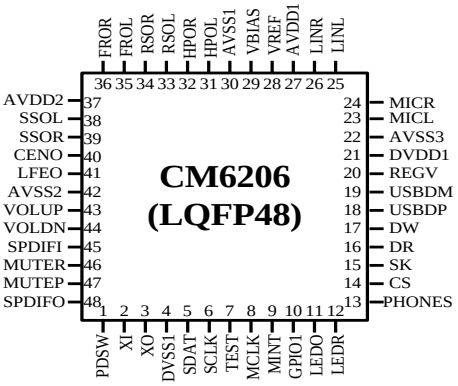


Figure 1. CM6206 LQFP 48 Pin Assignments (Top View)

3.2 CM6206 LQFP 48 PIN

Pin #	Symbol	Type	Description
1	PDSW	DO	Power down switch control (for PMOS polarity) 0: normal mode 1: power down mode
2	XI	DI	12MHz crystal, or oscillator input
3	XO	DO	12MHz crystal output
4	DVSS1	P	Digital ground
5	SDAT	DIO	External MCU serial bus data pin
6	SCLK	DI	External MCU serial bus clock pin
7	TEST	DI	Test mode select pin; pull low in normal operation
8	MCLK	DO	External MCU clock pin; clock frequency is programmable (12MHz, 6MHz, 3MHz, 1.5MHz) Default is 1.5 MHz
9	MINT	DO	External MCU interrupt pin (active L) When internal register address 0 ~ 3 or external serial EEPROM is accessed, MINT is set low; after MCU read, MINT is reset to H
10	GPIO1	DIO	GPIO pin #1
11	LEDO	DO	LED for operation; output H for power on; toggling for data transmit
12	LEDR	DO	LED for mute recording indication; output H when recording is muted
13	PHONES	DI	Phone jack sense pin for line out Tri-state; an internal register bit will be set when activated (active H)
14	CS	DO	EEPROM interface chip select
15	SK	DO	EEPROM interface clock
16	DR	DO	EEPROM interface data read
17	DW	DI	EEPROM interface data write
18	USBDP	AIO	USB data D+
19	USBDM	AIO	USB data D-
20	REGV	AO	3.3V reference output for internal 5 → 3.3V regulator
21	DVDD1	P	5V power supply to internal regulator
22	AVSS3	P	Analog ground
23	MICL	AI	Microphone input left channel
24	MICR	AI	Microphone input right channel

25	LINL	AI	Line-In input left channel

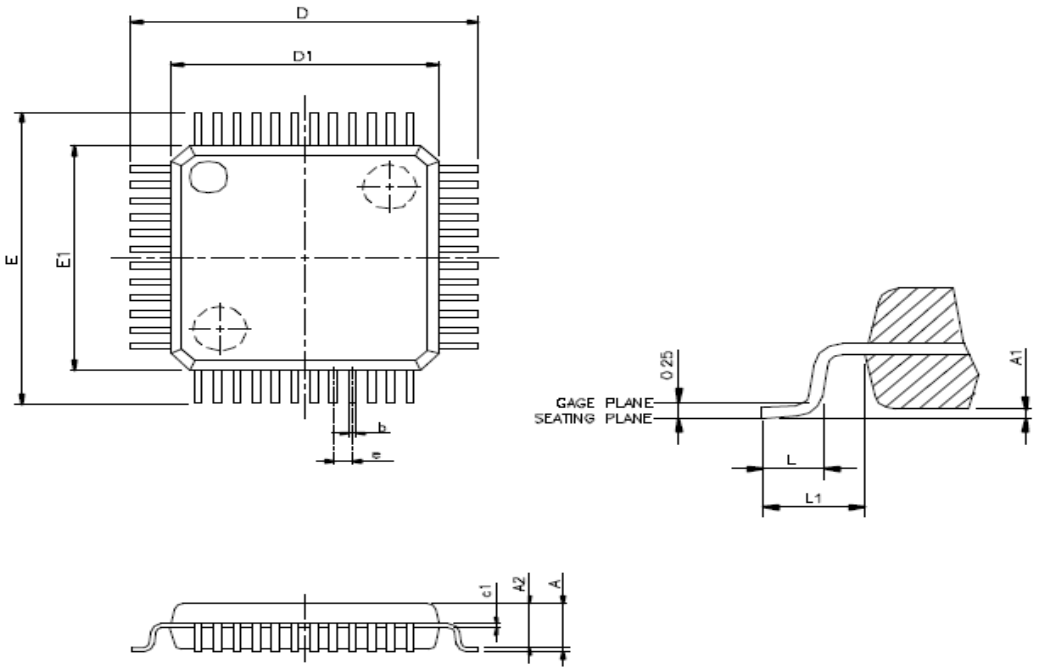
Pin #	Symbol	Type	Description
26	XLINER	AI	Line in right channel
27	AVDD1	P	5V analog power for analog circuit
28	VREF	AO	Connecting to external decoupling capacitor for embedded band-gap circuit; 2.25V output
29	VBIAS	AO	Microphone bias voltage supply (4.5V/2.25V)
30	AVSS1	P	Analog ground
31	HPOL	AO	Headphone out left channel
32	HPOR	AO	Headphone out right channel
33	RSOL	AO	Line out surround (rear) left channel (For Vista definition @ 7.1 CH)
34	RSOR	AO	Line out surround (rear) right channel (For Vista definition @ 7.1CH)
35	FROL	AO	Line out front left channel
36	FROR	AO	Line out front right channel
37	AVDD2	P	5V analog power for analog circuit
38	SSOL	AO	Line out side surround left channel (For Vista definition @ 5.1 / 7.1CH)
39	SSOR	AO	Line out side surround right channel (For Vista definition @ 5.1 / 7.1 CH)
40	CENO	AO	Line out center channel
41	LFEO	AO	Line out LFE (subwoofer) channel
42	AVSS2	P	Analog ground
43	VOLUP	DI	Volume up (edge trigger with de-bouncing)
44	VOLDN	DI	Volume down (edge trigger with de-bouncing)
45	SPDIFI	DI	S/PDIF input
46	MUTER	DI	Mute recording (edge trigger with de-bouncing)
47	MUTEP	DI	Mute playback (edge trigger with de-bouncing)
48	SPDIFO	DO	S/PDIF output

***Note 1:** **DI - digital input pad**
DO - digital output pad
DIO - digital bi-directional pad
AI/AO/AIO - analog pad
P - power pad

***Note 2:** **For LQFP 48 package, PWRSEL, PWRSEL1, MSEL1 and MSEL2 are internal bonding options; all of those 4 pins are notbounded in default state.**

4 Ordering Information

4.1 CM6206 (LQFP48)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0 15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

5 Block Diagram

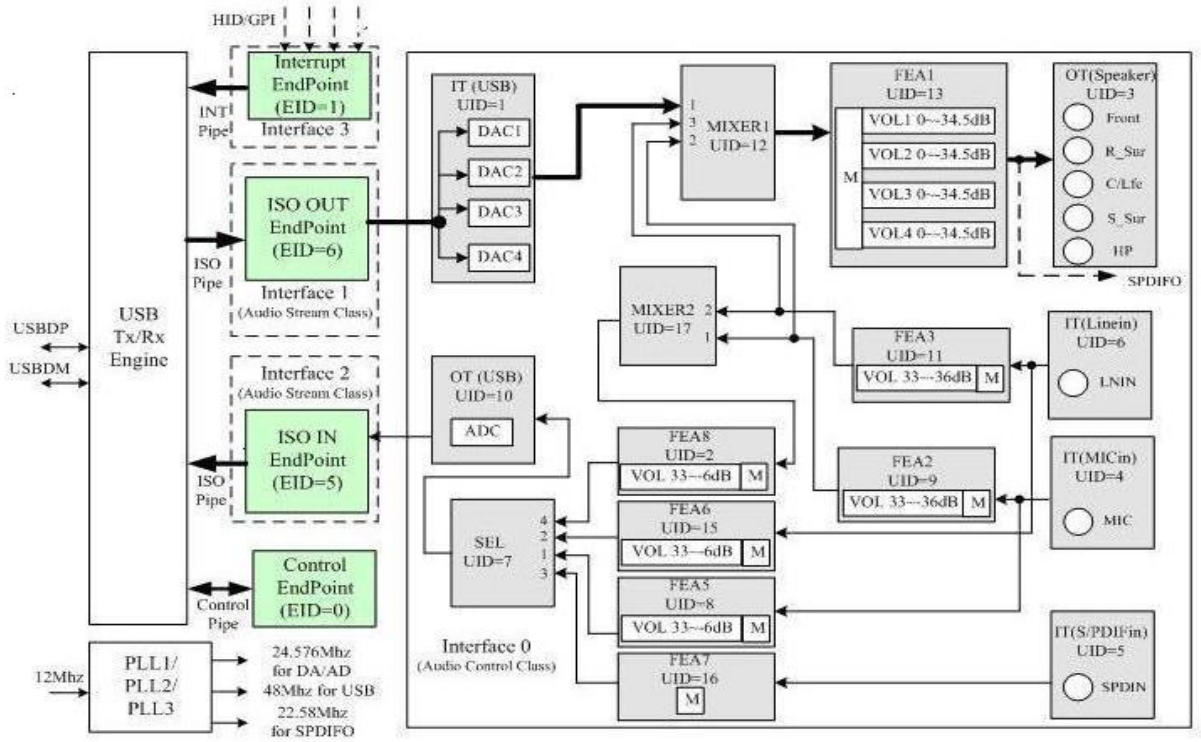


Figure 2 : Function Block Diagram of CM6206

6 Function Descriptions Block Diagram of CM6206

6.1 Internal Register

The internal registers of CM6206 can be divided to two parts. Some of them (REG0, REG1, REG2, REG3, REG4 and REG5) are 16-bit width and can be accessed via HID interface SET_RPT request. The others (REG8~ REG14) are 8-bit width and can be accessed by vendor requests.

To access registers via HID interface, users should issue a “Set Output Report” HID request. The four bytes of output report data is organized as below:

Byte [0]	Bit5 = 1 => Access internal register
	Bit4 = 1 => read Bit4 = 0 => write
Byte [1]	DATAL
Byte [2]	DATAH
Byte [3]	Register address (0, 1, 2, 3, 4, 5)

In addition to internal registers, users can also access external serial EEPROM by the same way:

Byte [0]	Bit6 = 1 => Access EEPROM
	Bit4 = 1 => read Bit4 = 0 => write
Byte [1]	DATAL
Byte [2]	DATAH
Byte [3]	EEPROM address (0 ~ 8'h3f)

REG0 Address: 0x00

SPDIF OUT channel status control Reset State: 0x2000

15	14	13	12	11	10	9	8
DMA_Master	Sampling rate			Category Code[7:4]			

7	6	5	4	3	2	1	0
Category Code[3:0]				Emphasis	Copyright	Non-Audio	PRO/CON

Bit Number	Bit Mnemonic	Read/ Write	Function
15	DMA_Master	R/W	1: SPDIFOUT as Master 0: DACs as Master
14-12	Sampling_rate	R/W	SPDIF out sample rate (48K: 3'b010; 96K: 3'b110)
11-4	Category code	R/W	SPDIF out category code depends on the equipment type.
3	Emphasis	R/W	SPDIFOUT emphasis. 1: emphasis-CD_type 0: Emphasis is not indicated
2	Copyright	R/W	1: not asserted; 0: asserted
1	Non-audio	R/W	1: non-PCM audio data (like AC3) 0: PCM-data
0	Pro/con	R/W	1: professional format 0: consumer

REG1 Address: 0x01

Reset State: 0x3002

15	14	13	12	11	10	9	8
Rsvd	SEL_CLK	PLLBINen	SOFTMUTEen	GPIO4_o	GPIO4_OEN	GPIO3_o	GPIO3_OEN

7	6	5	4	3	2	1	0
GPIO2_o	GPIO2_OEN	GPIO1_o	GPIO1_OEN	Valid	SPDIFLOOP	DIS_SPDIFO	SPDIFMIX

Bit Number	Bit Mnemonic	Read/ Write	Function
15	Rsvd	R/W	Reserved
14	SEL_CLK	R/W	For test. Select 44.1k source for DACs 1=from 22.58M 0=from 24.576M
13	PLLBINen	R/W	PLL binary search enable
12	SOFTMUTEen	R/W	Soft mute enable
11	GPIO4_o	R/W	Gpio4 signal
10	GPIO4_OEN	R/W	Gpio4 output enable
9	GPIO3_o	R/W	Gpio3 signal
8	GPIO3_OEN	R/W	Gpio3 output enable
7	GPIO2_o	R/W	Gpio2 signal
6	GPIO2_OEN	R/W	Gpio2 output enable
5	GPIO1_o	R/W	Gpio1 signal
4	GPIO1_OEN	R/W	Gpio1 output enable
3	VALID	R/W	SPDIFOUT Valid Signal 1=un-valid
2	SPDIFLOOP	R/W	SPDIF loop-back enable
1	DIS_SPDIFO	R/W	SPDIF out disable
0	SPDIFMIX	R/W	SPDIF in mix enable

REG2 Address: 0x02

Reset State: 0x6004

15	14	13	12	11	10	9	8
DRIVERON	HEADPSEL		PLAYMUTE				

7	6	5	4	3	2	1	0
PLAYMUTE					EN_BTL	MCUCLKSEL	

Bit Number	Bit Mnemonic	Read/ Write	Function
15	DRIVERON	R/W	If (HEADPON = 1 and DRIVERON = 0) z All channels muted except Headphone channels Select Headphone source from Front channels Else Channel mute controlled by PLAYMUTE registers Headphone source selected by HEADPSEL registers
14~13	HEADPSEL	R/W	Headphone source select 11: Front channels 10: Center and Subwoofer 01: Surround channels 00: Side channels
12~3	PLAYMUTE	R/W	Channel mute control (high active) PLAYMUTE[0]: mute Left Front PLAYMUTE[1]: mute Right Front PLAYMUTE[2]: mute Center PLAYMUTE[3]: mute Subwoofer PLAYMUTE[4]: mute Side Surround Left PLAYMUTE[5]: mute Side Surround Right PLAYMUTE[6]: mute Rear Surround Left PLAYMUTE[7]: mute Rear Surround Right **PLAYMUTE[8]: 0: mute Headphone Left** **PLAYMUTE[9]: 0: mute Headphone Right**
2	EN_BTL	R/W	1 = BTL mode enable. This bit only useful for 2ch mode.
1~0	MCUCLKSEL	R/W	MCU clock frequency 00: 1.5Mhz 01: 3Mhz

			10: 6Mhz 11: 12Mhz

REG3 Address: 0x03

Reset State: 0x143f / 0x147f

15	14	13	12	11	10	9	8
		FLYSPEED			VRAP25EN	MSEL1	SPDFI_F REQ[1]

7	6	5	4	3	2	1	0
SPDFI_F REQ[0]	PINSEL	FOE	ROE	CBOE	LOSE	HPOE	CANREC

Bit Number	Bit Mnemonic	Read/ Write	Function
15-14	Rsvd	R	Reserved
13-11	FLYSPEED	R/W	Sensitivity to FLY tuner volume control VP/VD signal
10	VRAP25EN	R/W	Microphone bias voltage supply select 0: 4.5V 1: 2.25V
9	MSEL1	R	0: MICINL/R and LIL/R mix to LOFL and LOFR 1: MICINL/R and LIL/R mix to 8 channels
8~7	SPDFI_FREQ	R	SPDIF in sample rate 00: 44.1K 01: reserved 10: 48K 11: 32K
6	PINSEL	R	0: 100 pin package 1: 48 pin package
5	FOE	R/W	1: LOFL/LOFR enable 0: LOFL/LOFR disable (Hi Z)
4	ROE	R/W	1: LOLS/LORS enable 0: LOLS/LORS disable (Hi Z)
3	CBOE	R/W	1: LOCF/LOLFE enable 0: LOCF/LOLFE disable (Hi Z)
2	LOSE	R/W	1: LOSL/LOSR enable 0: LOSL/LOSR disable (Hi Z)
1	HPOE	R/W	1: HPOUTL/HPOUTR enable 0: HPOUTL/HPOUTR disable (Hi Z)
0	CANREC	R	SPDIF in recording status 0: SPDIF in can not be recorded 1: SPDIF in can be recorded

REG4 Address: 0x04

Reset State: 0x0000

15	14	13	12	11	10	9	8
GPIO12_o	GPIO12_ OEN	GPIO11_o	GPIO11_ OEN	GPIO10_o	GPIO10_ OEN	GPIO9_o	GPIO9_ OEN

7	6	5	4	3	2	1	0
GPIO8_o	GPIO8_ OEN	GPIO7_o	GPIO7_ OEN	GPIO6_o	GPIO6_ OEN	GPIO5_o	GPIO5_ OEN

Bit Number	Bit Mnemonic	Read/ Write	Function
15	GPIO12_o	R/W	Gpio12 signal
14	GPIO12_OEN	R/W	Gpio12 output enable
13	GPIO11_o	R/W	Gpio11 signal
12	GPIO11_OEN	R/W	Gpio11 output enable
11	GPIO10_o	R/W	Gpio10 signal
10	GPIO10_OEN	R/W	Gpio10 output enable
9	GPIO9_o	R/W	Gpio9 signal
8	GPIO9_OEN	R/W	Gpio9 output enable
7	GPIO8_o	R/W	Gpio8 signal
6	GPIO8_OEN	R/W	Gpio8 output enable
5	GPIO7_o	R/W	Gpio7 signal
4	GPIO7_OEN	R/W	Gpio7 output enable
3	GPIO6_o	R/W	Gpio6 signal
2	GPIO6_OEN	R/W	Gpio6 output enable
1	GPIO5_o	R/W	Gpio5 signal
0	GPIO5_OEN	R/W	Gpio5 output enable

REG5 Address: 0x05

Reset State: 0x3000

15	14	13	12	11	10	9	8
Rsvd		DA_RSTN	AD_RSTN	AD2SPDO	SPDO_SEL		CODEM

7	6	5	4	3	2	1	0
EN_HPF	T_SEL_DSDA4	T_SEL_DSDA3	T_SEL_DSDA2	T_SEL_DSDA1	T_SEL_DSAD		

Bit Number	Bit Mnemonic	Read/ Write	Function
15-14	Rsvd	R	Reserved
13	DA_RSTN	R/W	DAC delta-sigma reset signal
12	AD_RSTN	R/W	ADC delta-sigma reset signal
11	AD2SPDO	R/W	1: enable ADC data to SPDIFOUT
10-9	SPDO_SEL	R/W	SPDIFOUT channel selector 00: Front; 01: Side_Sur; 10: CEN/LFE; 11: Rear_Sur
8	CODECM	R/W	0: USB mode; 1: CODEC mode
7	EN_HPF	R/W	1: Enable DAC high pass filter
6	T_SEL_DSDA4	R/W	1: Loopback ADC 1-bit delta-sigma data to RearSurround DAC
5	T_SEL_DSDA3	R/W	1: Loopback ADC 1-bit delta-sigma data to CEN/LFE DAC
4	T_SEL_DSDA2	R/W	1: Loopback ADC 1-bit delta-sigma data to SideSurround DAC
3	T_SEL_DSDA1	R/W	1: Loopback ADC 1-bit delta-sigma data to Front DAC
2-0	T_SEL_DSAD	R/W	Select delta-sigma 1-bit input source to AD digital filter. 000: normal; 100: Front; 101: SSurround; 110: Cen/LFE; 111: RSurround

CM6206 supports two vendor specific requests. The formats of vendor requests are shown below:

Vendor command writes

Offset	Field	Size	Value (H)	Description
0	bmRequestType	1	43	
1	bRequest	1	01	
2	wValue_L	1	Data	Write data
3	wValue_H	1	00	
4	wIndex	2	Address	Write address
6	wLength	2	0000	

Vendor command reads

Offset	Field	Size	Value (H)	Description
0	bmRequestType	1	C3	
1	bRequest	1	81	
2	wValue	2	0000	
4	wIndex	2	Address	Read address
6	wLength	2	Length	Length must less than or equal to 4

There are only two registers can be accessed via vendor requests.

REG8 Address: 0x08

Reset State: 0xb2

7	6	5	4	3	2	1	0
UNENCRDATA							

Bit Number	Bit Mnemonic	Read/ Write	Function
7-0	UNENCRDATA	R/W	Raw data for encryption (write) or after encryption (read)

REG9 Address: 0x09

Reset State:

7	6	5	4	3	2	1	0
MSEL1	SEL 3	SEL 2	PINSEL	MSEL2	HIDEN	SEL 1	SEL 0

Bit Number	Bit Mnemonic	Read/ Write	Function
7	MSEL1	R	MSEL1 bonding option value
6	SEL3	R	SEL3 bonding option value
5	SEL2	R	SEL2 bonding option value
4	PINSEL	R	PINSEL bonding option value
3	MSEL2	--	
2	HIDEN	R	0: No HID Function 1: With HID Function
1	SEL1	R	SEL1 bonding option value
0	SEL0	R	SEL0 bonding option value

REG10 Address: 0x0a

Reset State: 0x05

7	6	5	4	3	2	1	0
CHIP-ID							

Bit Number	Bit Mnemonic	Read/ Write	Function
7-0	CHIP-ID	R	Low byte of CHIP ID

REG11 Address: 0x0b

Reset State: 0x50

7	6	5	4	3	2	1	0
CHIP-ID							

Bit Number	Bit Mnemonic	Read/ Write	Function
7-0	CHIP-ID	R	High byte of CHIP ID

REG12 Address: 0x0c

Reset State: 0x00

7	6	5	4	3	2	1	0
FDBK1							

Bit Number	Bit Mnemonic	Read/ Write	Function
7-0	FDBK1	R/W	Lowest byte of Feedback information for ISO OUT

REG13 Address: 0x0d

Reset State: 0x00

7	6	5	4	3	2	1	0
FDBK2							

Bit Number	Bit Mnemonic	Read/ Write	Function
7-0	FDBK2	R/W	Middle byte of Feedback information for ISO OUT

REG14 Address: 0x0e

Reset State: 0x00

7	6	5	4	3	2	1	0
FDBK3							

Bit Number	Bit Mnemonic	Read/ Write	Function
7-0	FDBK3	R/W	Highest byte of Feedback information for ISO OUT

6.2 MCU Interface

CM6206 can communicate with external MCU via two-wire serial interface and act as a slave device. By this way, MCU can read four bytes from and write two bytes to USB host through CM6206. When MCU writes two bytes to CM6206, the data will be transferred to USB host via HID 'Input Report'. USB host will keep polling HID report every 1ms. CM6206 can also transfer four bytes from USB host to MCU. This is accomplished by a 'Set Output Report' HID request issued by USB host.CM6206 will then assert MINT to inform MCU to read them.

CM6206 has one input pin 'SCLK' to get serial clock from MCU, and one open-drain output pin 'SDAT' to send or receive serial signal to/from MCU. As shown below, 'SDAT' should be stable when 'SCLK' is high, and can have transition only when 'SCLK' is low.

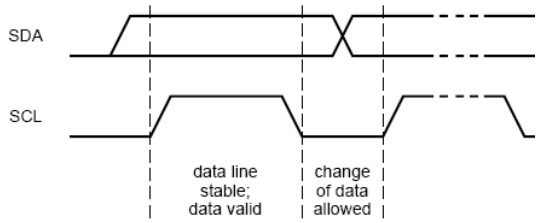


Figure 6-1. IIC data to clock protocol

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

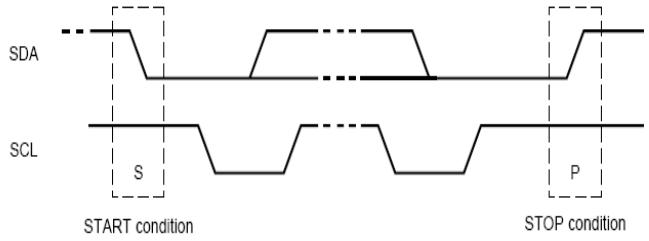


Figure 6-2. IIC start/stop condition protocol

The figure below demonstrates a transaction example. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow.

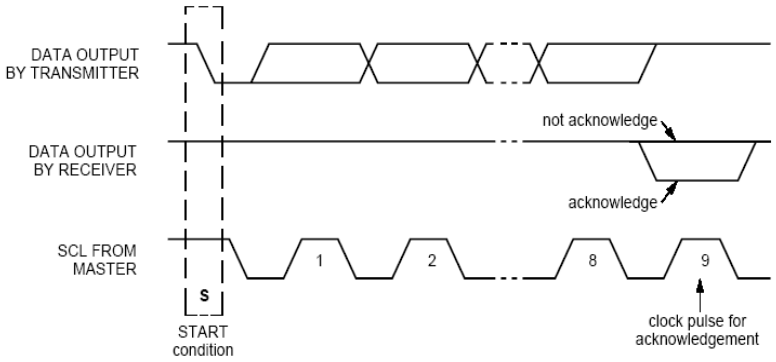


Figure 6-3. IIC transaction example

The figure below shows typical transactions between MCU and CM6206. After a START, MCU should send 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low.

MCU write:

S	8'h70	0	8'h01	0	Byte[1]	0	Byte[2]	1	P

MCU read:

S	8'h70	0	8'h00	1								
S	8'h71	0	Byte[0]	0	Byte[1]	0	Byte[2]	0	Byte[3]	1	P	

	From CM6206 to MCU		From MCU to CM6206
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte	One byte data		

In a write transfer, MCU keeps acting as the transmitter. CM6206 regards the first DATA byte as start register address. The second and third DATA bytes are the content that MCU writes to the register addresses.

In a read transfer, two transactions are necessary. MCU resets start register address by the first transaction. Then MCU changes to be the receiver during the second transaction to get four bytes of data.

6.3 Serial EEPROM Content

CM6206 supports four-wire serial EEPROM interface. When an external serial EEPROM is detected, Vendor ID and Product ID reported within Device Descriptor will be derived from the content of serial EEPROM. The organization of serial EEPROM is shown below:

Address = 0	16'h434dX
Address = 1	Vendor ID
Address = 2	Product ID
Address = 3	String 1,String 0
Address = 4	String 3,String 2
Address = 5	String 5,String 4
Address = 6	String 7,String 6
Address = 7	String 9,String 8
Address = 8	String 11,String 10
Address = 9	String 13,String 12
Address = 10	String 15,String 14
Address = 11	String 17,String16
Address = 12	String 19,String 18
Address = 13	String 21,String 20
Address = 14	String 23,String 22
Address = 15	
Address = 16	
Address = 17	
Address = 18	
Address = 19	
Address = 20	{8'dx,MString 0}
Address = 21	{8'dx,MString 1}
Address = 22	{8'dx,MString 2}
Address = 23	{8'dx,MString 3}
Address = 24	{8'dx,MString 4}
Address = 25	{8'dx,MString 5}
Address = 26	{8'dx,MString 6}
Address = 27	{8'dx,MString 7}
Address = 28	{8'dx,MString 8}
Address = 29	{8'dx,MString 9}
Address = 30	{8'dx,MString 10}
Address = 31	{8'dx,MString 11}
Address = 63	16'hXXXX

Users can program serial EEPROM via HID interface, as described in the former section. The first word is a magic code. Only when it matches, CM6206 will regard the serial EEPROM valid.

6.4 Audio Interface Format In Codec Mode

In codec mode, audio data is applied to the internal DAC filters or output from ADC filters, via the Digital Audio Interface. 2 popular interface formats are supported: Left Justified mode and I^2S mode. Both formats send the MSB first and note that the DAC filters only support 22-bit.

6.5 Left Justified Mode

In left justified mode, the MSB of DIN is sampled by RTKIP0 on the first rising edge of DACBCLK following a DACLRCK transition. The MSB of the ADC data is output on DOUT and changed on the same falling edge of ADCBCLK as ADCLRCK and may be sampled on the rising edge of ADCBCLK. ADCLRCK and DACLRCK are high during the left samples and low during the right samples. The timing diagram is illustrated in Figure 5-16. The polarity of ADCBCLK/DACBCLK and ADCLRCK/DACLRCK can be inverted by SPI register 01h and 02h.

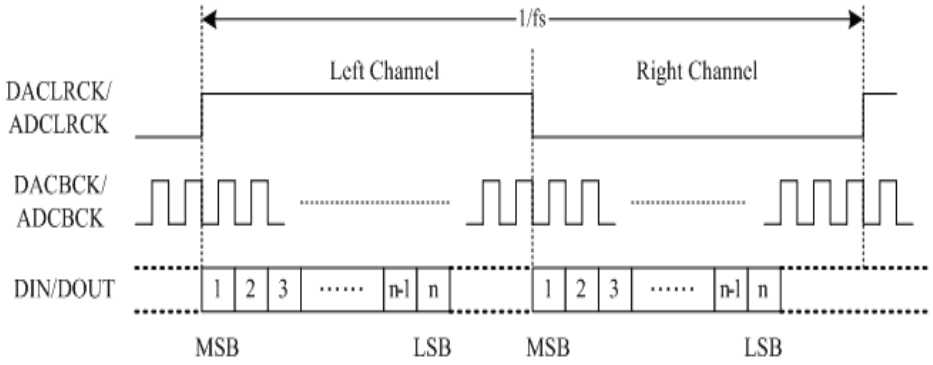


Figure 6-4. Left Justified Mode Timing Diagram

6.6 Power Management

To meet suspend current specification of USB; CM6206 turns off most blocks when entering suspend. The only two exceptions are power-on-reset and regulator.

To meet un-configured current specification of USB, CM6206 provides a control signal PDSW to turn off external components. PDSW would be active when USB host does not configure CM6206. PDSW would also be active when CM6206 is suspended. If serial EEPROM is exist, notice that it should not be powered off anyway because it contains Vendor ID and Product ID which should be returned to USB host before CM6206 is configured.

7 Volume Control

7.1 DAC Volume Control

VOL_*_ <5:0>	Scale (linear)	VOL_*_<5:0>	Scale (linear)	VOL_*_<5:0>	Scale (linear)	VOL_*_<5:0>	Scale (linear)
00	1.000	10	0.724	20	0.448	30	0.171
01	0.973	11	0.696	21	0.420	31	0.144
02	0.944	12	0.669	22	0.392	32	0.116
03	0.917	13	0.641	23	0.365	33	0.088
04	0.890	14	0.613	24	0.337	34	0.061
05	0.862	15	0.586	25	0.309	35	0.033
06	0.834	16	0.558	26	0.282	36	0.006
07	0.807	17	0.530	27	0.254	37	mute
08	0.779	18	0.503	28	0.227		
09	0.751	19	0.475	29	0.199		

Note: VOL_*_ stands for VOL_FL_, VOL_FR_, VOL_CF_, VOL_LFE_, VOL_LS_, VOL_RS_, VOL_SL_, VOL_SR_. The volume control is in linear scale.

7.2 ADC Volume Control

Note: VOL_*_ stands for VOL_REC_L_ and VOL_REC_R_. The volume control is in log scale.

USB Request Data (Hex)	VOL_*_<4:0>	Scale (log)	USB Request Data (Hex)	VOL_*_<4:0>	Scale (log)
0B7F~0B00	11111	+33dB	047F~0400	10001	+12dB
0AFF~0A80	11110	+31.5dB	03FF~0380	10000	+10.5dB
0A7F~0A00	11101	+30dB	037F~0300	01111	+9dB
09FF~0980	11100	+28.5dB	02FF~0280	01110	+7.5dB
097F~0900	11011	+27dB	027F~0200	01101	+6dB
08FF~0880	11010	+25.5dB	01FF~0180	01100	+4.5dB
087F~0800	11001	+24dB	017F~0100	01011	+3dB
07FF~0780	11000	+22.5dB	00FF~0080	01010	+1.5dB
077F~0700	10111	+21dB	007F~0000	01001	0dB
06FF~0680	10110	+19.5dB	FFFF~FC00	01000	-1.5dB
067F~0600	10101	+18dB	FBFF~F800	00111	-3dB
05FF~0580	10100	+16.5dB	F7FF~F400	00110	-4.5dB
057F~0500	10011	+15dB	F3FF~F000 / 8000	00101	-6dB
04FF~0480	10010	+13.5dB	EFFF~EC00	00100	-6dB

Note: VOL_*_ stands for VOL_REC_L_ and VOL_REC_R_. The volume control is in log scale.

7.3 MIC / Line-in Monitor Volume Control

VOL_*_<4:0>	Scale (log)	VOL_*_<4:0>	Scale (log)	VOL_*_<4:0>	Scale (log)	VOL_*_<4:0>	Scale (log)
00	+12.0dB	08	0.0dB	16	-12.0dB	24	-24.0dB
01	+10.5dB	09	-1.5dB	17	-13.5dB	25	-25.5dB
02	+9.0dB	10	-3.0dB	18	-15.0dB	26	-27.0dB
03	+7.5dB	11	-4.5dB	19	-16.5dB	27	-28.5dB
04	+6.0dB	12	-6.0dB	20	-18.0dB	28	-30.0dB
05	+4.5dB	13	-7.5dB	21	-19.5dB	29	-31.5dB
06	+3.0dB	14	-9.0dB	22	-21.0dB	30	-33.0dB
07	+1.5dB	15	-10.5dB	23	-22.5dB	31	mute

Note: VOL_*_ stands for VOL_MICM_L_, VOL_MICM_R_, VOL_LINEM_L_, VOL_LINEM_R_. The volume control is in log scale.

8 Electrical Characteristics

8.1 Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Digital power voltage	DVDD	4.5	5.5	V
Analog power voltage	AVDD	4.5	5.5	V
Digital Input Voltage	VIND	-0.5	3.6	V
Analog Input Voltage	VINA	-0.5	5.5	V
Operating temperature range	TO	0	70	°C
Storage temperature range	TST	-40	125	°C
Power dissipation	PDMAX		900	mW

8.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Operating Voltage	DVDD	4.75	5	5.25	V
Analog Operating voltage	AVDD	4.75	5	5.25	V
Operating Ambient Temperature	TO	0	25	70	°C

8.3 Power Consumption

Parameter	Min.	Typ.	Max.	Unit
Power Supply Current (Normal)				
AVDD (5.0V)	-	120	-	mA
DVDD (5.0V)	-	35	-	mA

8.4 DC Characteristics (Digital)

PARAMETER	Symbol	Condition	Min.	Typ.	Max.	Unit
Input high voltage	VIH		2.0	-	VDD+0.3	V
Input low voltage	VIL		-0.5	-	0.8	V
Output high voltage	VOH	I_{OH}= 4mA	2.4	-	VDD	V
Output low voltage	VOL	I_{OL}= -4mA	0.0	0.2	0.4	V
Input Leakage Current	IIL	0<Vin<VDD	-70	-	70	μA
Input Pin Capacitance	Cin		-	-	10	pF
Pin Inductance	Lpin		-	-	20	nH

8.5 AC Characteristics (Digital)

Parameter	Symbol	Condition	Min.	Max.	Units
Output Rise Slew Rate	SLEWr	0.2Vdd-0.6Vdd load	1	4	V/ns
Output Fall Slew Rate	SLEWf	0.6Vdd-0.2Vdd load	1	4	V/ns

8.6 Analog Performance

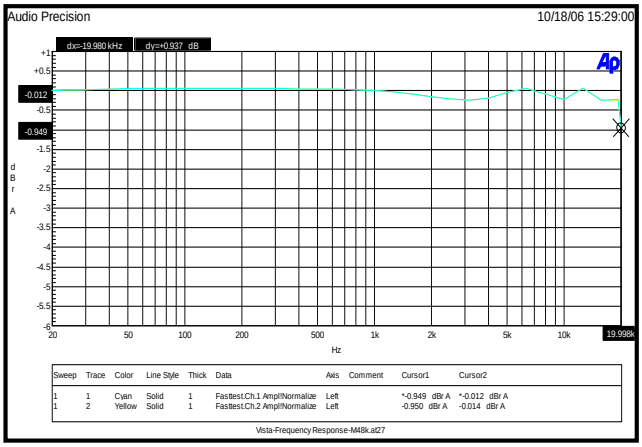
The measurements are performed under the circumstance as:
Tambient = 25℃, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, 10kΩ/50pF external load. Input is 1 kHz sine wave; Sampling frequency = 48 kHz; Bandwidth = 20 to 20 kHz; 0dB attenuation; All sound effects such as 3D effects are disabled.

Parameter	Minimum	Typical	Maximum	Units
Full Scale Input Voltage:				
Line Inputs (Mixer)	-	1.1	1.25	Vrms
Line Inputs (A/D)	-	1.1	1.25	Vrms
Mic Inputs (33dB Maxinum)	-	0.1	1.25	Vrms
Full Scale Output Voltage:				
Front_Out	-	1.1	-	Vrms
Side_Surround_Out	-	1.1	-	Vrms
Center / LFE_out	-	1.1	-	Vrms
Back_Surround_Out	-	1.1	-	Vrms
SNR (Idle)				-
D/A	96	97	-	dBFSA
A/D	80	85	-	dBFSA
Dynamic Range (-60dB)				
D/A	-	96	-	dBFSA
A/D	-	91	-	dBFSA
THD+N				
D/A	-	-88	-	dBFS
A/D	-	-88	-	dBFS
Frequency Response				
D/A	16	-	19,200	Hz
A/D	16	-	19,200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800		∞	Hz
Stop Band Rejection	-	-75	-	dB
Out-Of-Band Rejection	-	-65	-	dB
Power Supply Rejection Ratio	-	-40	-	dB
Master Volume Gain (38 steps)				
Step Size		Linear		
Control Range	-34.5		0	dB
Analog Input Gain (48 steps)				
Step Size		1.5		dB
Control Range	-36	-	+22.5	dB
Recording Gain (26 steps)				
Step Size		1.5		dB
Control Range	-6	-	+33	dB
Input Impedance				
Line-In, CD, MIC, PCSPK	-	20	-	KΩ
Vrefout	-	2.25	-	V

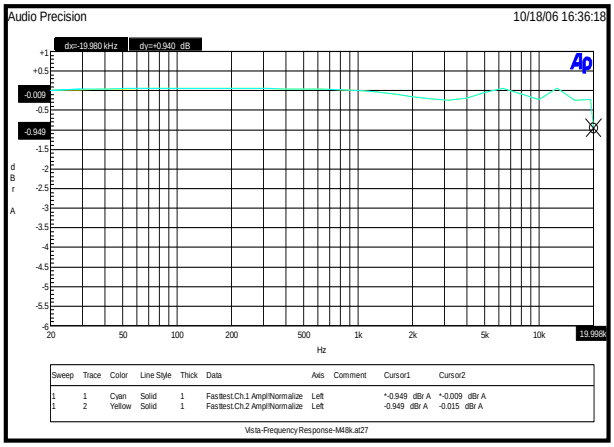
9 Audio Performance Curves

9.1 10K loading (Line Out / Surround / Center LFE / Side Surround) Frequency Response

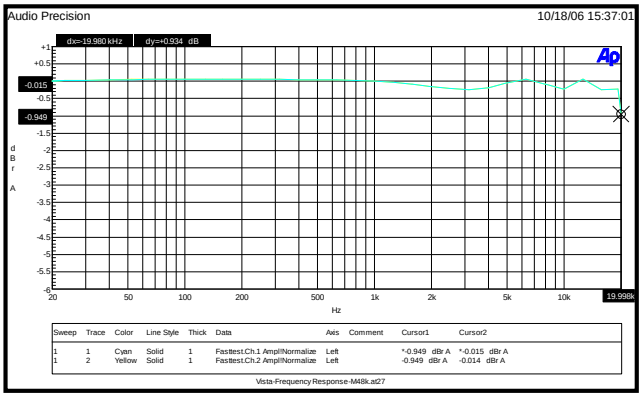
Front out



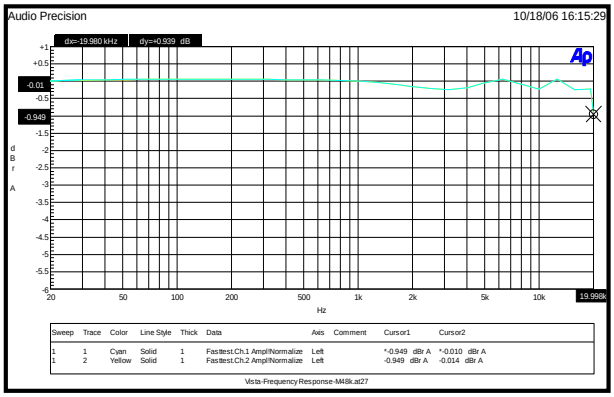
Center LFE out



Surround out

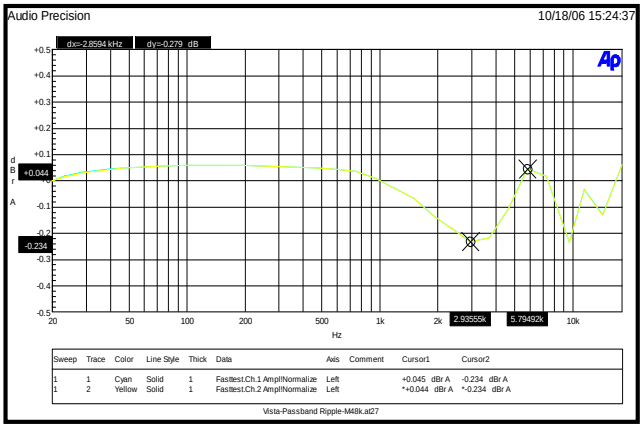


Side Surround out

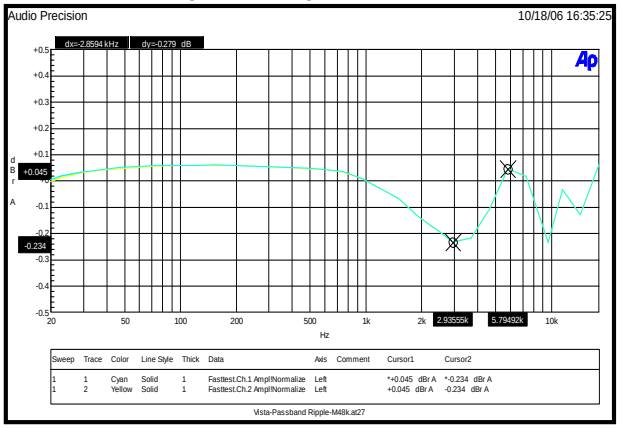


9.2 10K loading (Line Out / Surround / Center LFE / Side Surround) Passband Ripple

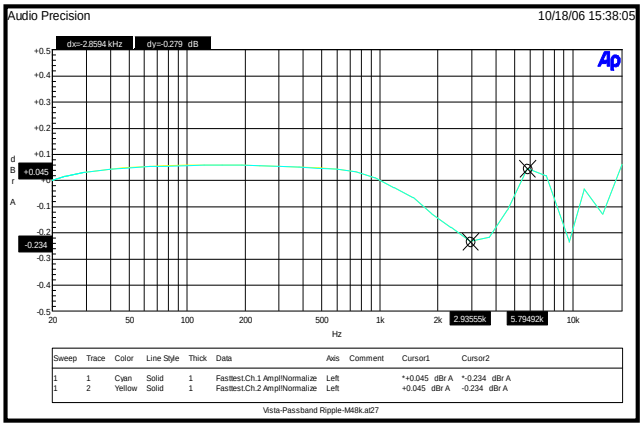
Front out



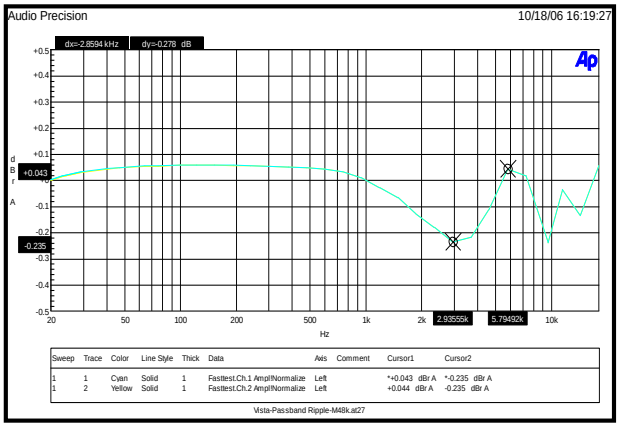
Center LFE Out



Surround out

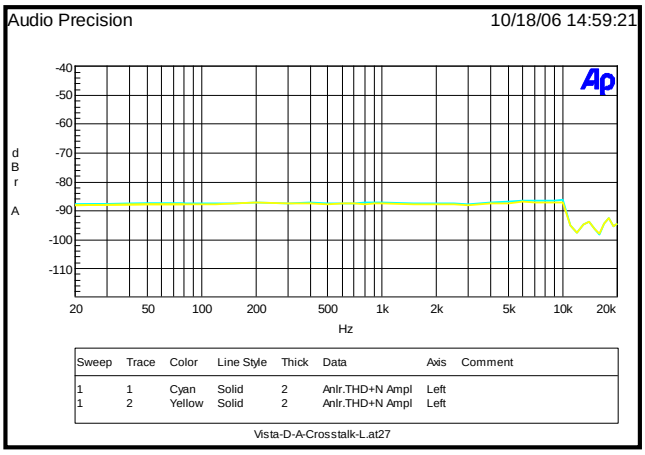


Side Surround out

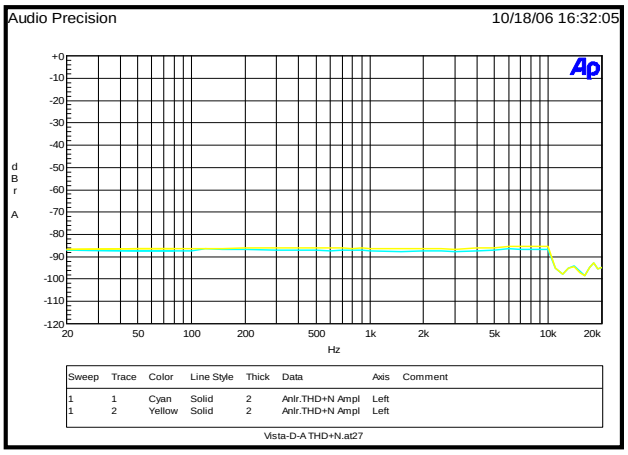


9.3 10K loading (Line Out / Surround / Center LFE / Side Surround) THD+N Curve

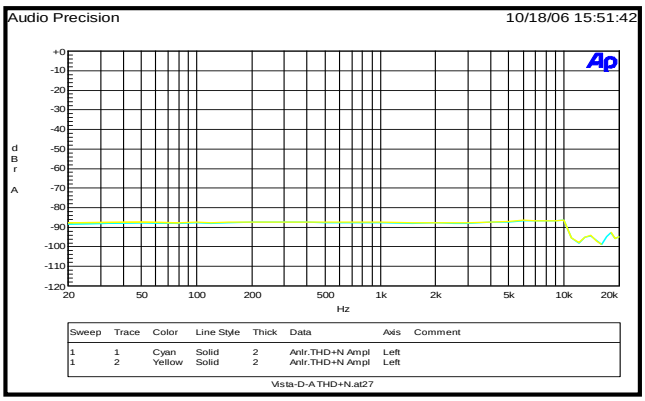
Front out



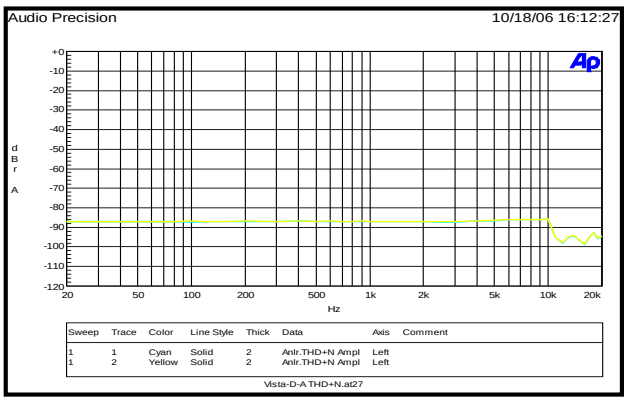
Center LFE Out



Surround out

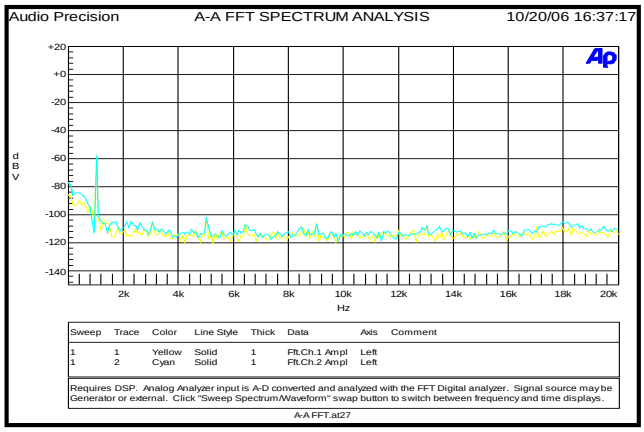


Side Surround out

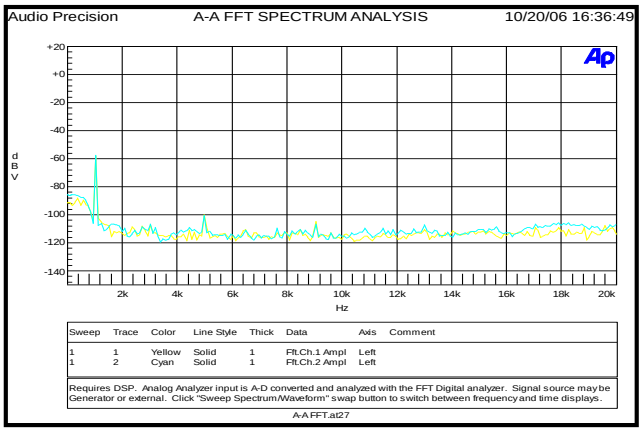


9.4 10K loading (Line Out / Surround / Center LFE / Side Surround) Dynamic Range

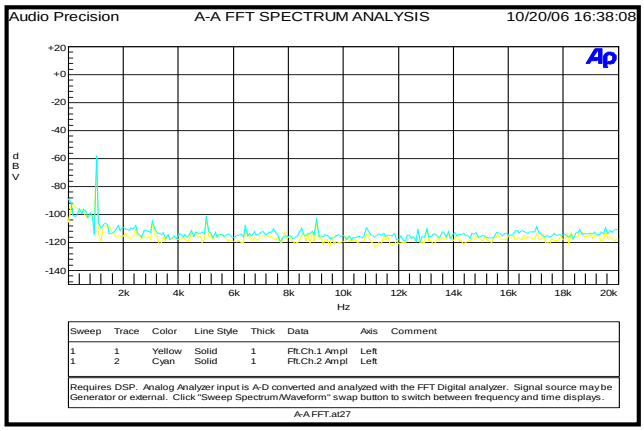
Front out



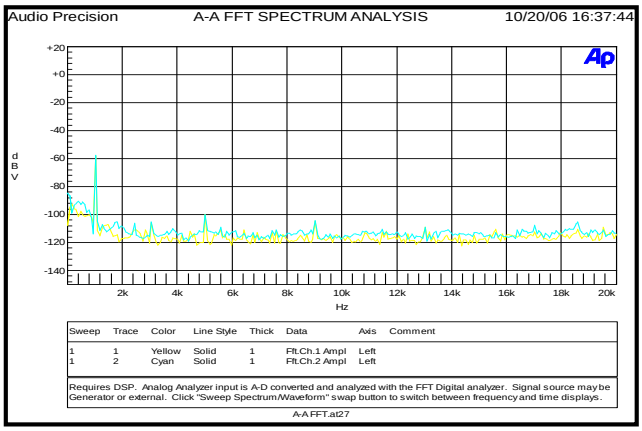
Center LFE Out



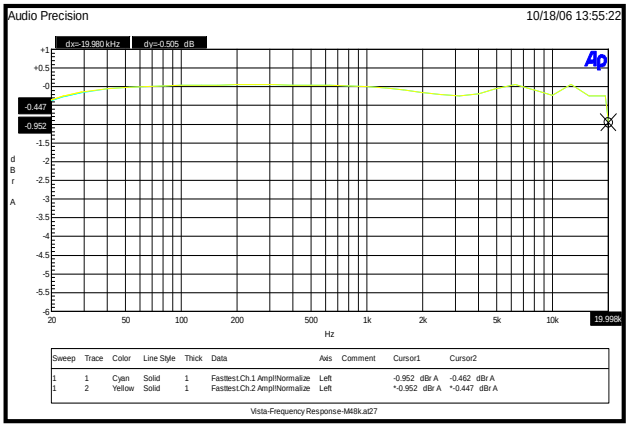
Surround out

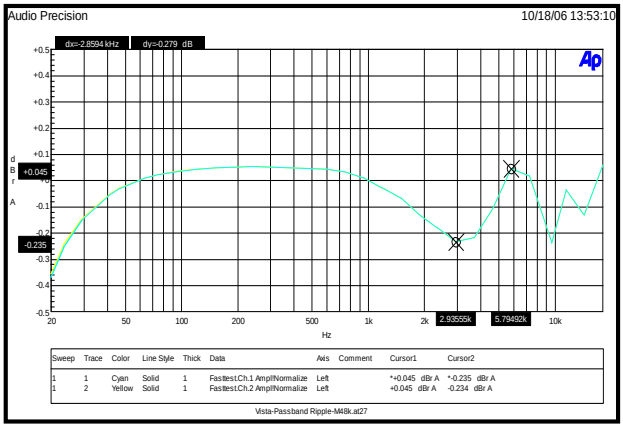


Side Surround out

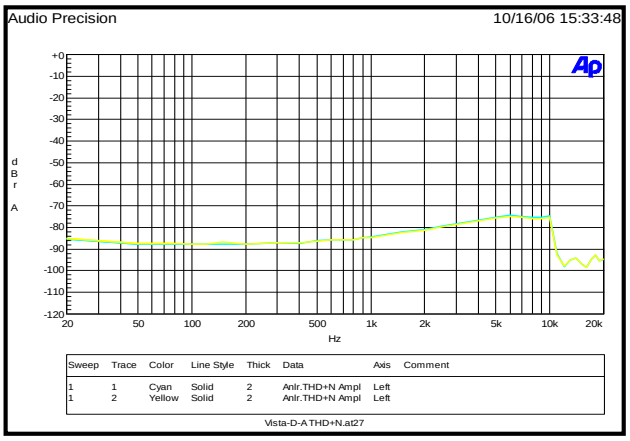


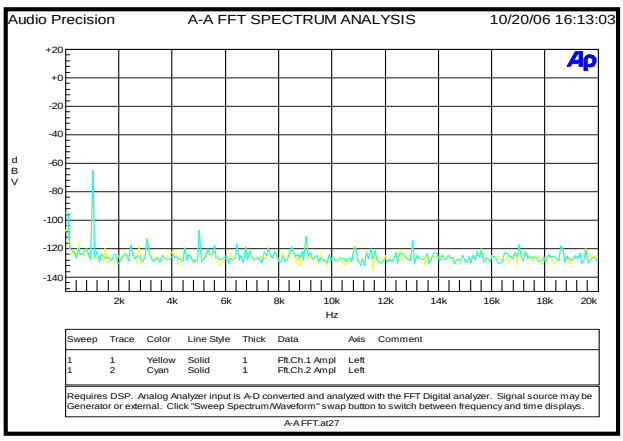
9.5 32 ohm Headphone Loading Frequency Response / Passband Ripple



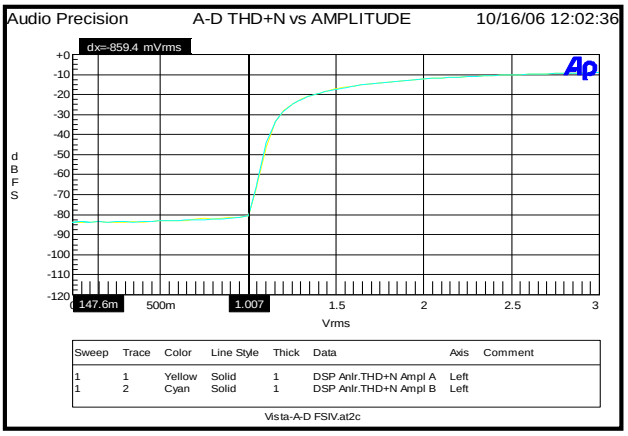


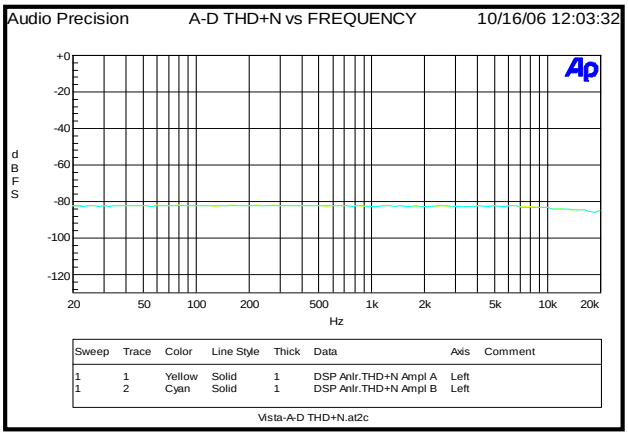
9.6 32 ohm Headphone Loading THD+N Curve / Dynamic Range



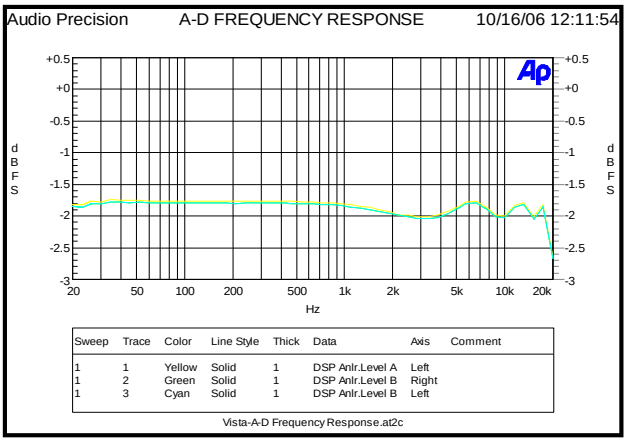


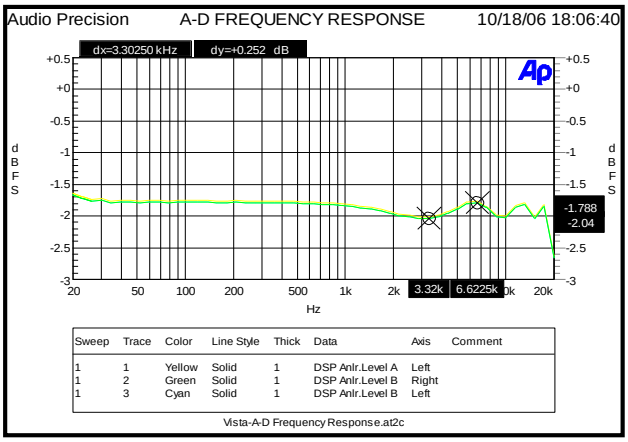
9.7 A-D Line in FSIV / THD+N Curve



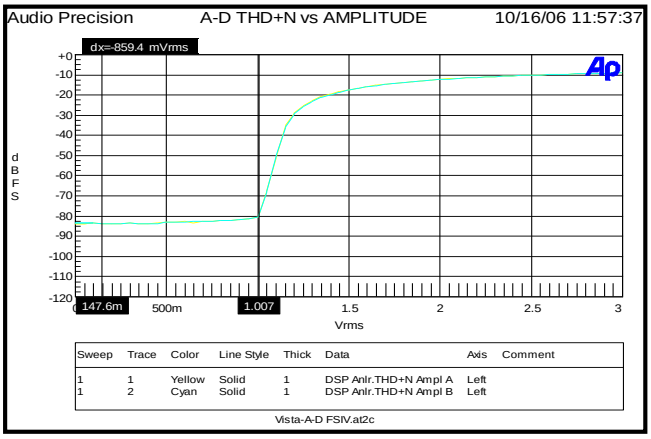


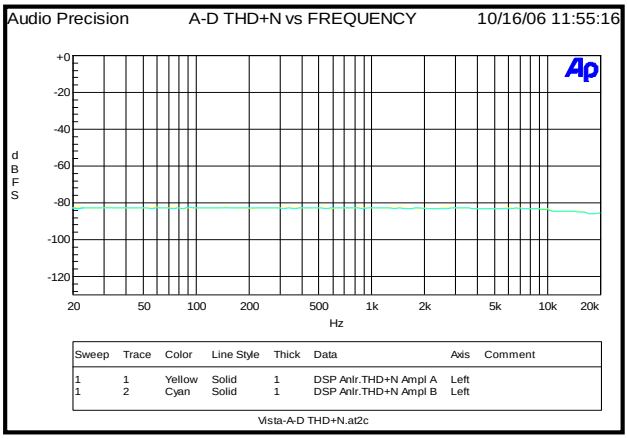
9.8 A-D Line in Frequency Response / Passband Ripple



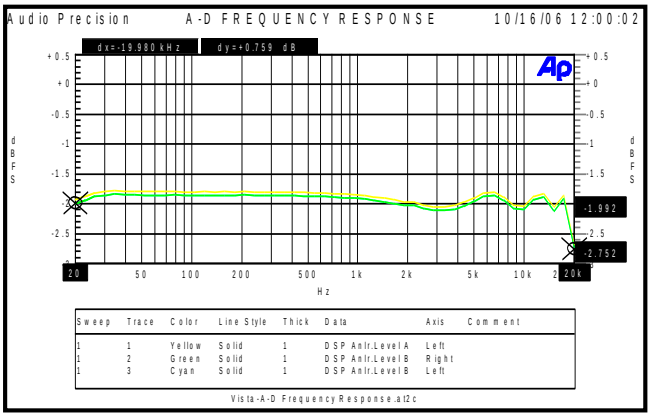


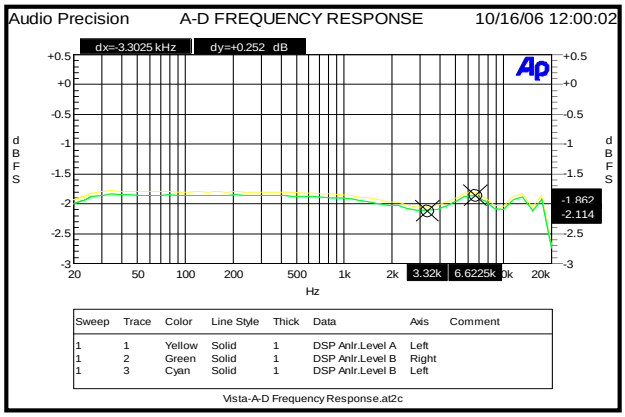
9.9 A-D Mic in FSIV / THD+N Curve





9.10 A-D Mic in Frequency Response / Passband Ripple





Reference

USB-IF, USB Specification, Revision 1.1 and 2.0, and USB Audio Device Class Specification, Revision 1.0.

—End of Specifications—

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