[AIR-RISCV Module Specification]

Purpose:
- Defines instruction-level implementation of AIR DSP pipeline for RISC-V architecture
- Serves as low-level abstraction target from AIR-Runtime module

Note: This module was co-developed via GPT-4o-based prompt-driven vibe coding in collaboration with 제현.

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[1] AIR Instruction Set (AIR-ISA)
- AIR_MULQ31(rd, rs1, rs2): Multiply two Q31 values with saturation
- AIR_MDCT16(rd, rs): 16-point MDCT transform on input block
- AIR_QUANT8(rd, rs, bitdepth): Subband quantizer to 8-bit
- AIR_VECMAP(rd, rs): Convert float32 to Q31 (normalized)
- AIR_PACK(rd, rs1, rs2): Packetize spectral frame + header

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[2] Pipeline Flow (RISC-V Assembly Mapping)
1. Load PCM block → buffer
2. AGC/NS: Optional preprocessor (external or AIR_VECMAP)
3. Transform: AIR_MDCT16 + AIR_MULQ31 windowing
4. Quantize: AIR_QUANT8 per band
5. Encode: AIR_PACK with frame header
6. Store to output buffer

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[3] Special Registers
- QACC: 64-bit accumulator for Q31
- LATENCY_CTL: frame-time budget register (μs)
- FORMAT_FLAG: runtime format switching control (FP/Q/BFP)

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[4] Compatibility
- Follows RISC-V DSP Extension spec (rv32dsp / rv64dsp)
- Can run on FPGA emulation (LiteX, PicoRV32, etc)
- Compatible with AIR-Runtime if used as execution backend

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