Using split-gate structures to explore the implementation of a coupled-electron-waveguide qubit scheme

2007 J. Phys.: Condens. Matter 19 276205

(http://iopscience.iop.org/0953-8984/19/27/276205)

IOP PUBLISHING JOURNAL OF PHYSICS: CONDENSED MATTER

J. Phys.: Condens. Matter **19** (2007) 276205 (15pp) doi:10.1088/0953-8984/19/27/276205

Using split-gate structures to explore the implementation of a coupled-electron-waveguide qubit scheme

A Ramamoorthy[1], J P Bird[2] and J L Reno[3]

[1] Nanostructures Research Group, Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287-5706, USA
[2] Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, NY 14260-1920, USA
[3] Center for Integrated Nanotechnologies, Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185-1303, USA

E-mail: arunkumar@asu.edu and jbird@buffalo.edu

Received 5 April 2007, in final form 6 April 2007
Published 20 June 2007
Online at stacks.iop.org/JPhysCM/19/276205

Abstract

We explore the use of the split-gate method to implement coupled-electron waveguides (CEWs), for possible application as a scalable qubit in quantum computing. Electron switching in these structures is found to be strongly influenced by structural asymmetry, which appears to arise quite naturally when using the split-gate method to implement complicated nanostructures. The consequences of the asymmetry are shown to depend strongly on the manner in which the input and output ports of the device are configured, and include unwanted decoherence due to geometry-induced scattering of electrons into regions outside of the classical current path. An approach to eliminating the influence of this asymmetry, to allow the realization of a 'balanced qubit', is also explored.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Quantum computing promises manifold improvements over conventional (classical) computing, in fields such as computational science, cryptography, and secure communications. Central to this approach is the existence of a physically well-defined *qubit*, the quantum analogue of the conventional two-state bit that is used in classical digital logic. To provide compatibility with existing microelectronic technology, and the promise of scale-up to large networks, a solid-state approach to qubit realization is highly desirable. A number of different solid-state qubits are currently being explored in the literature, making use of distinct physical phenomena. Charge- and flux-based superconducting qubits have already been demonstrated

successfully, although their operation is restricted to extremely low temperatures [1–7]. Other promising schemes include efforts to use nuclear [8] and electron [9–11] spins as the basis of a qubit. Recent work on single-electron spins in quantum dots, in particular, has demonstrated great strides in the readout and manipulation of single spins [12–14]. Another idea that has attracted attention involves using coupled-electron waveguides (CEWs) to implement *electron-wave* qubits [15–21]. The functionality of such qubits derives from allowing two otherwise independent quantum wires (QWs), through which electrons propagate ballistically while maintaining the coherence of their wavefunction, to overlap in a short-coupling region. (We shall use the terms 'waveguide', 'wire' and 'QW' interchangeably here to refer to the same object.) When the properties (dimensions, local potential barrier) of this coupling window are modified through external control, the resulting change in electron interference in the coupling region is expected to induce the switching of electron waves between the wires [17]. The logic states ('1' or '0') of these qubits are defined by the presence of an electron in one wire or the other, and the ability of the coupling window to split the wavefunction between *both* wires should allow for the creation of the superposition states necessary for quantum computing. Both Gaussian-wavepacket [15] and plane-wave based [19] implementations of this qubit have been considered theoretically, and logic operations based on multiply-coupled qubits have also been proposed [20, 21]. In spite of the intense theoretical interest, however, there has been no successful demonstration of this qubit system to date. (It should be mentioned that there *have* previously been several experiments exploring wave switching in coupled QWs, although none of these were performed in the context of qubit realization [22–26].)

Recently, we have reported on our efforts to implement a CEW qubit by making use of the split-gate approach [27, 28]. This work has highlighted a significant obstacle to implementation of the qubit, in the form of structural asymmetry that appears to arise almost inevitably in devices realized by this method. In [28], we reported how this asymmetry contributes to a novel NOT switching behaviour, in which electrons injected into one waveguide are scattered with high efficiency into the other. On the basis of the temperature-dependent characteristics of this effect, it was suggested that a complicated interplay of both structural asymmetry and quantum transport were responsible for this effect. In this report, we present the result of a new and extensive study of switching in this system, further clarifying the role of structural asymmetry while identifying further issues associated with the implementation of CEWs by this approach. An important result is our finding of a significant *back-voltage* in these devices, which arises from the unintended scattering of electrons into waveguide ports that lie outside the intended path for current flow. This back-voltage should serve as a significant source of decoherence in these structures and therefore needs to be minimized if such structures are ever to find any useful application as a coherent qubit. Through careful configuration of the various gates that are used to implement the CEWs, however, we find that we are able to demonstrate the operation of a 'balanced qubit', in which these various structural complications are minimized. Based on these results, we believe that there may therefore be reason to hope that the proposed qubit operation of CEWs may be implemented in the future.

The remainder of this paper is organized as follows. In section 2, we describe the implementation of CEWs by the split-gate approach and clarify the different regimes of device operation. In section 3, we present the results of experiments that show the influence of structural asymmetry in these devices. This section features results that are an extension of our earlier reports [27, 28] and are included here for completeness of discussion. In section 4, we systematically investigate the influence of such asymmetry on the multi-port operation of these devices, showing the various behaviours that can arise when a high-resistance path is present on either the input or output side of the device. We conclude in section 5 by considering the further prospects for implementation of CEW qubits by this approach.

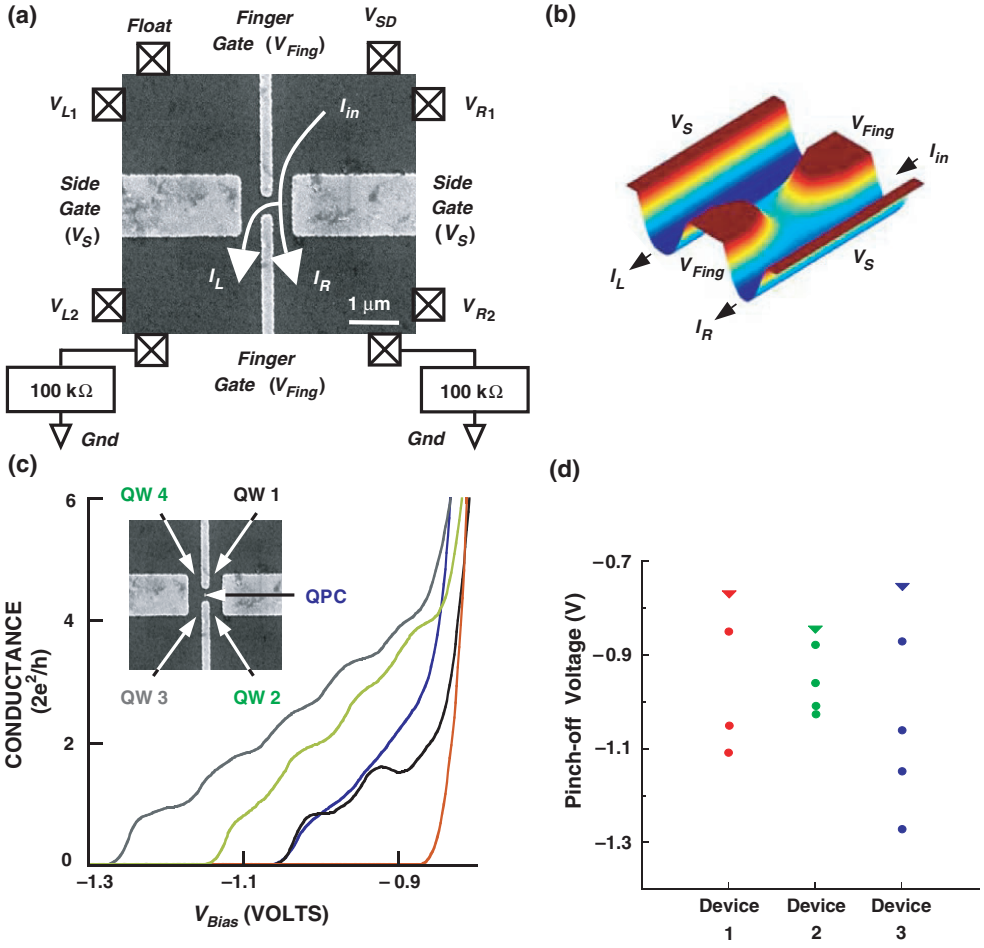

Figure 1. (a) Scanning electron micrograph of one of the CEW devices, showing current flow and voltage probes schematically. (b) Potential profile of the CEW device (modelling, see [33] for further details). (c) Conductance characterization of the individual QWs and the finger-gate QPC of device 3 at 40 mK. (d) Spread of pinch-off voltages of the various QWs ('●') and gate voltage to deplete the 2DEG under the gates ('▼') in three devices.

2. Split-gate implementation of CEWs

The CEWs that we have studied were implemented by the split-gate approach, in which Cr/Au gates, with fine-line patterns defined by electron-beam lithography, were deposited on a high-mobility GaAs/AlGaAs heterostructure (Sandia samples EA750 and EA739). The results presented here were obtained in studies of three nominally identical devices, which we refer to as devices 1, 2 and 3. (Other results from these devices have previously been presented in [27] (device 1) and [28] (devices 1 and 2).) A two-dimensional electron gas (2DEG) was located ∼200 nm below the heterostructure surface and, at 4.2 K, its carrier density and mobility were 2.7×10^{11} cm^{-2} and 4×10^6 cm^2 V^{-1} s^{-1}, respectively. The corresponding mean free path for electron transport was ∼35 μm, which is very much larger than the size of the device. An electron-microscope image of the CEW system is shown in figure 1(a), along with a measurement schematic relevant to the experiments reported here. The application of negative

voltage (V_S) to the 'side-gates' forms a wide QW that can then be divided to form a pair of coupled QWs by applying a negative bias (V_{Fing}) to the 'finger-gates'. With the gates thus configured, a small ac voltage (V_{SD}, chosen to ensure a current level of a few nanoamperes) is applied across the device and the currents (I_L and I_R) flowing to ground via its left- and right-hand side wires are measured. These measurements are made using low-frequency lock-in detection, with the sample mounted in either a variable-temperature insert or a Janis JDR-100 dilution refrigerator. A feature of the measurement configuration of figure 1(a) that we have not emphasized previously, but which will be shown to be critically important here, is the fact that the upper-left region of 2DEG is left floating in this experiment. Note that if a situation exists where the device scatters any charge into this region (which will actually be found to be the case in experiment), the potential drop ($V_{L_1} - V_{L_2}$) will be negative.

There have been many numerical studies of the switching characteristics of CEW qubits that have modelled these structures using a hard-walled potential, whose bottom is assumed to remain constant throughout the device (i.e. both in the two wires and in the coupling window). The experimental implementation of CEWs by the split-gate method, however, is expected to result in the formation of very different potential, consisting of a smooth saddle barrier in the coupling region that is connected continuously to soft-walled quantum wires, as shown in figure 1(b) [18, 29–33]. Variation of V_{Fing} in the experiment modulates the height of the barrier defined by the saddle point, and in previous experiment we have been able to identify two distinct regimes of operation, dependent on the position of this barrier relative to the Fermi level. In the *weak-coupling* regime, the saddle barrier lies above the Fermi energy (figure 2(c)), and we have found that the device operation is *dominated* by the properties of this barrier alone [27]. In the *strong-coupling* regime, in contrast, the barrier lies below the Fermi level (figure 2(b)) and there is significant wavefunction overlap between the wires. In [27], we showed that a study of the temperature dependence of the output currents (I_L and I_R) allows the transition between these two regimes and the variation in the barrier height (E_B in figure 2(c)) with V_{Fing} to be determined reliably.

3. Influence of structural asymmetry on switching in CEWs

The gate-voltage characteristics of the four different QWs, and of the quantum point contact (QPC) formed by the finger gates, are shown (colour coded) for device 3 in figure 1(c). The inset to this figure shows the labelling format of the four QWs that will be used in the discussion throughout this paper. Unlike our earlier studies [27, 28], which were all performed at a temperature of 4.2 K, the data shown here were obtained at a dilution-refrigerator temperature of 40 mK. The characteristics for QWs 1, 2 and 3 show well-established one-dimensional conductance quantization in units of $2e^2/h$ [29], providing a clear demonstration of the ballistic nature of transport. In the case of the QPC formed by finger gates, only the last conductance step is clearly seen, which suggests that this structure gives rise to weaker confinement than the longer QWs. The quantization is completely absent in the data for QW 4, and it pinches off at a much less negative gate voltage than the other regions of the device. We presume that this non-uniformity arises from the influence of microscopic fluctuations in the electron potential, due to the random distribution of ionized dopants in the heterostructure. From the perspective of implementing the CEW system, we note a potentially problematic issue arising from the very different pinch-off voltage for QW 4, i.e. especially under conditions where one is interested in configuring the QWs as single-mode structures, significant asymmetry should develop in the system. Indeed, the role of such asymmetry has been noted in previous implementations of CEWs in the literature [23, 24]. As we summarize in figure 1(d), asymmetry of the gate-voltage characteristics is found to be an issue in all devices that we have studied (in fact we believe that

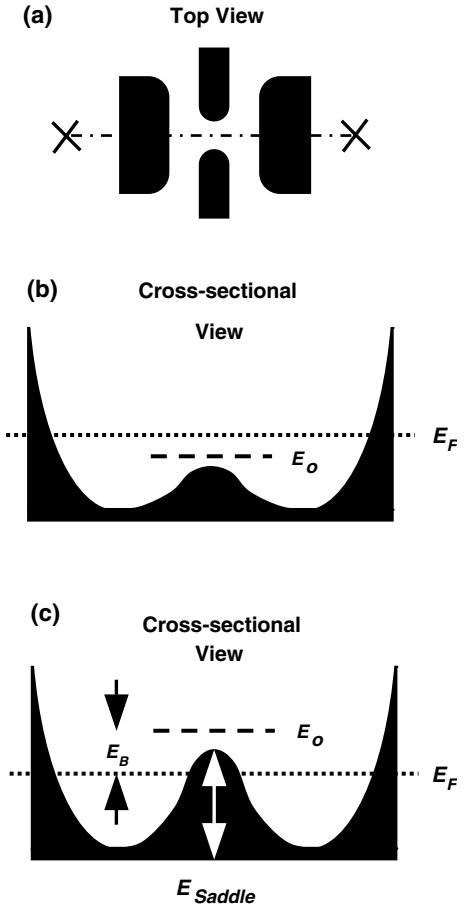

Figure 2. (a) Top view of CEW schematic showing cross-sectional plane. (b) and (c) Cross-sectional view of CEW in the strong- and weak-coupling regimes, respectively. E_B: energy barrier between the waveguides; E_o: first quantized energy level in saddle potential; E_F: Fermi energy.

such asymmetry is inevitable, since, due to the mesoscopic nature of these devices, there will always be one QW that pinches off first and therefore forms a bottleneck in the system). The voltage at which the 2DEG is first depleted *underneath* the gates is indicated for each device in this figure by the inverted triangle. In addition, the filled circles indicate the pinch-off voltage of each waveguide, thus this figure gives a comparative scale for the spread of pinch-off voltages of the waveguides.

In [28], the role of asymmetry was shown to contribute significantly to the switching characteristics exhibited by the CEWs as V_{Fing} and V_{S} were varied. We illustrate this in figure 3, where we show the results of measurements on device 1 at a temperature of 4.2 K. For low side-gate biases (figure 3(a)), the coupled waveguides are not yet fully formed and the device functions simply as a QPC that is formed by the finger gates. Increasing the side-gate bias, and hence forming the CEWs, reveals an interesting intermediate regime where the current characteristics show NOT-switching behaviour (figure 3(b)) [28]. In this effect, the current (I_{L}) flowing into the left wire actually increases as the coupling window is narrowed, and this effect becomes more pronounced as the side-gate conferment is increased by making V_{S} more

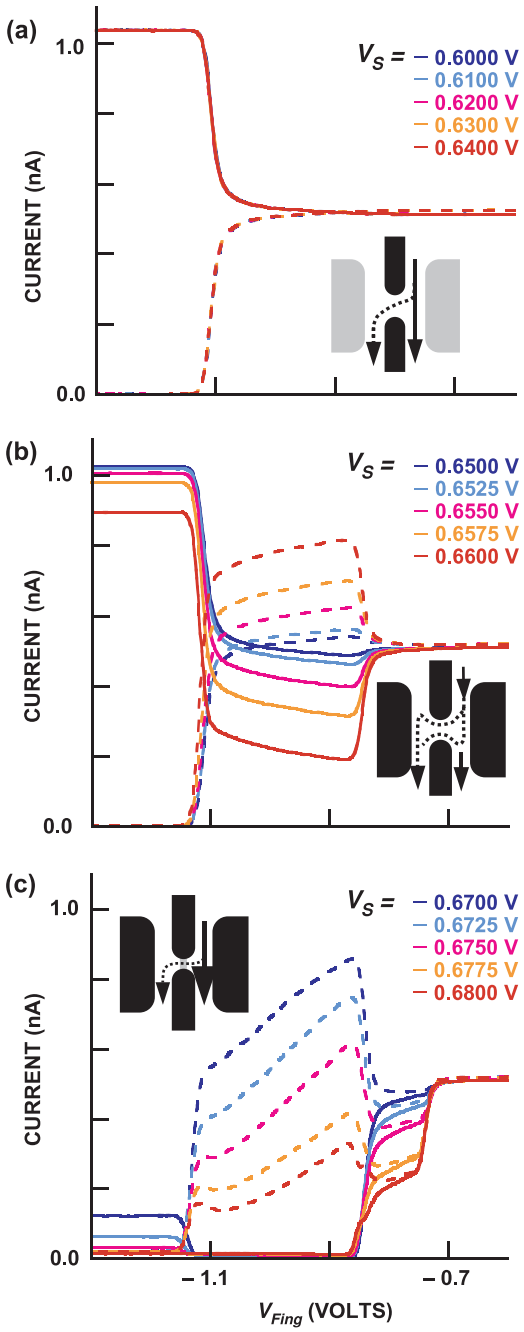

Figure 3. Experimentally obtained I_L (dotted line) and I_R (solid line) as a function of V_{Fing} at various V_S at 4.2 K: (a) low V_S, simple current splitting; (b) intermediate V_S, NOT- switching; (c) high V_S, asymmetric switching and current quenching. Results are for device 1.

negative (at least over the range shown in figure 3(a)). The NOT switching is observed only in the strong-coupling regime, which for this device [27, 28] ranges from $V_{Fing} \sim -0.85$ V, where the finger bias first forms the CEWs, to $V_{Fing} \sim -1.15$ V, where the QPC defined by the

finger gates completely pinches off. However on reversing the input and output terminals of the device, the NOT switching is no longer observed, indicating that it arises in large part from structural asymmetry in the device [28]. The magnitude of the NOT switching decreases with increasing temperature and is found to quench at temperatures beyond ∼20 K [28]. At higher temperatures than this, the variations in I_L and I_R exhibit a crossover, reverting to a form more reminiscent of that found in figure 3(a) [28]. While the precise mechanism responsible for the NOT behaviour remains undetermined, we have suggested that it may arise from the interplay of structural asymmetry and the onset of strong quantization in the waveguides [28].

It is clear from the behaviour in figures 3(a) and (b) that, for low and medium V_S, the total current $(I_L + I_R)$ remains roughly constant while I_L and I_R vary individually, indicating that the main effect of sweeping V_{Fing} under these conditions is to modulate the barrier in the coupling region without significantly modifying the potential of the waveguides. With a further increase in V_S, however, asymmetric current switching eventually develops, in which both I_L and I_R are quickly quenched as V_{Fing} is swept (figure 3(c)). In this situation, it is clear that the strong confinement generated by the side-gate bias modifies the geometry of the entire device (both the waveguides and the coupling window).

The presence of structural asymmetry in the CEWs has important implications for proposals to utilize them in multi-qubit networks [20, 21]. *Symmetric* waveguides are required for such applications, in which the idea is to connect *all four* QWs of each qubit to four other qubits in a multiply-connected network. Consequently, it is desirable to perform a comprehensive investigation of the switching characteristics of CEWs, studying the transport behaviour obtained in all four of their possible input configurations. Such an experiment should be very helpful, in particular for clarifying how the qubit switching is influenced by structural asymmetry. In the section that follows, we therefore describe the results of such a study for device 3.

4. Comprehensive study of switching in CEW system

Due to the *nominal* symmetry of the CEWs, their input and output QWs may be implemented in any one of four possible combinations, as indicated in figures 4(a) and (b), 6(a) and (b). In this section, we present the results of low-temperature (∼40 mK) measurements of device 3 in these different combinations. Our measurements are performed for the fairly typical situation that can arise in these structures, where the gate-biasing results in the formation of a current-limiting high resistance in one branch of the device. The preferred way to operate a CEW for qubit application would be to have both side-gates biased at the same voltage, thereby reducing the number of independent voltages needed to control the structure. Thus, in the following experiments, the side-gates are held at the same fixed voltage (V_S) and V_{Fing} is varied to control the inter-wire coupling. In contrast to our earlier studies [27, 28], where we measured only the currents flowing to the two output ports, in these experiments we also simultaneously measure the voltage drop that appears across the ends of the 'tunnelled-into' wire. In this way, we are able to obtain new information on the processes of electron injection into this wire.

4.1. Back-voltage as a source of decoherence

In figures 4(a) and (c), we show the measurement schematic and the corresponding current (I_L and I_R) and voltage ($V_{L_1} - V_{L_2}$) data obtained when QW 1 is used as the input terminal. In this device, the working range of the finger-gate voltage for strong waveguide coupling is $-1.05 < V_{Fing} < -0.9$ V. The higher negative bias is that for which the energy barrier in the coupling region rises above the Fermi level. The lower limit, as will be shown shortly,

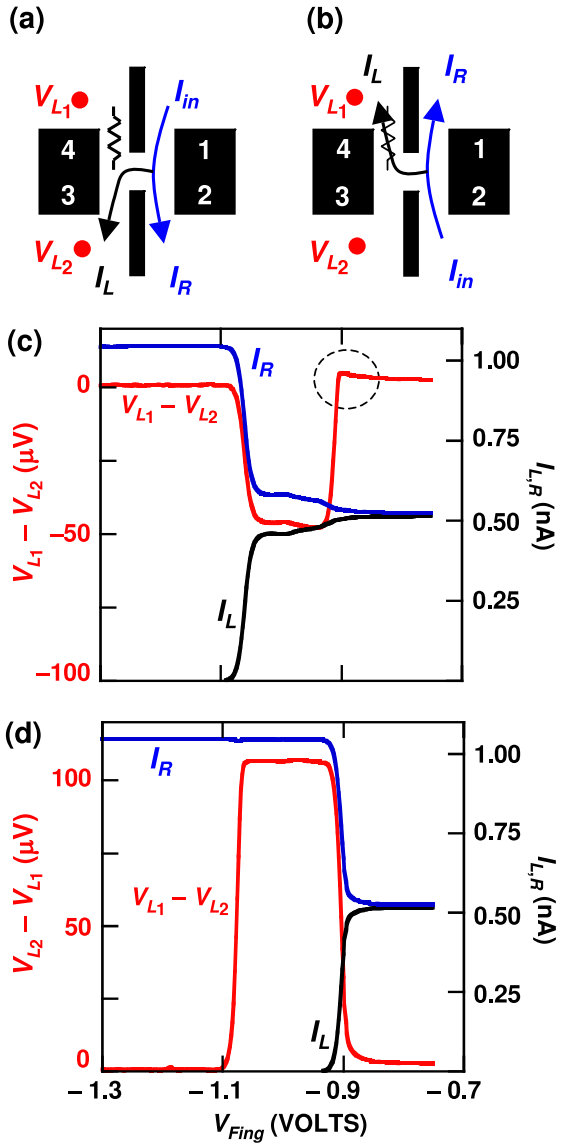

Figure 4. ((a) and (b)) Schematic of two schemes of qubit operation; $V_S = -0.92$ V and V_{Fing} is varied. Numbers 1–4 indicate the numbering scheme for the waveguides. ((c) and (d)) Voltage drop (orange) and output currents, I_L (black) and I_R (blue), at 40 mK for the schemes in (a) and (b), respectively. Device 3 at 40 mK.

corresponds to the point where QW 4 pinches-off. The interesting aspect of this measurement scheme is provided by the voltage data of figure 4(c), which develops a large negative value (∼95% of V_{SD}) over the working range of the device. In the discussion that follows, we refer to this voltage as the *back-voltage*, since it indicates the potential at which the floating terminal sits relative to ground. Typically, one might expect this voltage to have a small positive value, since the voltage is measured as ($V_{L_1} - V_{L_2}$) with the output side of QW 3 grounded and no net current drawn by QW 4. While the back-voltage is certainly close to zero in the range

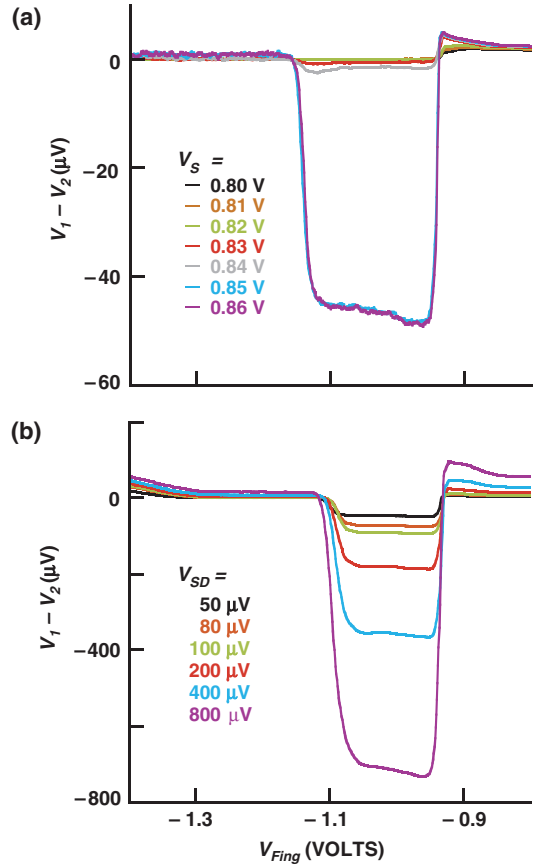

Figure 5. (a) V_S dependence of negative back-voltage, clearly showing its onset at $V_S \sim -0.85$ V. (b) Back-voltage at different source voltages (V_{SD}) with $V_S = -1.12$ V. Device 3 at 40 mK.

$-0.9 < V_{Fing} < -0.7$ V, there is a sudden reversal of its sign close to the point where QW 4 pinches off (indicated by the dashed circle in figure 4(c)). The connection between the pinch-off of QW 4 and the development of the negative back-voltage is established in figure 5(a), where we show voltage drop data over a range of side-gate biases. There is a marked shift in the voltage response at $V_S \sim -0.85$ V, which is close to the pinch-off voltage of QW 4 (~ -0.87 V in figure 1(c)). The negative sign of $V_{L_1} - V_{L_2}$ indicates that it is generated as a response to the unexpected injection of electrons into the floating region. We believe that the back-voltage arises from the tendency of the QPC formed by the finger gates to diffract electron waves as they pass through it [34, 35]. Over distances smaller than the mean free path, it is well known that this diffraction can inject electrons against the nominal direction of current flow. (This same collimation effect gives rise to the well-known ballistic-transport phenomena of bend resistance and quenching of the Hall effect [29].) In the case of the CEW system here, and in order to preserve overall current conservation, the back-voltage must then develop to ensure that any electrons driving into the floating probe are then ultimately returned to the current ground. The behaviour of the back-voltage found here is consistent with the simulations reported in [33], where the introduction of a saddle barrier in the coupling region of the CEWs was found to result in the development of a small wavefunction amplitude in

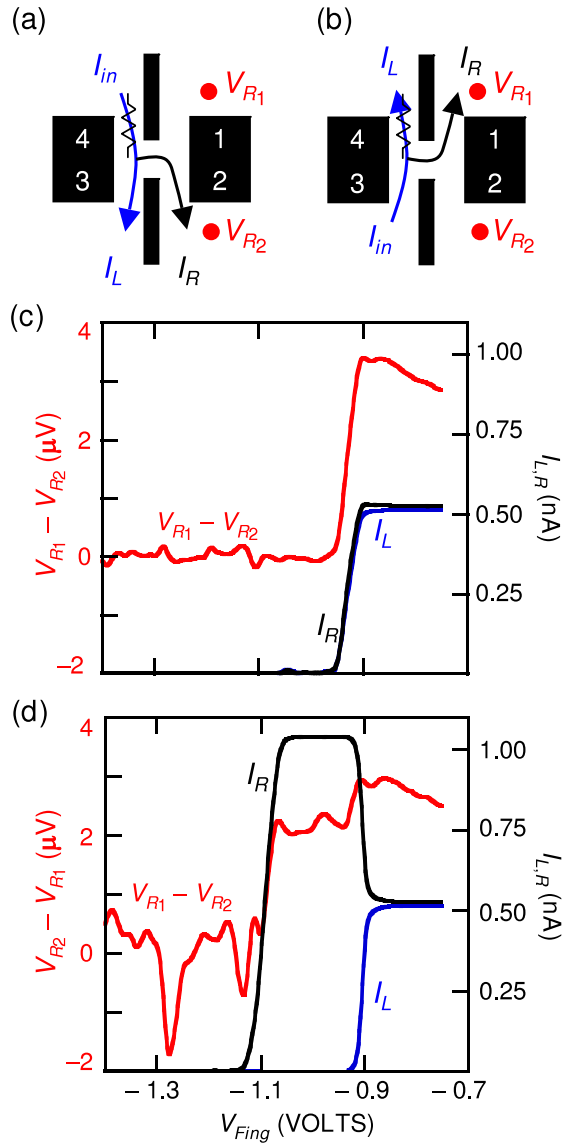

Figure 6. ((a) and (b)) Schematic of two schemes of qubit operation; $V_S = -0.92$ V and V_{Fing} is varied. Numbers 1–4 indicate the numbering scheme for the waveguides. ((c) and (d)) Voltage drop (orange) and output currents, I_L (black) and I_R (blue), for the schemes in (a) and (b), respectively. Device 3 at 40 mK.

the wire where no electron activity is expected. The magnitude of this back-voltage has been investigated in an additional set of experiments, in which the source voltage applied across the device was varied. The results of this experiment (figure 5(b)) verify that the back-voltage reaches an upper limiting value close to V_{SD}. This does not seem unreasonable, however, since the back-voltage develops when electrons are directed into a region with very high resistance ($\sim$10 MΩ, limited by the input impedance of the lock-ins).

The unintended scattering of electrons into the floating region, and the development of the back-voltage, have critical implications for the application of CEWs to quantum computing.

As discussed by Büttiker and others [36], the electrons injected into this reservoir will be thermalized to its electrochemical potential, thereby losing their initial phase information before being re-injected back into the device. Since coherent propagation of electrons is one of the prerequisites of the waveguide scheme for quantum computing [15–21], the appearance of the back-voltage is therefore problematic. In the case where the back-voltage approaches the source–drain voltage, as is the case in figure 5, the influence of this dephasing should be particularly pronounced.

In figure 4(b) we illustrate schematically the situation where the direction of current direction is reversed and QW 4 now forms one of the output waveguides. The results of experimental measurements in this geometry are shown in figure 4(d). The working range of V_{Fing} is the same as in figure 4(c), but the responses are very different. As QW 4 develops a high resistance at $V_{\mathrm{Fing}} \sim -0.87$ V, a simple splitting of the current (shown in blue and red) is obtained. This is accompanied by the development of a *positive* back-voltage, whose maximal value corresponds to $\sim 2V_{\mathrm{SD}}$. In contrast to the negative value found earlier, this back-voltage can be attributed to an instrumental effect. When a high-resistance path develops in QW 4, it cuts off one of the 100 kΩ current-measuring resistors (see figure 1(a)), and the constant-current circuit at the input wire sees only one 100 kΩ resistor. The resistance to ground on the output side of the device therefore doubles from 50 to 100 kΩ, resulting in an associated doubling of the input voltage (from 50 to 100 μV). Under such conditions, the coupling region, QW 2 and QW 3, are all open, thus V_{L_2} reads this increased source voltage, which shows up as a voltage drop across the 'tunnelled-into' wire. Finally, at a $V_{\mathrm{Fing}} \sim -1.1$ V, the coupling region is pinched-off and $V_{\mathrm{L}_2} \sim 0$ V, as shown in figure 4(d).

4.2. Tunnelling spectroscopy of 1D density of states

Further interesting behaviour is found in the situation where the roles of the left- and right-hand sides of the device are reversed, and QW 4 is chosen as the input wire (figure 6(a)). In this case, the total current drops from the expected value of ∼1 nA to an almost negligible value at $V_{\mathrm{Fing}} \sim -0.9$ V (figure 6(c)) as the input pinches off. While no further useful information can be obtained for the currents once this occurs, interesting behaviour is found instead in the back-voltage. For a further increase in V_{Fing}, the back-voltage exhibits reproducible oscillations, with an average value of zero (red curve in figure 6(c)). These oscillations measure the voltage drop arising from the tunnelling of current into the two output wires. For example, when all of the tunnel current is injected into QW 3, the back-voltage (in this case $V_{\mathrm{R}_1} - V_{\mathrm{R}_2}$) should be equal to zero. A non-zero back-voltage, on the other hand, indicates that at least a fraction of the current that tunnels through QW 4 enters the right output wire. When this back-voltage is negative, this tunnelling should involve the scattering of electrons into the back probe (QW 1). The fact that the magnitude of the voltage oscillations in this case is small (much less than $V_{\mathrm{SD}} = 50$ μV) is presumably due to the fact that V_{SD} is dropped largely across (the high-resistance) QW 4.

To further address the origins of the back-voltage oscillations in figure 6(c), it is helpful to consider the results of measurements performed in the last possible current injection scheme, which is shown schematically in figure 6(b). In this configuration, the resulting current response (figure 6(d)) can be explained by the fact that, when QW 4 pinches-off for $V_{\mathrm{Fing}} \sim -0.9$ V, all of the current is directed into QW 1. At $V_{\mathrm{Fing}} \sim -1.1$ V, the barrier in the coupling region rises above the Fermi level and reduces I_{R} to a negligible value. Within the range $-1.1 < V_{\mathrm{Fing}} < -0.9$ V, there are small, but reproducible, fluctuations in the voltage data $(V_{\mathrm{R}_2} - V_{\mathrm{R}_1})$. These grow significantly in amplitude for $V_{\mathrm{Fing}} < -1.1$ V, in which the output through the left wire is essentially completely shut down and the only path for current flow is through the output of the right wire. In order for this flow to occur, however, electrons

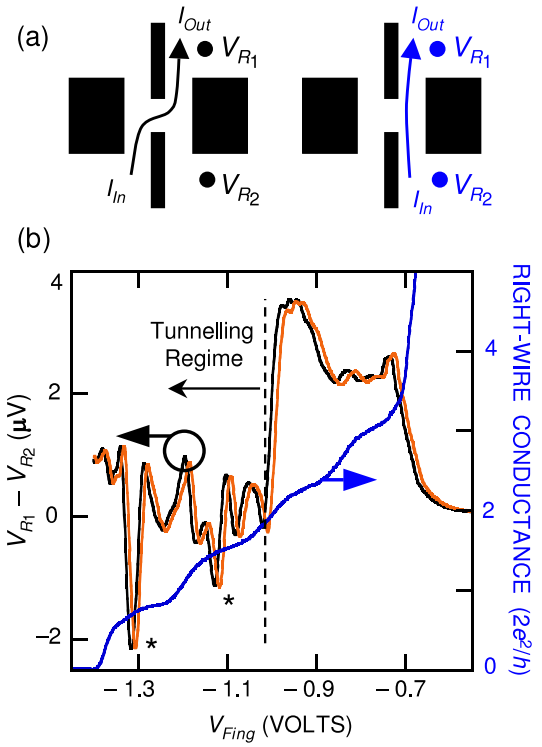

Figure 7. (a) Schematic of voltage drop (left figure) and conductance (right figure) measurement. (b) Voltage drop (black and light grey curves indicate up and down sweeps of V_{Fing}) across output QW as V_{Fing} is varied with $V_{\mathrm{S}} = -0.94$ V. The blue curve represents the conductance of the output QW. The dashed line indicates commencement of the tunnelling regime for the coupling region. Device 3 at 40 mK.

must tunnel through the coupling region (which is also close to pinch off). To confirm these ideas, a simpler experiment, using the arrangement shown in figure 7(a), may be performed. The scheme shown on the left of this figure is used to measure the voltage drop across the 'tunnelled-into' wire, as current is injected into it, while that on the right is used to measure the conductance of this wire itself. When the results of these two measurements are plotted together (figure 7(b)), it is seen, in the tunnelling regime (indicated by the dashed line), that the major dips in the voltage data (indicated by the asterisks in figure 7(b)) are correlated to the situation where the conductance is rising towards one of its quantized plateaus. Such behaviour is relatively straightforward to understand. As successive plateaus are being approached, new one-dimensional subbands are being populated and each of these should be characterized by a strongly enhanced density of states at its subband edge. The data of figures 6(d) and 7 therefore show that the CEW system can be configured to serve as a density of states spectrometer [22]. While the use of this technique will be described in detail in a future publication [37], we find that the voltage oscillations wash out at a temperature of a few Kelvin, consistent with a quantum effect related to the one-dimensional density of states. An interesting aspect of figure 7 is the presence of smaller oscillations in the back-voltage that are *not* correlated to the 1D subband events. These features, too, wash out quickly with increasing temperature and are presumably related to quantum interference that is established by the injection of electrons into the right wire.

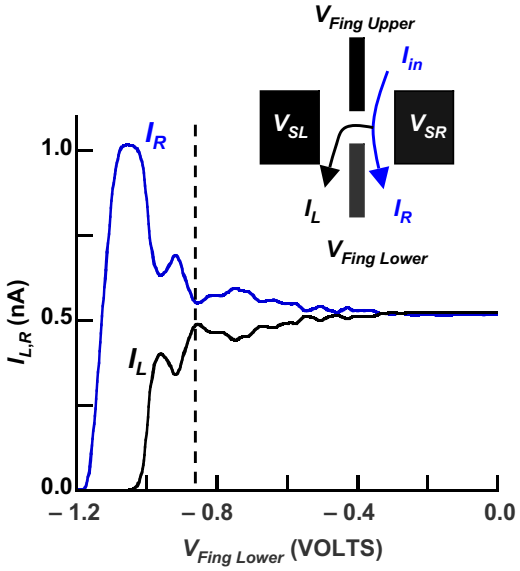

Figure 8. Inset: balanced-qubit schematic; $V_{\mathrm{SL}} = -1.09$ V, $V_{\mathrm{SR}} = -1.43$ V, $V_{\mathrm{Fing\ Lower}} = -1.05$ V, and $V_{\mathrm{Fing\ Upper}}$ is varied. Main plot: output currents, I_{L} (black) and I_{R} (blue). The dashed vertical line represents commencement of the quantization of input QW. Device 3 at 40 mK.

4.3. The balanced qubit

The discussion above has shown that the application of a common bias to the side-gates tends to result in the formation of an asymmetric structure, with a high resistance developing in at least one branch of the device as the side-gate confinement is increased. In an attempt to implement a symmetric waveguide system, such as that considered in the theoretical proposals of [15–21], we have therefore applied different biases to the side-gates in an attempt to realize waveguides with similar conductance (close to $2e^2/h$). The inset to figure 8 shows the schematic of this 'balanced-qubit' experiment, in which the side-gates are biased at different voltages. In addition, to ensure that the output QWs maintain as constant a conductance as possible, the lower finger-gate is held at -1.05 V (the pinch-off voltage of the finger-gates when commonly biased) and only the upper finger-gate bias is swept. The results of such an experiment are plotted in figure 8, and now show interesting complementary oscillations in almost the entire range of operation. The oscillations actually consist of two distinct sets, one of which has higher amplitude and evolves abruptly from smaller oscillations at $V_{\mathrm{Fing\ Upper}} \sim -0.85$ V (the dashed line in figure 8). The smaller oscillations occur in the range where the 2DEG remains beneath the upper finger-gate. The oscillations therefore presumably arise from a change in quantum interference that is caused by the resulting variation in the electron density under this gate.

The most interesting region of figure 8 lies in the range $-1.05 < V_{\mathrm{Fing\ Upper}} < -0.85$ V. At the most negative end of this range, the current behaviour is similar to that exhibited in figure 3(a) due to the pinch-off of the coupling window. As the finger-bias is swept even further, both currents drop to zero beyond $V_{\mathrm{Fing\ Upper}} \sim -1.1$ V, indicating the total pinch-off of all current paths. At the other end of the finger-voltage range ($V_{\mathrm{Fing\ Upper}} \sim -0.85$ V), however, we note that the value of this gate voltage also corresponds to that at which QW 1 starts to show quantized behaviour in its conductance (see figure 1(c)). Thus one can correlate

the sudden increase in the amplitude of the current oscillations in the balanced system to the onset of one-dimensional quantization in the input waveguide. Oscillations similar to those shown in figure 8 have not been seen in any of our previous experiments, performed on either unbalanced structures or in the balanced system at higher temperatures (∼4.2 K). We therefore conclude that they are a manifestation of quantum interference in highly symmetric coupled waveguides.

5. Conclusions

In this report, we have presented the results of detailed investigations of the switching characteristics of CEWs realized by the split-gate method. These investigations have been undertaken from the perspective of assessing the suitability of such structures to a proposed scheme for electron-wave qubit realization [15–21]. Our studies have revealed that a variety of behaviours can be observed in these structures, with the switching being strongly influenced by structural asymmetry. Such asymmetry arises quite naturally in split-gate nanostructures, in which microscopic variations in the local doping profile can lead to significantly different pinch-off voltages for nominally identical gates. When this asymmetry gives rise to a high resistance in the 'tunnelled-into' waveguide, we have seen that a large back-voltage can develop across this wire, which is indicative of the unintended scattering of electrons into waveguide ports outside of the current path. This back-voltage should serve as a significant source of decoherence, which would be particularly detrimental to the operation of multiply-connected CEW-qubit networks. In the theoretical proposals for such networks [20, 21], the qubits have been assumed to have symmetric waveguides. Hence, the role of structural asymmetry, and associated decoherence, needs to be minimized if CEWs are ever to find any useful application as a coherent qubit. By careful tuning of the biases applied to the different gates of the device, we have found, however, that a 'balanced-qubit' can be realized, in which the unwanted back reflection can be minimized and symmetric characteristics can be obtained. Although the balanced-qubit is a complicated approach to its operation, it would form an excellent tool to investigate the underlying dynamics of the coupled waveguide system. We intend to focus on such implementations in future explorations of this scheme.

Acknowledgments

This work was sponsored by the US Department of Energy (DE-FG03-01ER45920) and NYSTAR (Faculty Development Program). This work was performed, in part, at the Center for Integrated Nanotechnologies, whhich is a Department of Energy (DOE) Office of Basic Energy Sciences nanoscale science research centre. Sandia National Laboratories is a multi-program laboratory operated by Sandia Corporation, a Lockheed-Martin Company, for the DOE under contract no. DE-AC04-94AL85000.

References

[1] Nakamura Y, Pashkin Yu A and Tsai J S 1999 *Nature* **398** 786
[2] Martinis J M, Nam S, Aumentado J and Urbina C 2002 *Phys. Rev. Lett.* **89** 117901
[3] Vion D, Aassime A, Cottet A, Joyez P, Pothier H, Urbina C, Esteve D and Devoret M H 2002 *Science* **296** 886
[4] Pashkin Yu A, Yamamoto T, Astafiev O, Nakamura Y, Averin D V and Tsai J S 2003 *Nature* **421** 823
[5] Yamamoto T, Pashkin Yu A, Astafiev O, Nakamura Y and Tsai J S 2003 *Nature* **425** 941
[6] Chiorescu I, Nakamura Y, Harmans C J P M and Mooij J E 2003 *Science* **299** 1869
[7] McDermott R, Simmonds R W, Steffen M, Cooper K B, Cicak K, Osborn K D, Oh S, Pappas D P and Martinis J M 2005 *Science* **307** 1299

[8] Kane B E 1998 *Nature* **393** 133
[9] Burkard G and Loss D 2002 *Semiconductor Spintronics and Quantum Computation* ed D D Awschalom, D Loss and N Samarth (Berlin: Springer) p 229
[10] Furuta S, Barnes C H W and Doran C J L 2004 *Phys. Rev.* B **70** 205320
[11] Jelezko F, Gaebel T, Popa I, Gruber A and Wrachtrup J 2004 *Phys. Rev. Lett.* **92** 076401
[12] Elzerman J M, Hanson R, Willems van Beveren L H, Witkamp B, Vandersypen L M K and Kouwenhoven L P 2004 *Nature* **430** 431
[13] Petta J R, Johnson A C, Taylor J M, Laird E A, Yacoby A, Lukin M D, Marcus C M, Hanson M P and Gossard A C 2005 *Science* **309** 2180
[14] Koppens F H L, Buizert C, Tielrooij K J, Vink I T, Nowak K C, Meunier T, Kouwenhoven L P and Vandersypen L M K 2006 *Nature* **442** 766
[15] Bertoni A, Bordone P, Brunetti R, Jacoboni C and Reggiani S 2000 *Phys. Rev. Lett.* **84** 5912
[16] Ionicioiu R, Amaratunga G and Udrea F 2001 *Int. J. Mod. Phys.* B **15** 125
[17] Bertoni A, Bordone P, Brunetti R and Jacoboni C 2002 *J. Mod. Opt.* **49** 1219
[18] Marchi A, Bertoni A, Reggiani S and Rudan M 2003 *IEEE Trans. Nanotechnol.* **3** 129
[19] Harris J, Akis R and Ferry D K 2001 *Appl. Phys. Lett.* **79** 2214
[20] Snyder M G and Reichl L E 2004 *Phys. Rev.* A **70** 052330
[21] Akguc G B, Reichl L E, Shaji A and Snyder M G 2004 *Phys. Rev.* A **69** 042303
[22] Eugster C C and del Alamo J A 1991 *Phys. Rev. Lett.* **67** 3586
[23] Hirayama Y, Wieck A D, Bever T, von Klitzing K and Ploog K 1992 *Phys. Rev.* B **46** 4035
[24] Pingue P, Piazza V, Beltram F, Farrer I, Ritchie D A and Pepper M 2005 *Appl. Phys. Lett.* **86** 052102
[25] Bielejec E, Seamons J A, Reno J L and Lilly M P 2005 *Appl. Phys. Lett.* **86** 083101
[26] Fischer S F, Apetrii G, Kunze U, Schuh D and Abstreiter G 2006 *Nat. Phys.* **2** 91
[27] Ramamoorthy A, Bird J P and Reno J L 2006 *Appl. Phys. Lett.* **89** 013118
[28] Ramamoorthy A, Bird J P and Reno J L 2006 *Appl. Phys. Lett.* **89** 153128
[29] van Houten H, Beenakker C W J and van Wees B J 1992 *Semiconductors and Semimetals* ed M A Reed (New York: Academic) pp 9–112
[30] Büttiker M 1992 *Semiconductors and Semimetals* ed M A Reed (New York: Academic) pp 191–277
[31] Ando T 1991 *Phys. Rev.* B **44** 8017
[32] Timp G 1992 *Semiconductors and Semimetals* ed M A Reed (New York: Academic) pp 113–90
[33] Ramamoorthy A, Akis R and Bird J P 2006 *IEEE Trans. Nanotechnol.* **5** 712
[34] Akis R, Ferry D K and Bird J P 1996 *Phys. Rev.* B **54** 17705
[35] Bird J P, Ishibashi K, Aoyagi Y, Sugano T, Akis R, Ferry D K, Pivin D M, Connolly K M, Taylor R P, Newbury R, Olatona D M, Ochiai Y and Okubo Y 1997 *Chaos Solitons Fractals* **8** 1299
[36] Büttiker M 1986 *Phys. Rev.* B **33** 3020
[37] Ramamoorthy A, Mourokh L, Reno J L and Bird J P 2007 in preparation