KING ABDULAZIZ UNIVERSITY

THE COLLEGE OF ENGINEERING

Digital Design II

EE460 – Winter 2023

Design Assignment #5

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Saturday, February 11, 2023

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Introduction

In this design assignment, we were tasked to design a digital system that implements an algorithm that takes input **x** and compare it with an array **a** of size 256. While counting the frequency that x is not found within the array.

Top Level Design

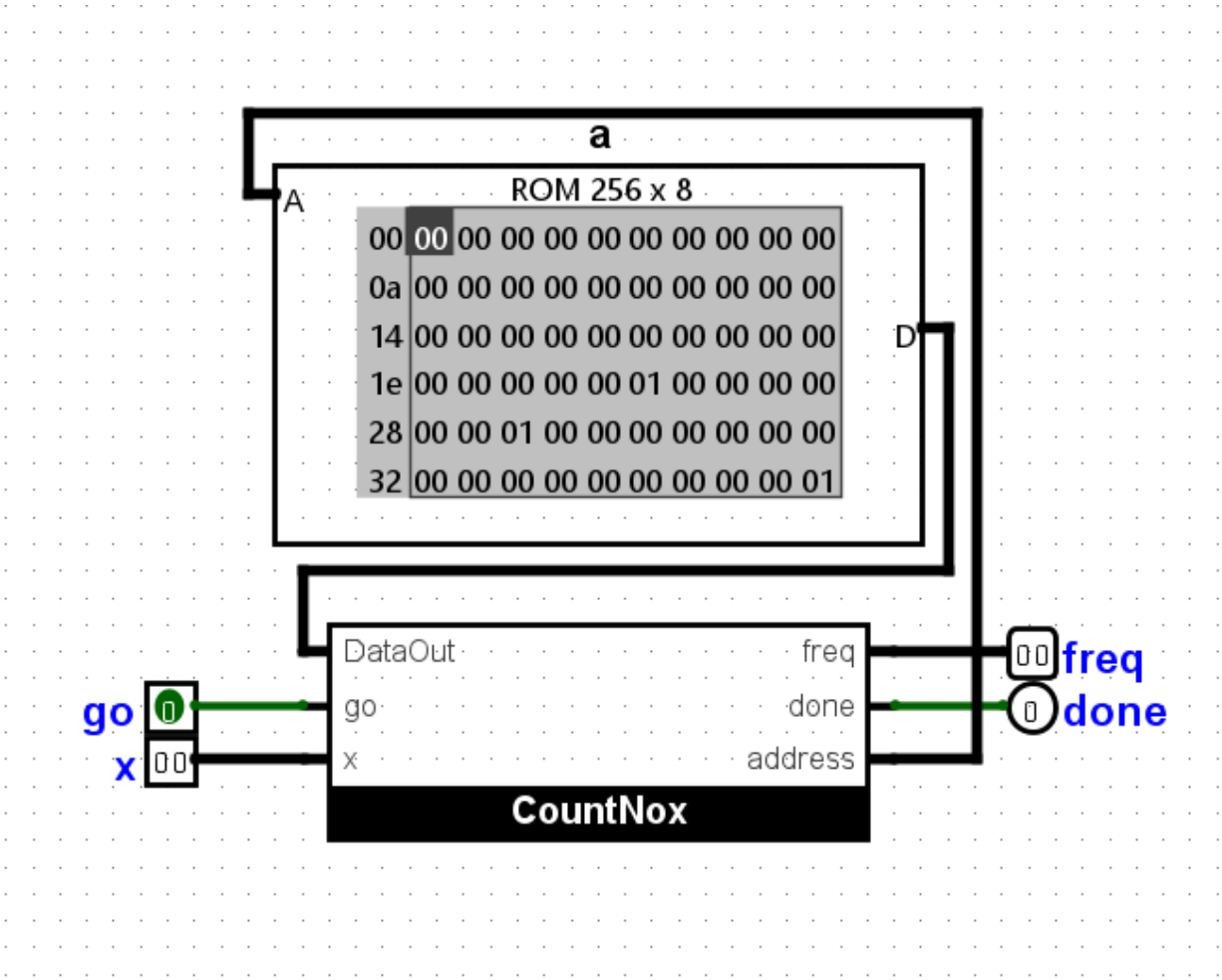


Figure 1 Top Level Design

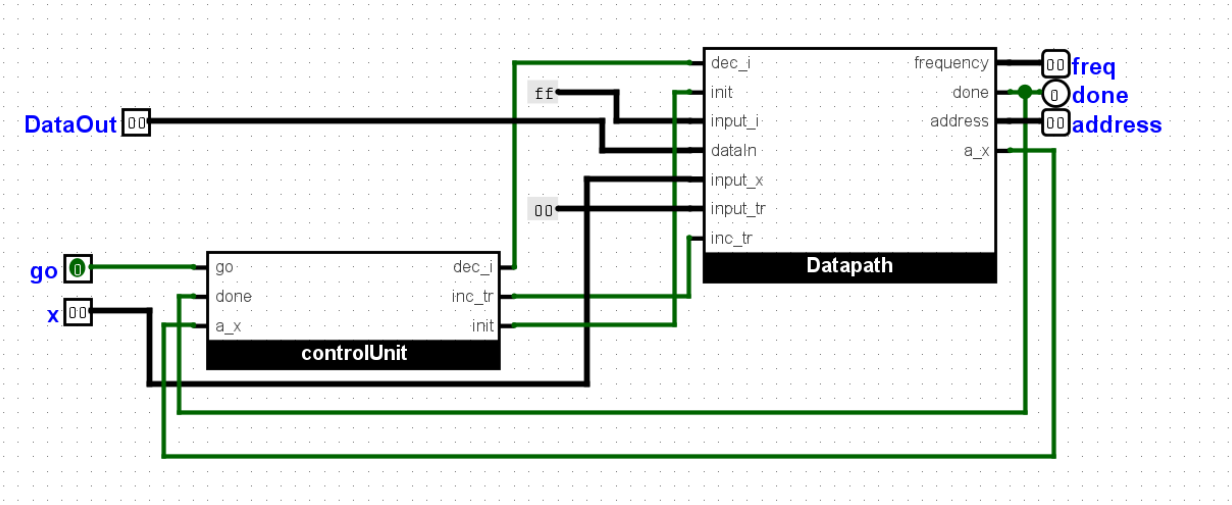


Figure 2 Control unit and Datapath interconnections

Datapath

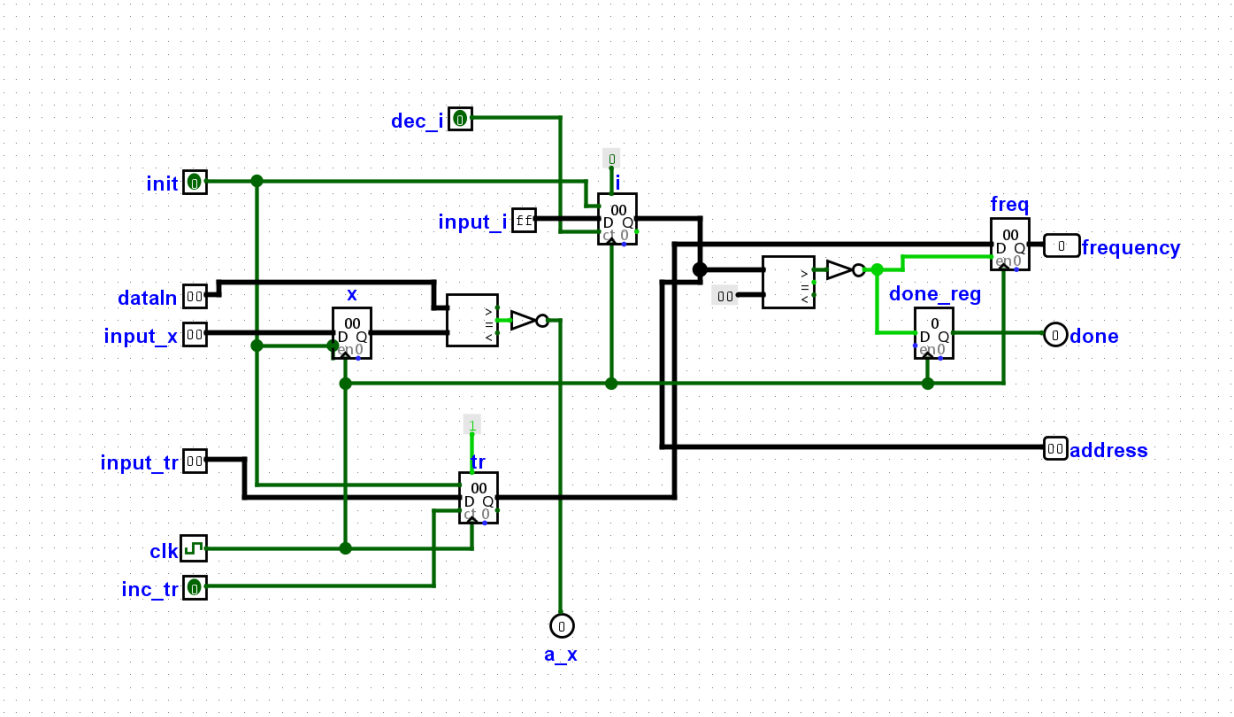


Figure 3 Datapath

Control Unit

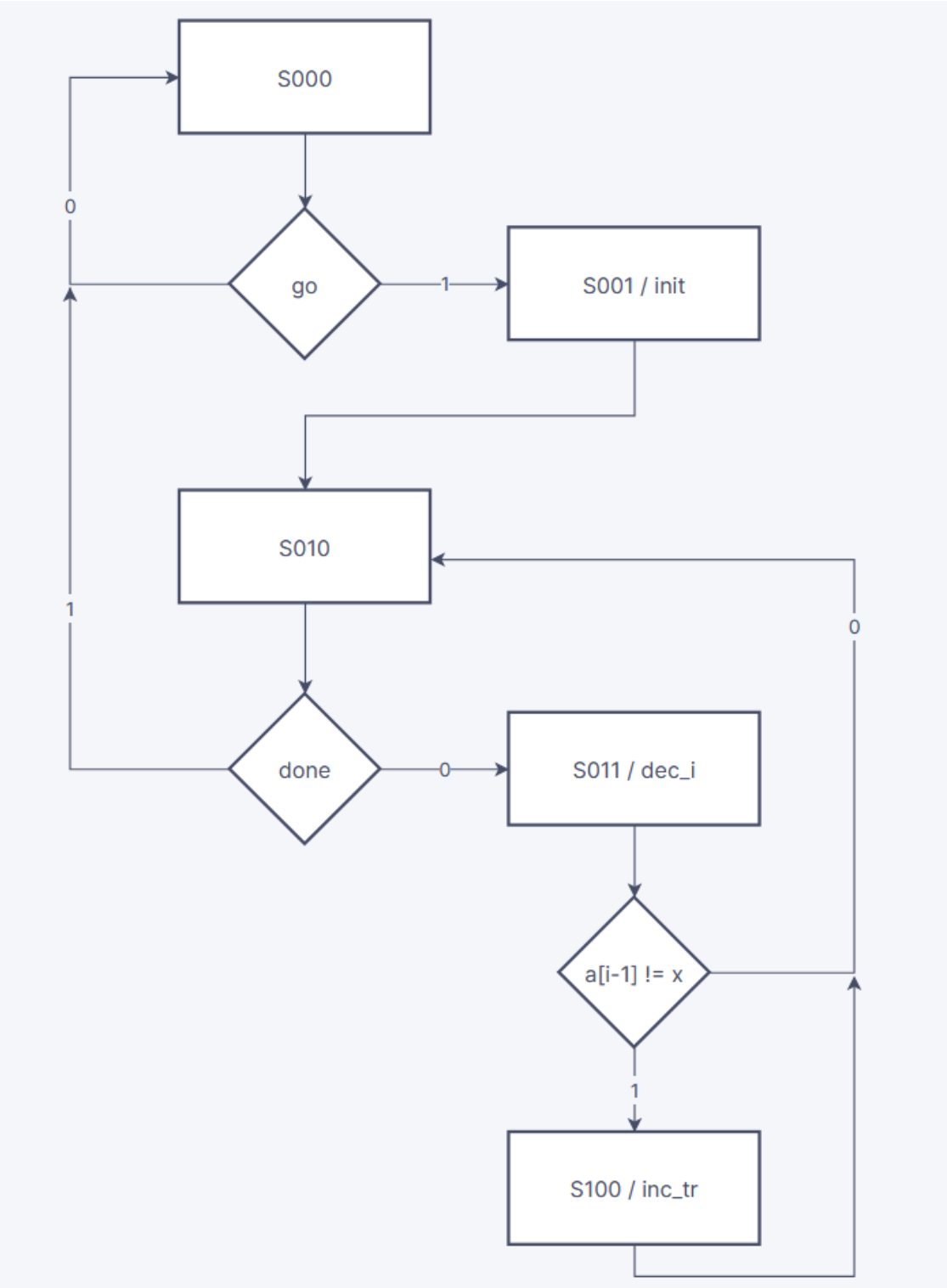
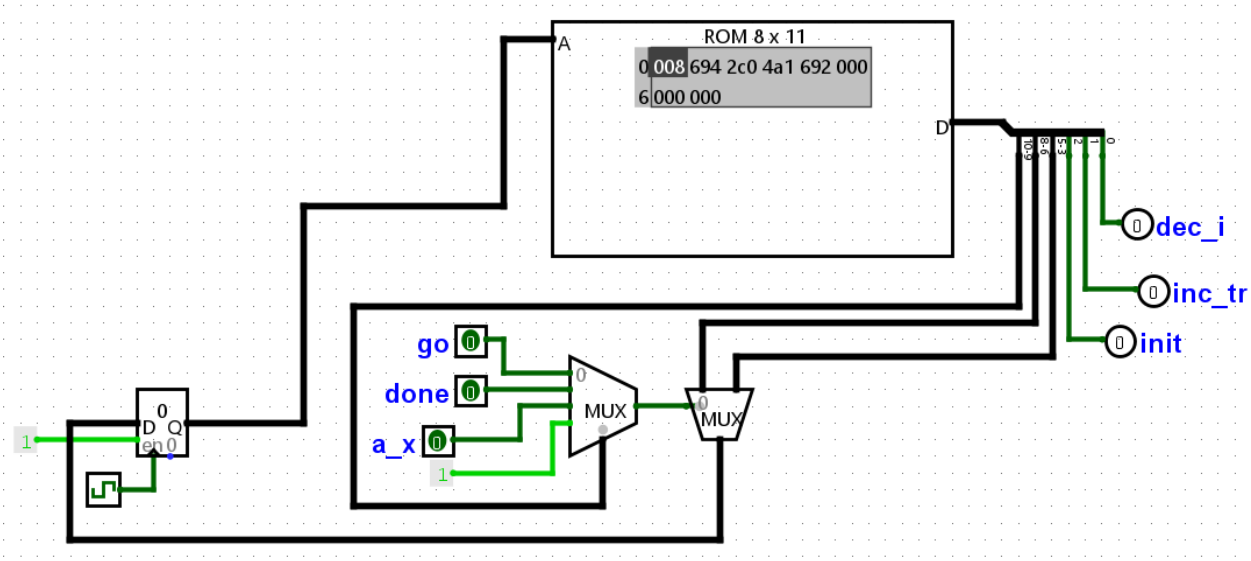


Figure 4 ASM for Two-address Microcode



State	TEST	NSF	NST	init	Inc_tr	dec_i	Hex
000	00	000	001	0	0	0	008
001	11	010	010	1	0	0	694
010	01	011	000	0	0	0	2C0
011	10	010	100	0	0	1	4A1
100	11	010	010	0	1	0	692

In this design Logisim was used to visualize the Datapath and simulate how the design will operate. Based on that the Verilog code was written. The control unit used is a Two address microcode control unit. Using ROM and multiplexers.

In the test bench simulation, we checked how many times x=1b’0 was not repeated, while array a is all zeros expect for 7 different addresses. The test bench simulation confirmed that there is 7 addresses were x didn’t equal a[i-1];