ACT: **A**rchitectural **C**arbon Modeling **T**ools

@ MICRO 2024
Tutorial

CORNELL TECH

Leo Han
Udit Gupta

ACT Tutorial: Today

Time	Topic
1:00 – 1:15pm	Welcome to the ACT tutorial!
1:15 – 1:30pm	Motivation: Understanding the source of computing’s emissions
1:30 – 2:15pm	**Overview of ACT: An Architectural Carbon Modeling Tool**
2:15 –2:45pm	Hands-on ACT demo’s
2:45 – 3:00pm	Extending ACT
3:00 – 3:30pm	Coffee break

Tackling computing’s carbon footprint requires optimizing emissions across ***hardware life cycles*** (manufacturing and operational use)

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But (unlike performance, power, energy) there is a distinct lack of architectural tools and infrastructure to quantify carbon

Challenge: How do we design sustainable systems by considering the footprint across lifecycles

This work: Architectural Carbon Modeling Tools (ACT)

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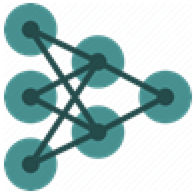
Architectural Carbon Modeling Tools (ACT)

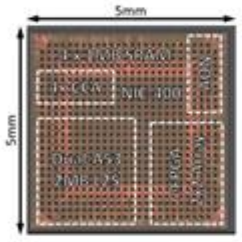
Arch. Carbon **Model**

Carbon–aware HW **design metrics**

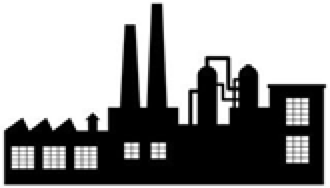
Architectural Carbon Modeling Tools (ACT)



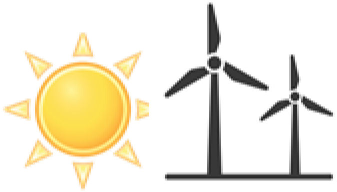
SW design & performance



HW design & power



Fab



Environmental

Arch. Carbon **Model**

Carbon–aware HW **design metrics**

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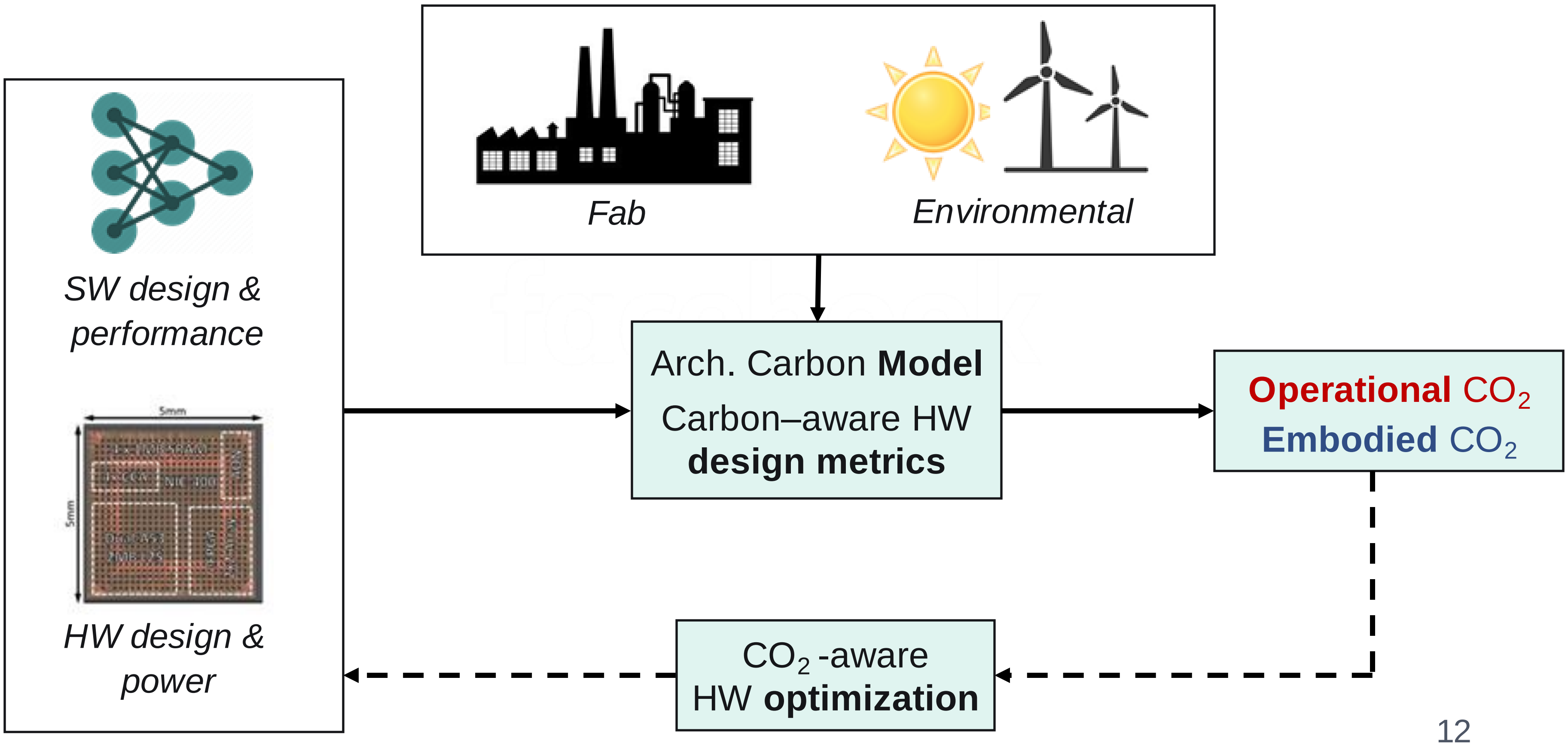

Architectural Carbon Model

Model	Hardware/software input

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$OP_{CF} = CI_{use} \times Energy$	**Energy efficiency** and environment (**carbon intensity**)

Architectural Carbon Model

Model	Hardware/software input
$Carbon = OP_{CF} + \frac{Runtime}{Lifetime} Emb_{CF}$	**Performance/power/energy** and **lifetime** of hardware
$OP_{CF} = CI_{use} \times Energy$	**Energy efficiency** and environment (**carbon intensity**)
$Emb_{CF} = Packaging + \sum_{r}^{SoC,Memory,Storage} Emb_r$	Overhead of **hardware manufacturing**

Embodied carbon of application processors (SoC’s)

$$Emb_{soc} = Area \times \frac{\left(CI_{fab} \times Fab_{energy}\right) + Fab_{gasses} + Fab_{materials}}{Yield}$$

Embodied carbon of application processors (SoC's)

Energy source (grid)

Device and fab characterization (industry fabs, device data)

$$Emb_{soc} = \color{darkred}{Area} \times \frac{\left(CI_{fab} \times Fab_{energy}\right) + Fab_{gasses} + Fab_{materials}}{Yield}$$

Hardware design

Embodied carbon of application processors (SoC's)

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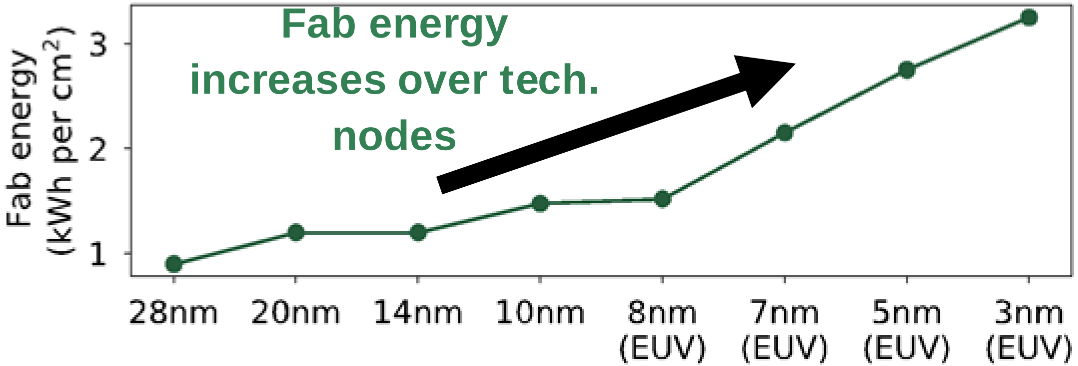

DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies. Bardon et. al (IEDM 2020)

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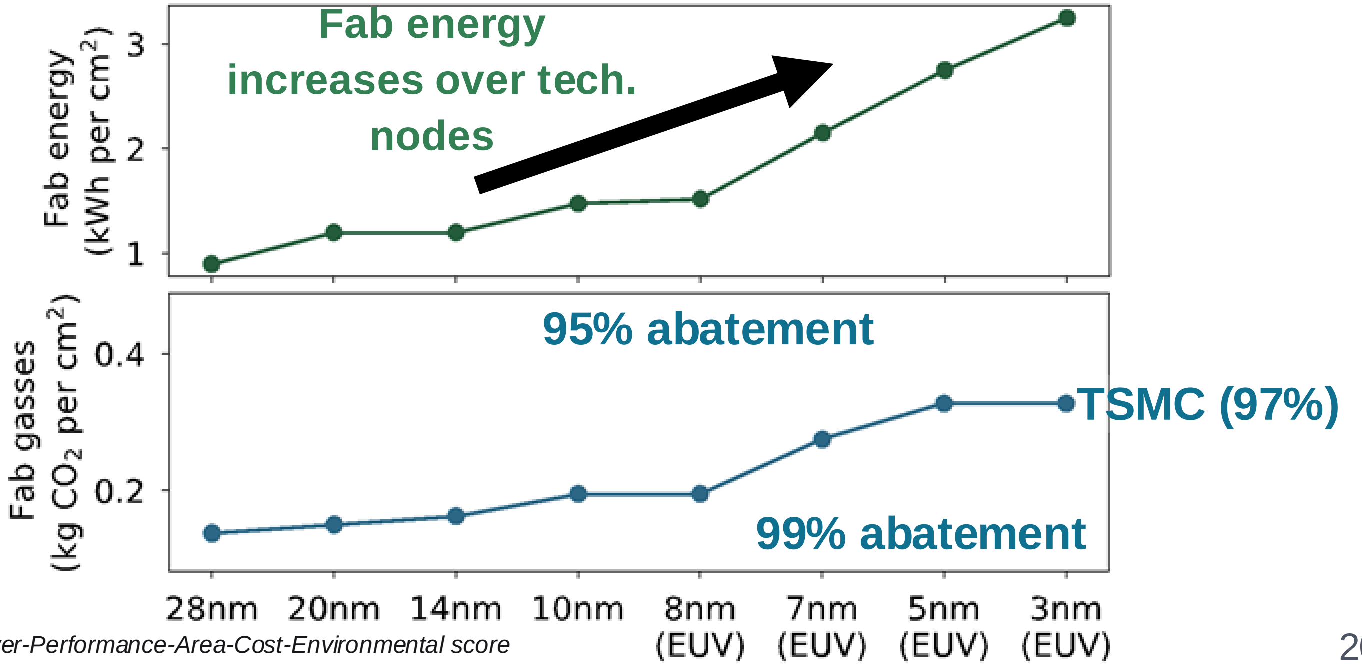

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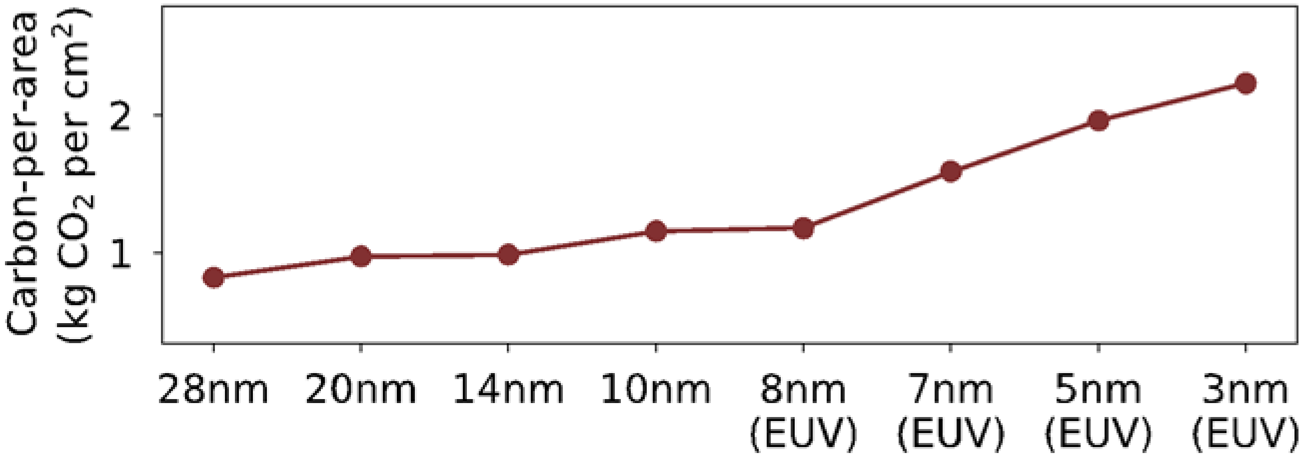

Data sources:

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- *[TSMC] TSMC Sustainability Reports 2018-2020*

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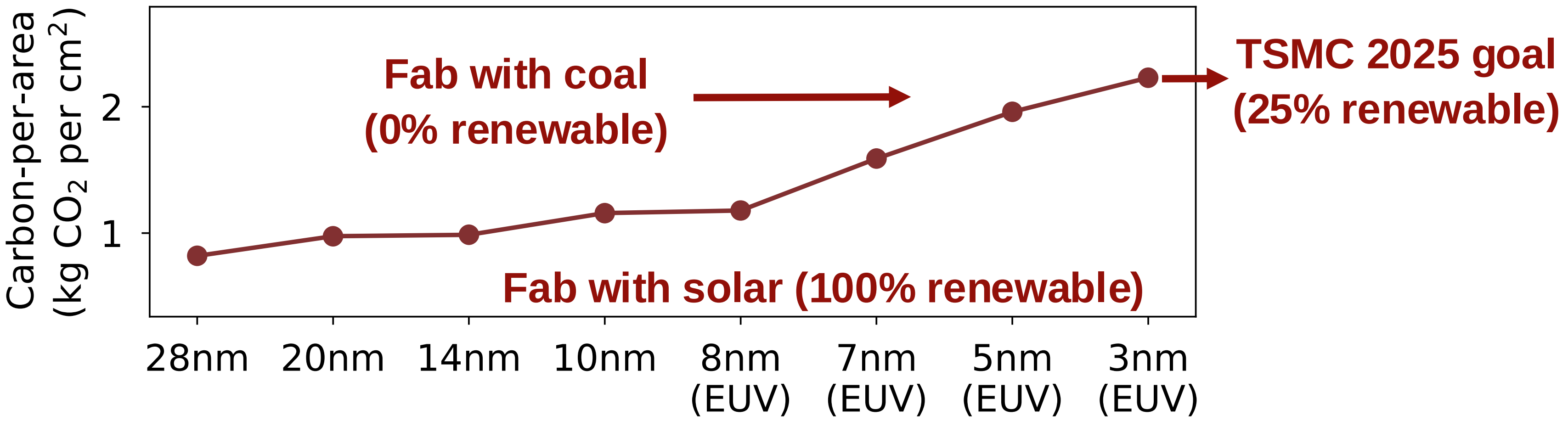

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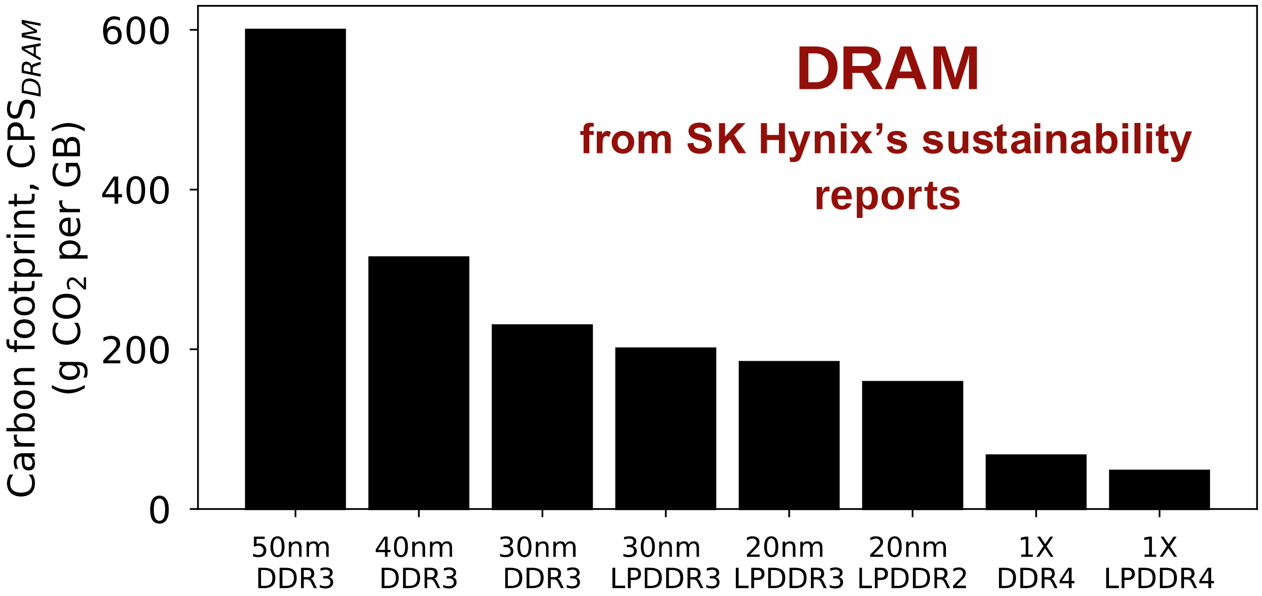
Embodied carbon of DRAM memory

$$Emb_{DRAM} = DRAM_{capacity} \times CPS_{DRAM}$$



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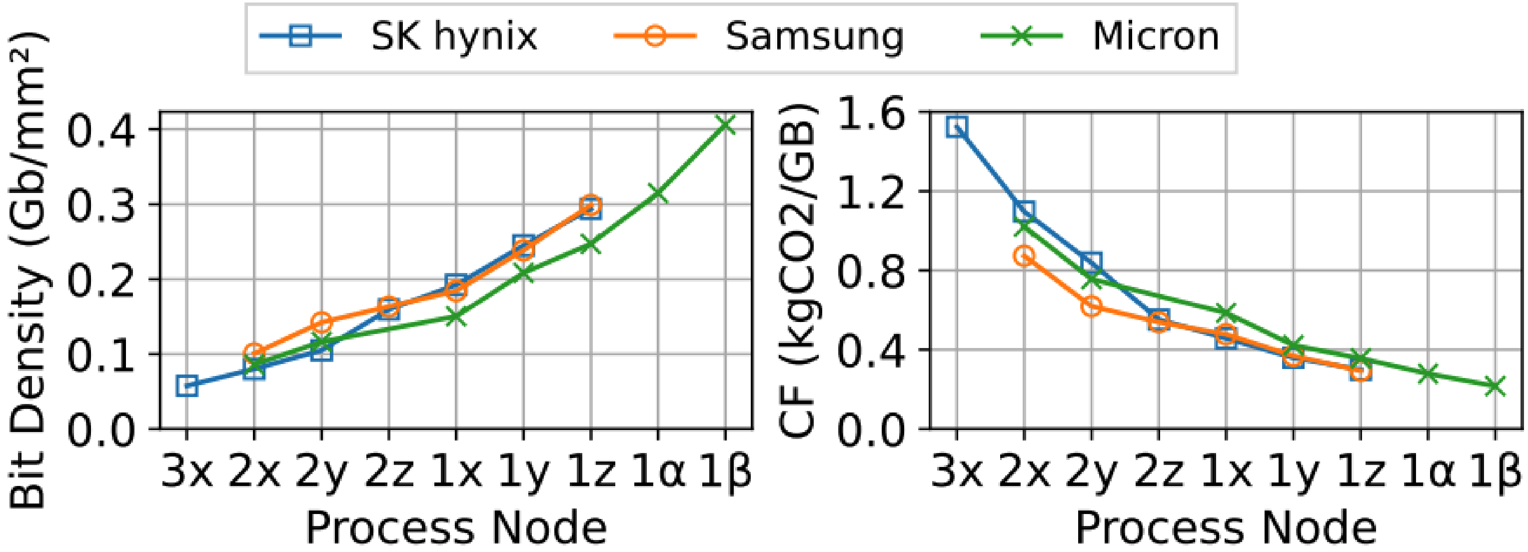
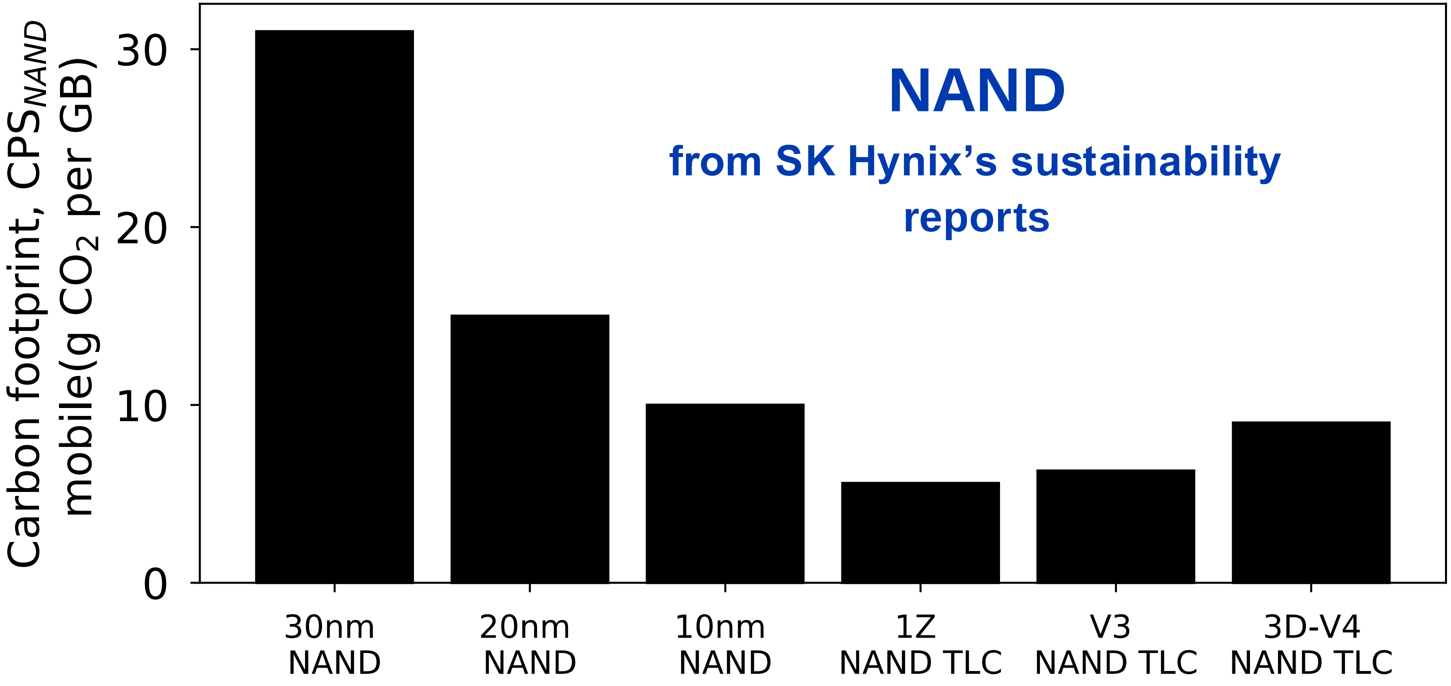


https://hotcarbon.org/assets/2024/pdf/hotcarbon24-final154.pdf

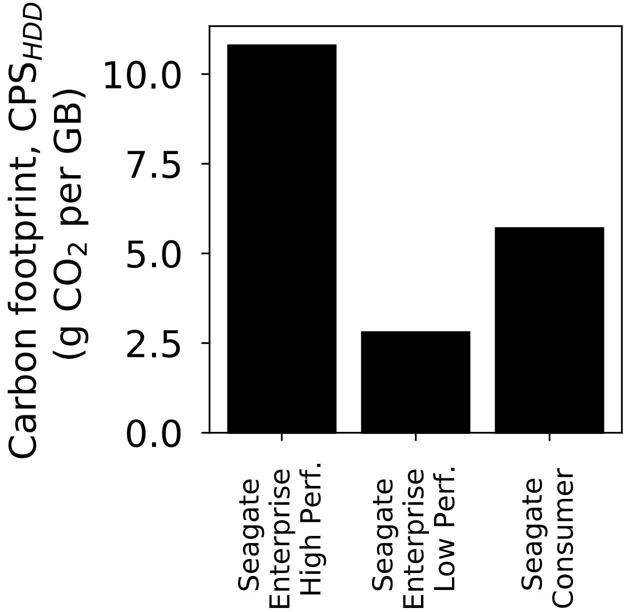
Embodied carbon of NAND Flash storage

$$Emb_{SSD} = SSD_{capacity} \times CPS_{SSD}$$



Embodied carbon of HDD storage

$$Emb_{DRAM} = DRAM_{capacity} \times \boldsymbol{CPS_{DRAM}}$$



HDD

from Seagate's product environmental reports

Additional details found in the paper…

ACT parameters

Parameter	Description	Range
T	App. execution time	From SW profiling
LT	HW lifetime	1-10 years
N_r	Number of ICs	From HW design
K_r	IC packaging footprint	0.15 kg CO_2
A	IC Area	From HW design (cm^2)
p	Process node	3-28 nm
MPA	Procure materials	~0.50kg CO_2 per cm^2
EPA	Fab energy	0.8-3.5 kWh per cm^2
CI_{use}	HW CO_2 intensity	30-700 g CO_2 per kWh
CI_{fab}	Fab CO_2 intensity	30-700 g CO_2 per kWh
GPA	GHG from fab	0.1-0.5 kg CO_2 per cm^2
Y	Fab yield	0-1
CPA	CO_2 from fab	0.1-0.4 kg CO_2 per cm^2
E_{DRAM}	DRAM embodied CO_2	0-0.6 kg CO_2 per GB
E_{SSD}	SSD embodied CO_2	0-0.03 kg CO_2 per GB
E_{HDD}	HDD embodied CO_2	0-0.12 kg CO_2 per GB

Challenge: How do we design sustainable systems by considering the footprint across lifecycles

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Current carbon accounting methodologies

Economic Input/Output (EIO)

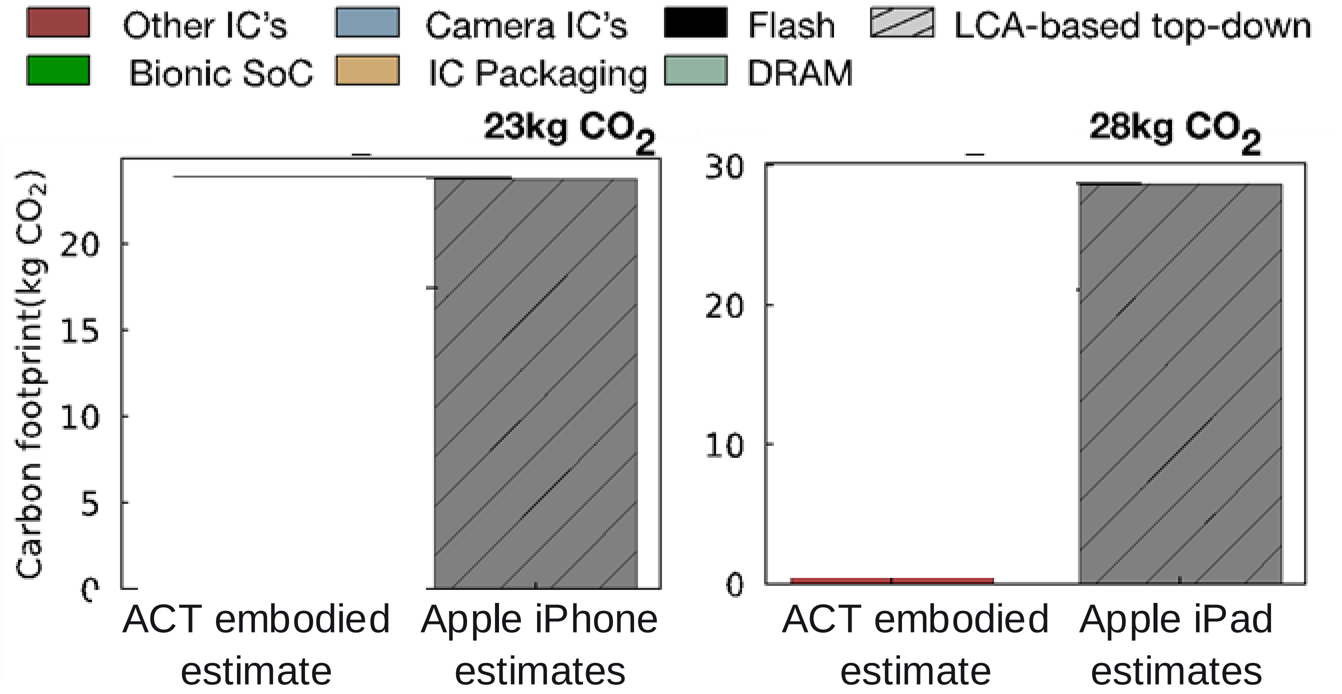
Carbon is tied directly to economic cost which is susceptible to market effects.

Life cycle analysis (LCA)

Current databases are out-of-date (45nm or older nodes).

LCA's take high $$ and time to conduct.

Comparing ACT with Apple's product environmental reports



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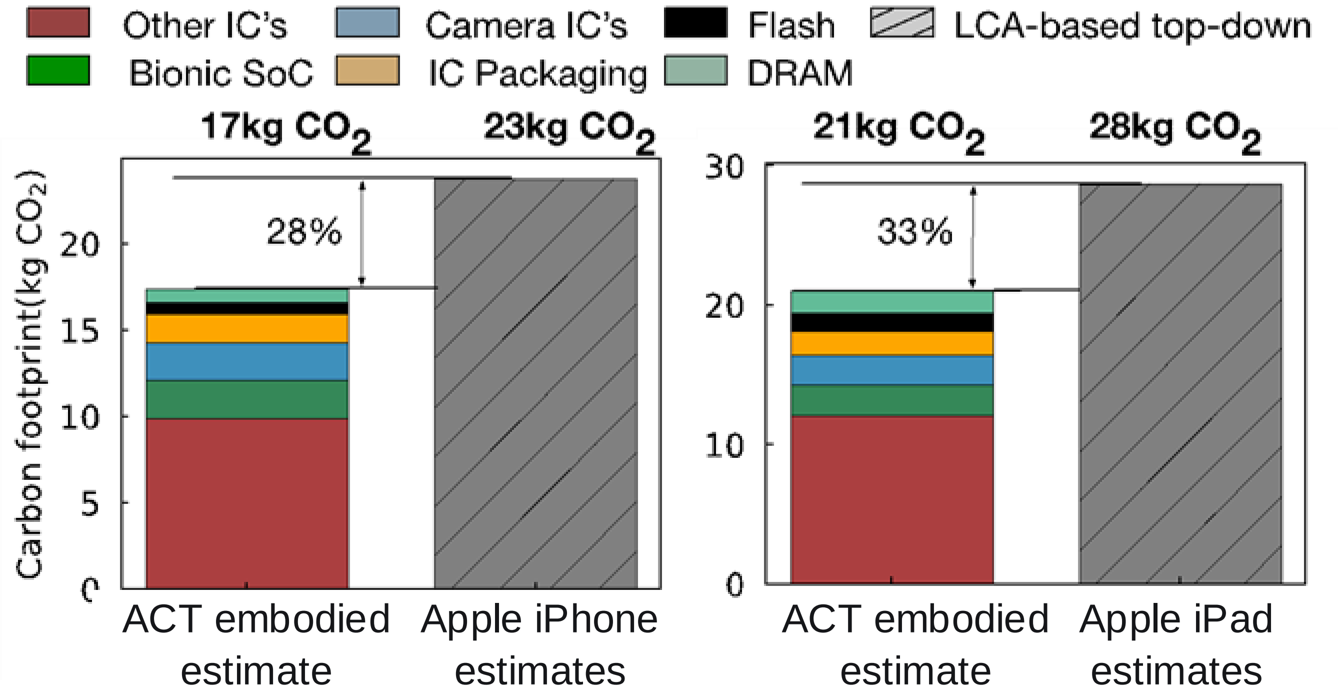

More comparisons (ACT vs. LCA’s) in the paper…

	ACT vs. Dell R740 server LCA	ACT vs. Fairphone 3 mobile device LCA

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IC component	ACT vs. Dell R740 server LCA	ACT vs. Fairphone 3 mobile device LCA
Compute (processors, SoC’s)	Within 2.2x	Within 1.18x
Memory	Within 1.62x	Within 2.1x
Storage	Within 1.05-2.2x	

Takeaways

(1) ACT provides first-order approximate of LCA’s that use old technology nodes (45nm NAND, 32nm CPU)

(2) ACT enables architects to study new technology nodes

Setting the standard for data center sustainability

Understanding the life cycle impact of data center components

We cannot reduce what we do not measure. In 2022, we conducted Life Cycle Assessments (LCAs) on several data center hardware products and developed internal visualization tools to identify the highest carbon emitting components of each product.

At the data center fleet level, the Sustainability, Physical Modeling, and Meta AI Systems and Machine Learning teams have partnered on a large-scale project to develop and scale a dataset containing the best available embodied carbon estimates at the scale of the hundreds of millions of components in our data center hardware.

In 2022, the teams reached more than 90% coverage, meaning there is primary data, an LCA, or a [modeled↗] value assigned to each asset. This dataset lays the foundation for value chain carbon reductions by helping us use less or choose low-carbon options, engage suppliers, and drive value chain and system-level interventions in line with Meta's net zero strategy.

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Tenets of Environmental Design

Reduce

Design leaner footprint software and hardware.

Recycle

Recover discarded systems and components.

Reuse

Repurpose systems already produce.

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Reuse: General purpose versus custom mobile HW

AI inference case study (MobileNet) assuming 3 year hardware lifetime, and same utilization in all cases

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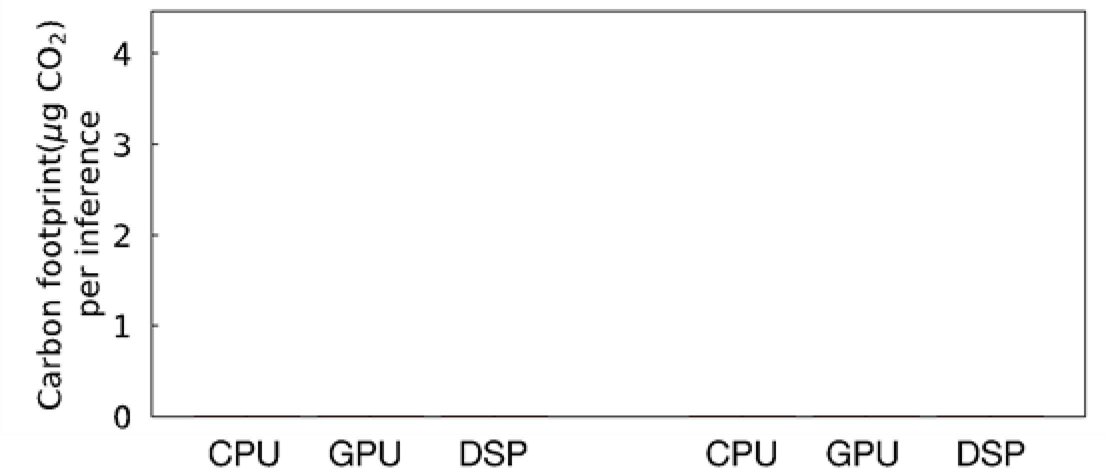

Without renewables during operation → **With renewables during operation**

Reuse: General purpose versus custom mobile HW

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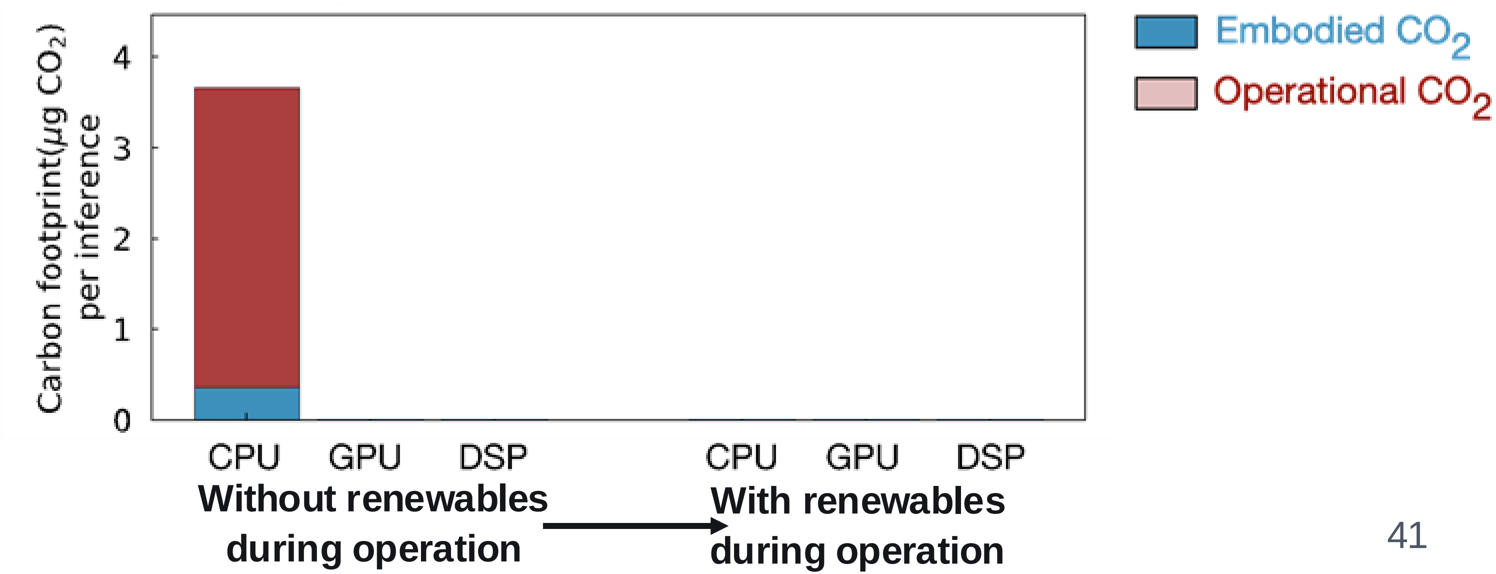
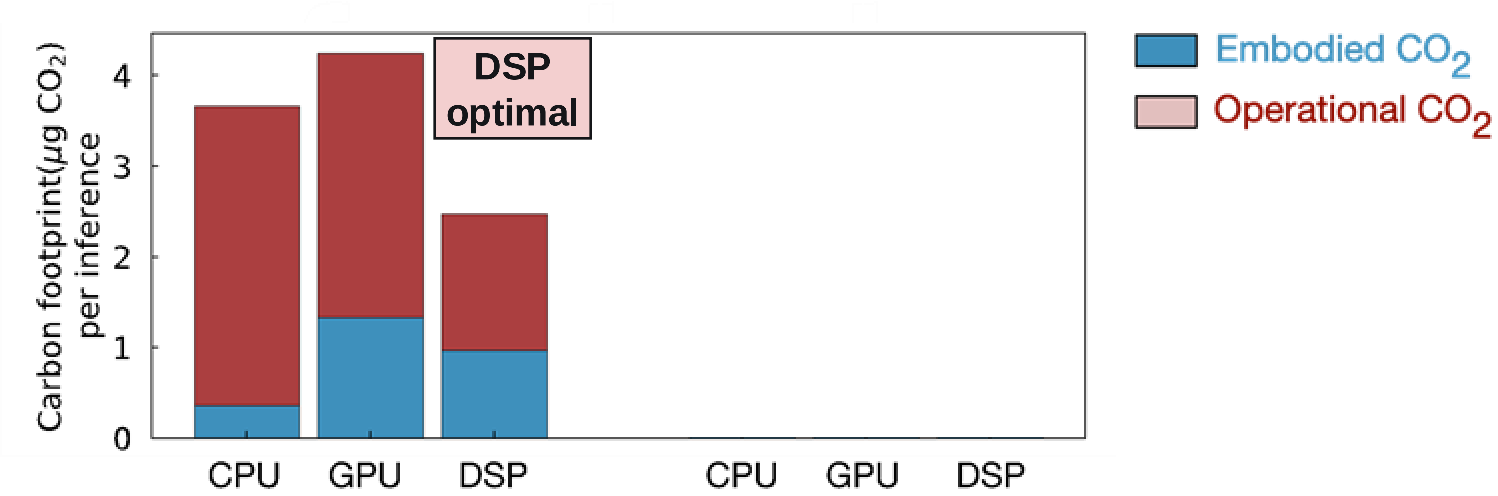


Reuse: General purpose versus custom mobile HW

AI inference case study (MobileNet) assuming 3 year hardware lifetime, and same utilization in all cases

Commodity (mobile CPU)
Specialized (mobile GPU, DSP)
→ **Architectural Carbon Model** → Carbon per inference



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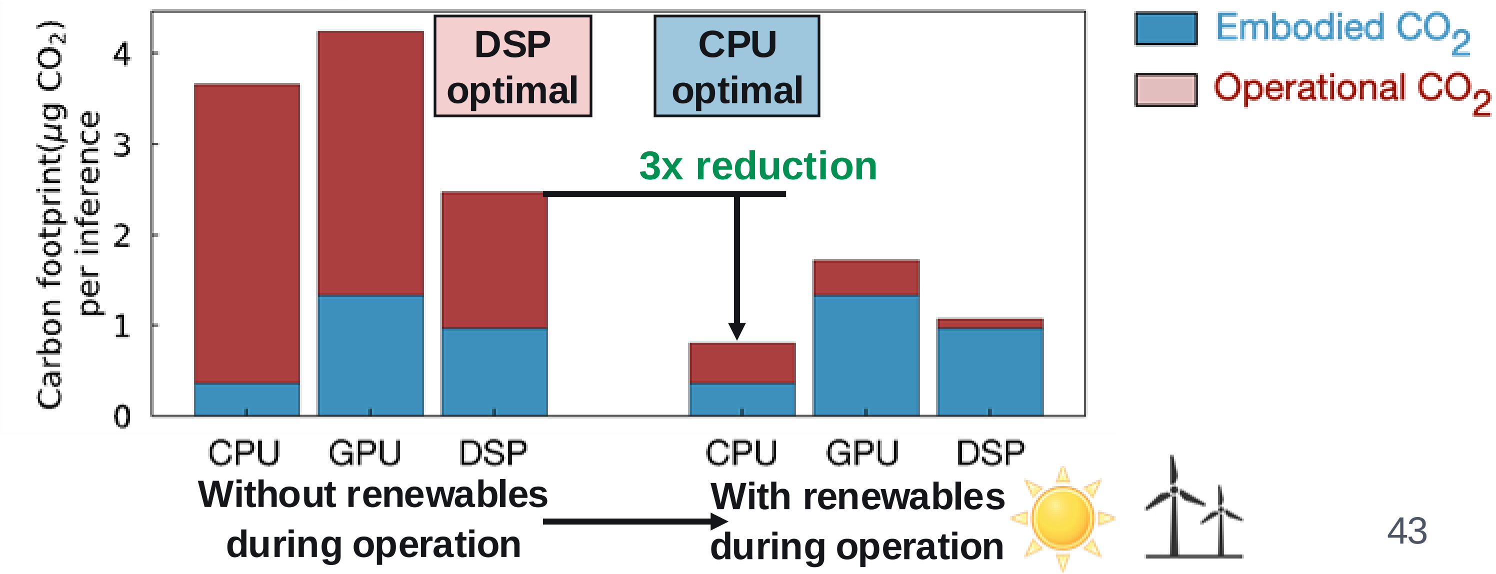

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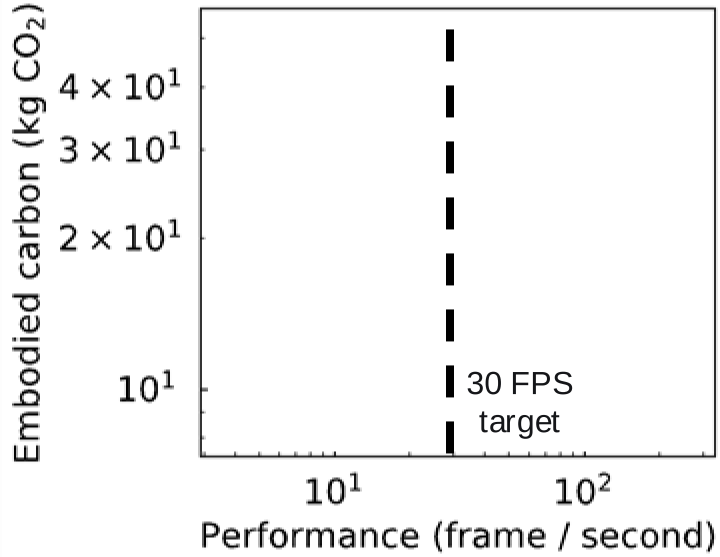

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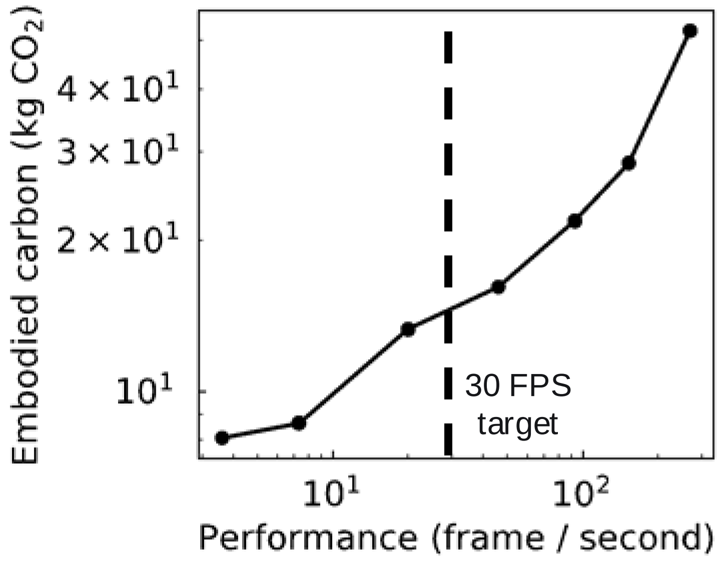

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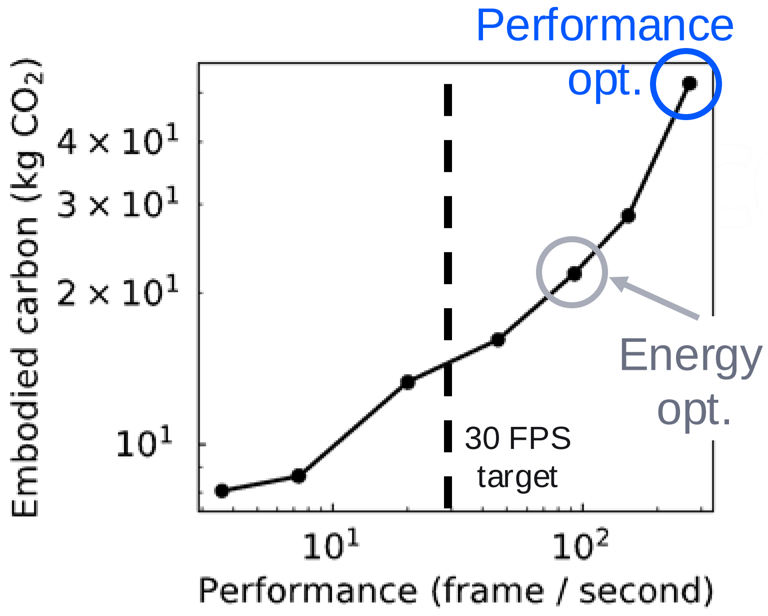

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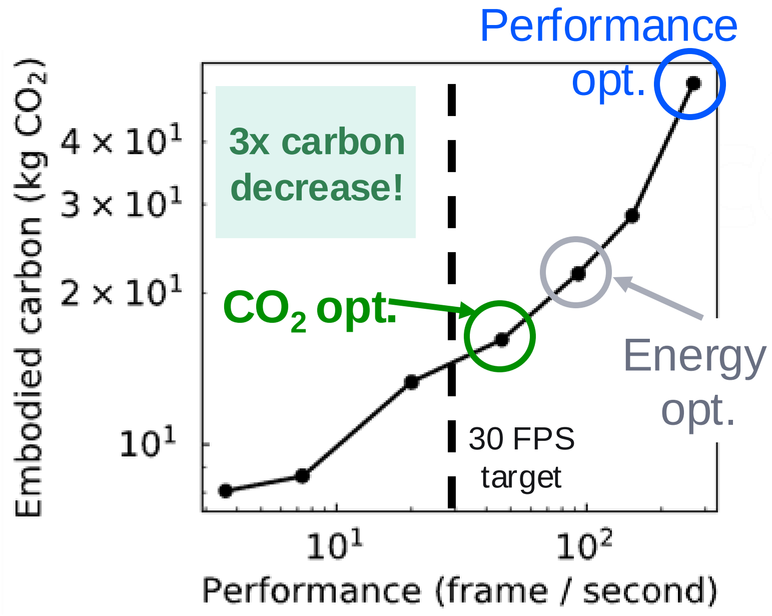

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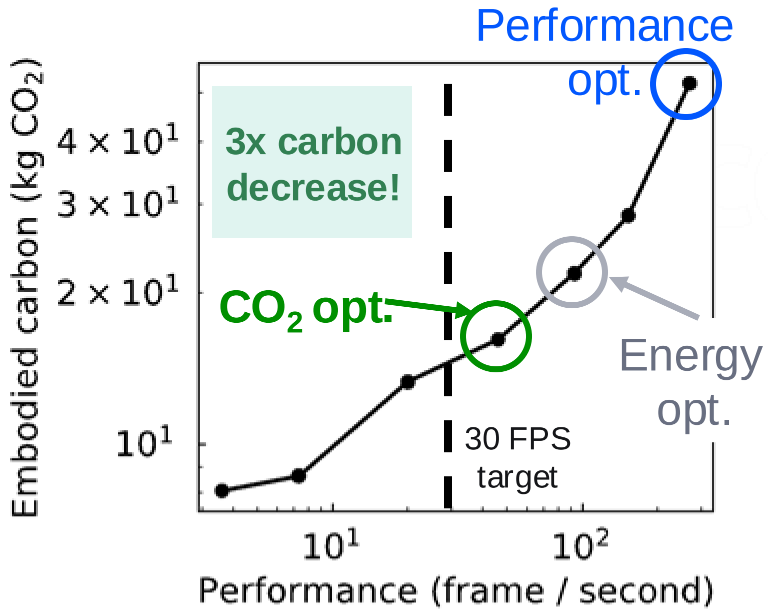

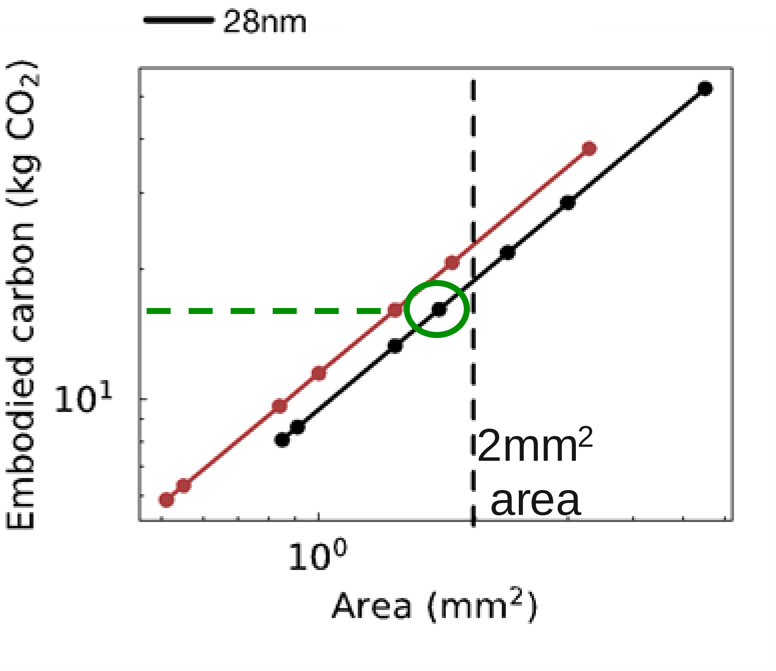

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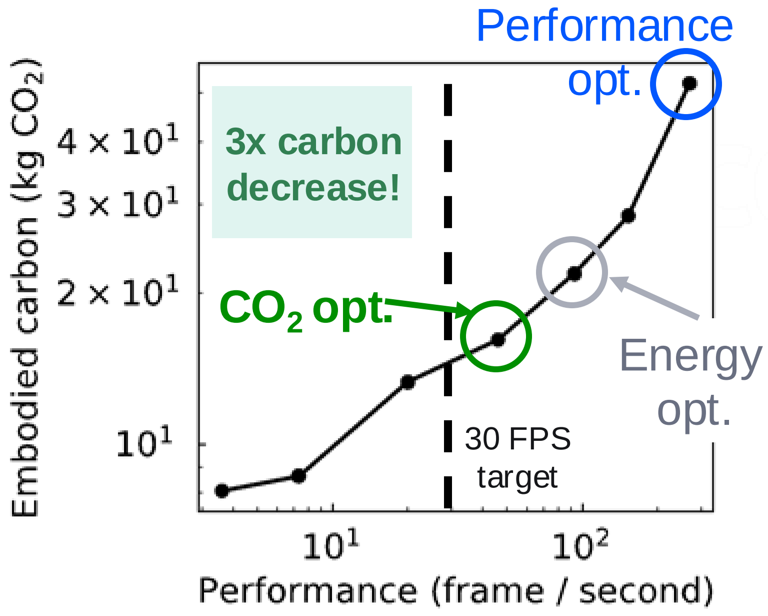

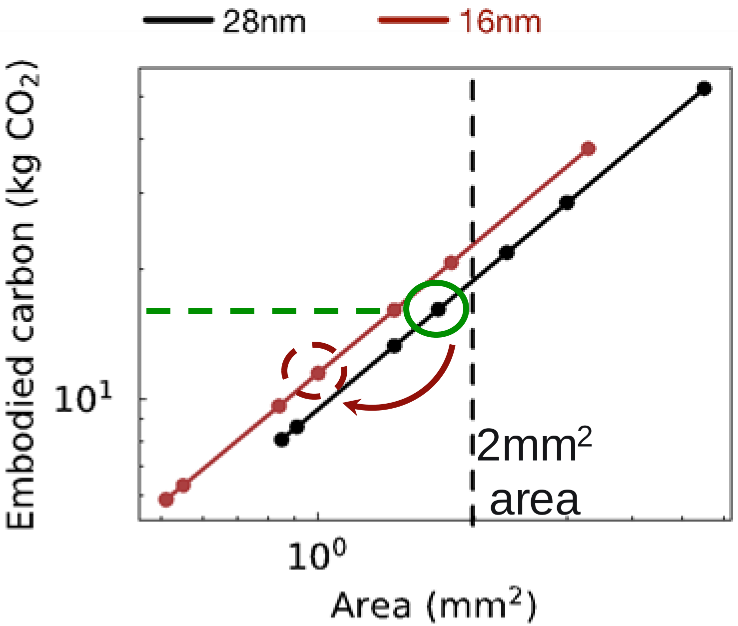

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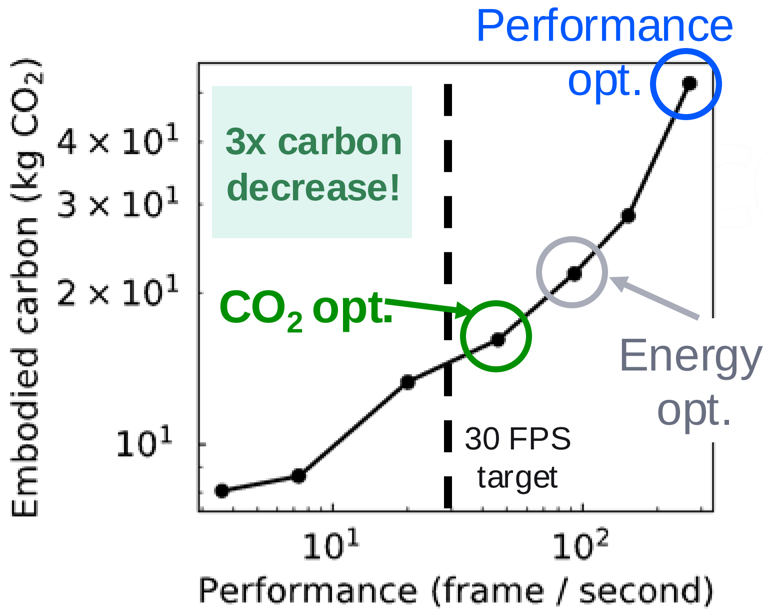

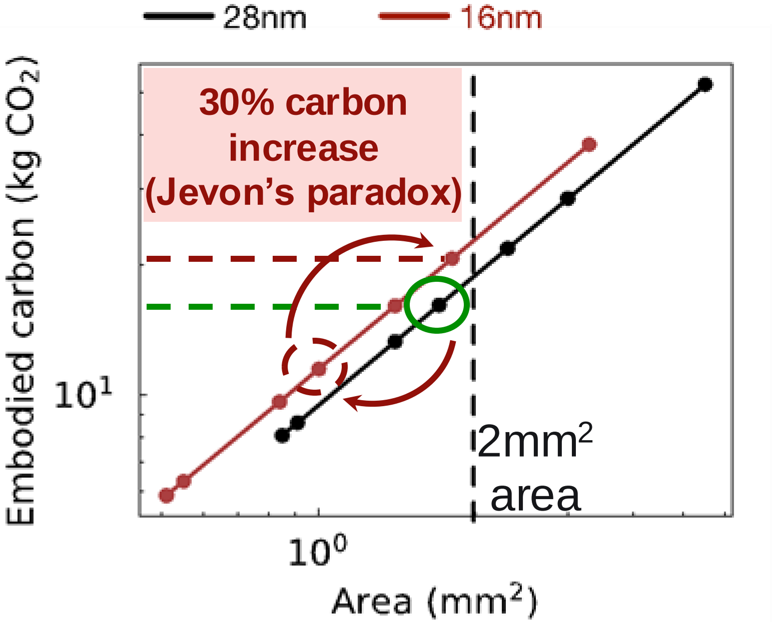

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Recycle: Extending hardware lifetime

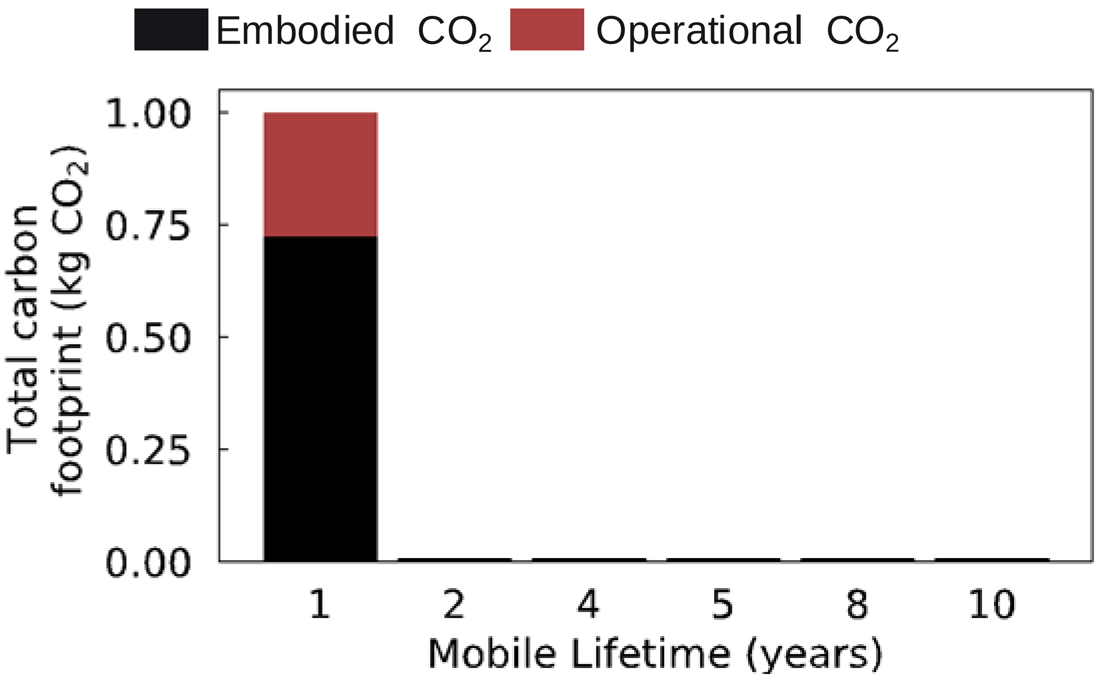
Mobile SoC's
Geekbench characterization

Architectural Carbon Model

Operational vs. Embodied carbon

Recycle: Extending hardware lifetime

Mobile SoC's Geekbench characterization → **Architectural Carbon Model** → Operational vs. Embodied carbon



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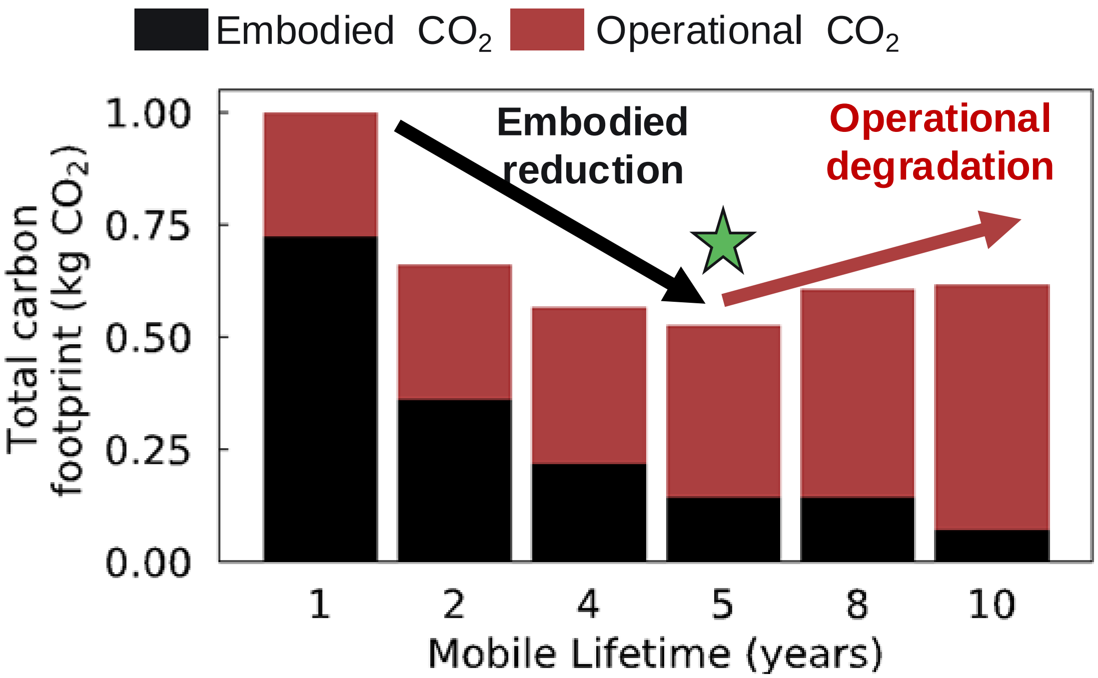

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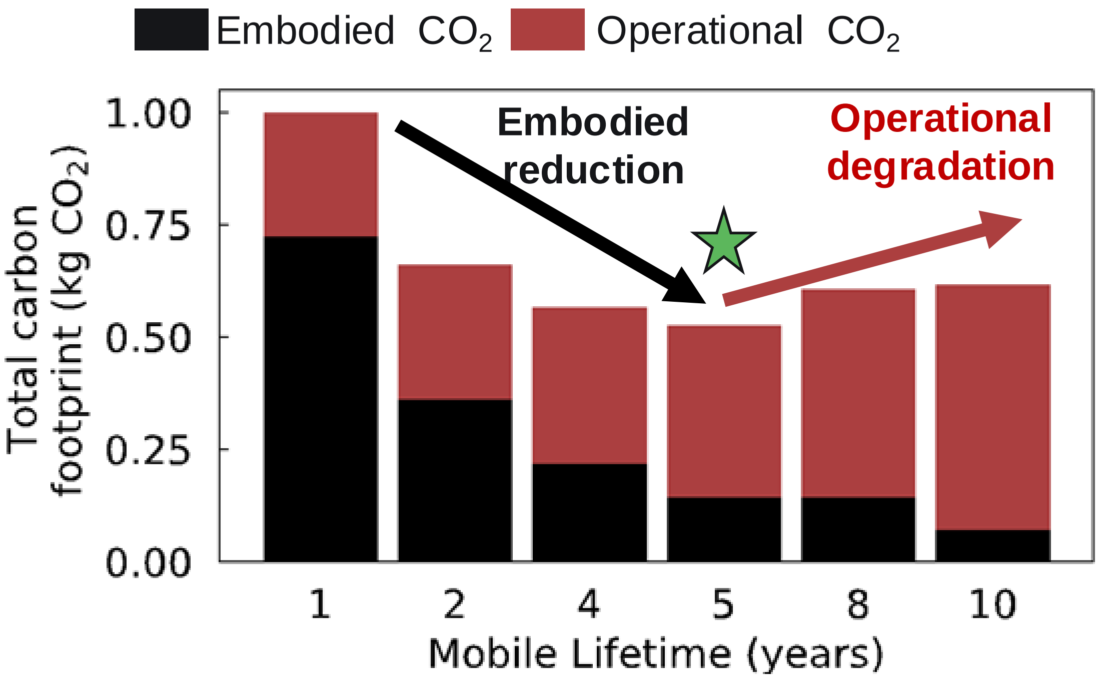

Enabling **2nd life** requires enhancing **HW reliability**

See paper for case study on storage reliability using **SSD overprovisioning**

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Application

OS/Run-time

Systems

Compiler

Architecture

Circuits

Devices & Technology

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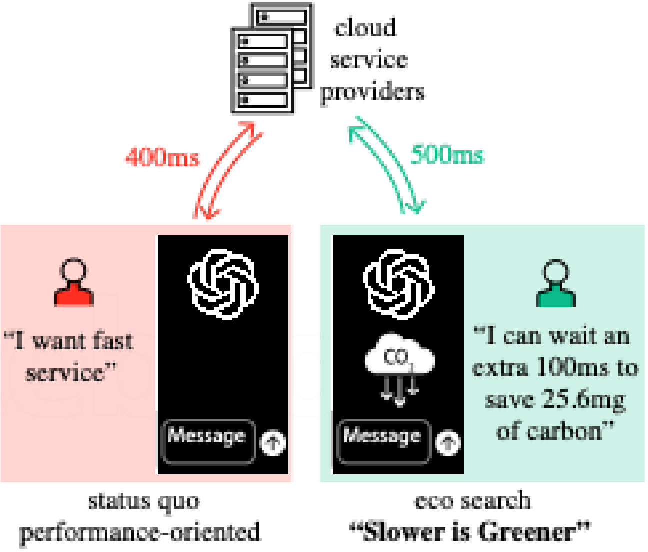
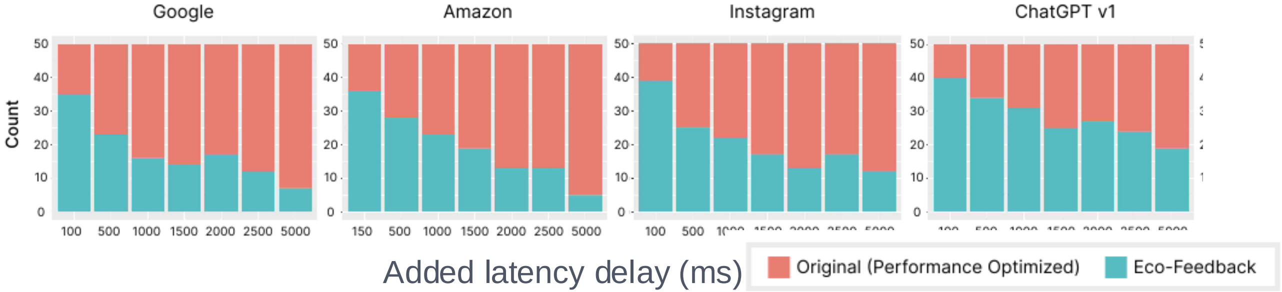
Leveraging Eco-Feedback for Carbon-Aware SLO’s

- Application
- OS/Run-time
- Systems
- Compiler
- Architecture
- Circuits
- Devices & Technology





Attributing carbon footprint of cloud usage

Application

OS/Run-time

Systems

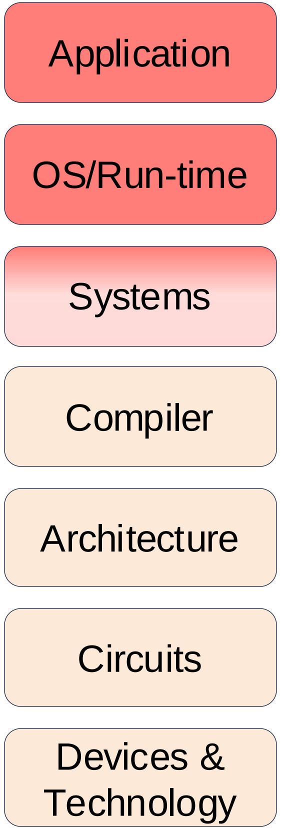
Compiler

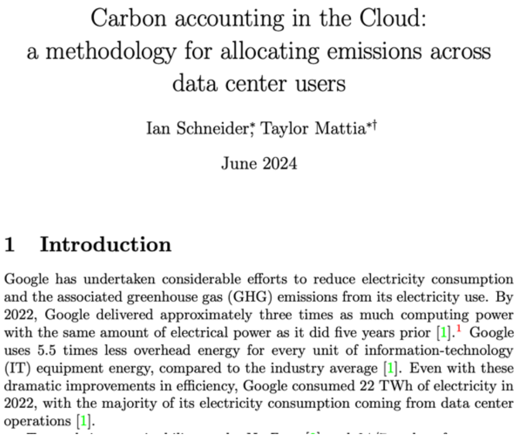
Architecture

Circuits

Devices & Technology

Fairly attributing carbon




Carbon accounting in the Cloud:
a methodology for allocating emissions across data center users

Ian Schneider*, Taylor Mattia*†

June 2024

1 Introduction

Google has undertaken considerable efforts to reduce electricity consumption and the associated greenhouse gas (GHG) emissions from its electricity use. By 2022, Google delivered approximately three times as much computing power with the same amount of electrical power as it did five years prior [1].[1] Google uses 5.5 times less overhead energy for every unit of information-technology (IT) equipment energy, compared to the industry average [1]. Even with these dramatic improvements in efficiency, Google consumed 22 TWh of electricity in 2022, with the majority of its electricity consumption coming from data center operations [1].

Fairly attributing carbon

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- OS/Run-time
- Systems
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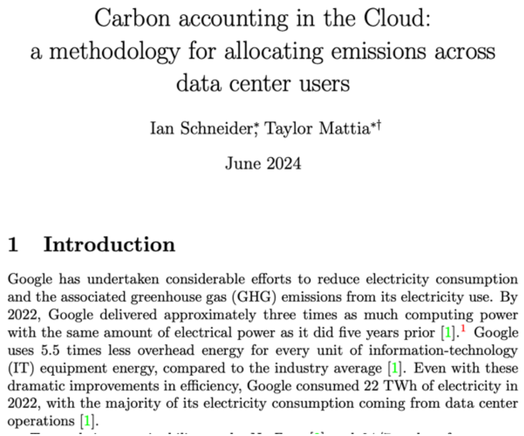

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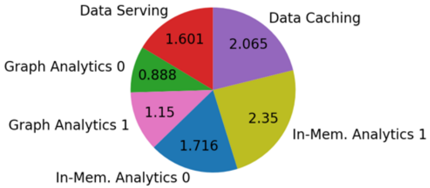
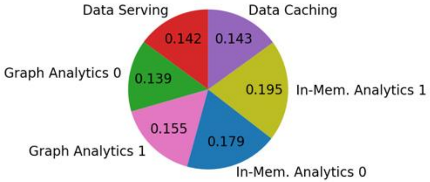


Operational Breakdown

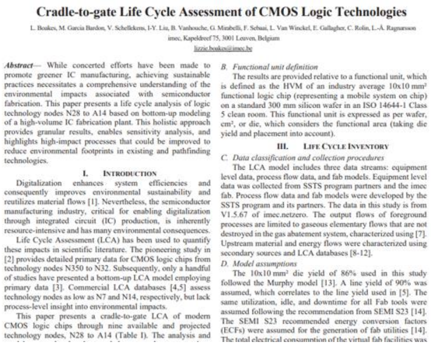


Embodied Breakdown

Open research questions:

- How do we fairly attribute operational and embodied carbon to individual cloud services?
- How do we consider varying demand in data centers in attributing carbon responsibility?
- How do we scale attribution mechanisms to cloud-scale?

Uncertainty is inherent in carbon accounting



Cradle-to-gate Life Cycle Assessment of CMOS Logic Technologies

L. Boakes, M. Garcia Bardon, V. Schellekens, I-Y. Liu, B. Vanhouche, G. Mirabelli, F. Sebaai, L. Van Winckel, E. Gallagher, C. Rolin, L.-Å. Ragnarsson
imec, Kapeldreef 75, 3001 Leuven, Belgium
lizzie.boakes@imec.be

Abstract— While concerted efforts have been made to promote greener IC manufacturing, achieving sustainable practices necessitates a comprehensive understanding of the environmental impacts associated with semiconductor fabrication. This paper presents a life cycle analysis of logic technology nodes N28 to A14 based on bottom-up modeling of a high-volume IC fabrication plant. This holistic approach provides granular results, enables sensitivity analysis, and highlights high-impact processes that could be improved to reduce environmental footprints in existing and pathfinding technologies.

I. Introduction

Digitalization enhances system efficiencies and consequently improves environmental sustainability and reutilizes material flows [1]. Nevertheless, the semiconductor manufacturing industry, critical for enabling digitalization through integrated circuit (IC) production, is inherently resource-intensive and has many environmental consequences.

Life Cycle Assessment (LCA) has been used to quantify these impacts in scientific literature. The pioneering study in [2] provides detailed primary data for CMOS logic chips from technology nodes N350 to N32. Subsequently, only a handful of studies have presented a bottom-up LCA model employing primary data [3]. Commercial LCA databases [4,5] assess technology nodes as low as N7 and N14, respectively, but lack process-level insight into environmental impacts.

This paper presents a cradle-to-gate LCA of modern CMOS logic chips through nine available and projected technology nodes, N28 to A14 (Table I). The analysis and

B. Functional unit definition

The results are provided relative to a functional unit, which is defined as the HVM of an industry average 10x10 mm² functional logic chip (representing a mobile system on chip) on a standard 300 mm silicon wafer in an ISO 14644-1 Class 5 clean room. This functional unit is expressed as per wafer, cm², or die, which considers the functional area (taking die yield and placement into account).

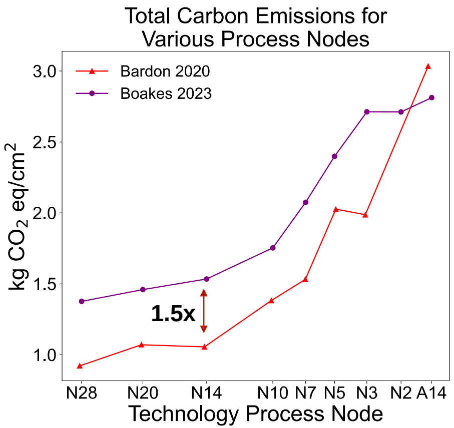
III. Life Cycle Inventory

C. Data classification and collection procedures

The LCA model includes three data streams: equipment level data, process flow data, and fab models. Equipment level data was collected from SSTS program partners and the imec fab. Process flow data and fab models were developed by the SSTS program and its partners. The data in this study is from V1.5.67 of imec.netzero. The output flows of foreground processes are limited to gaseous elementary flows that are not destroyed in the gas abatement system, characterized using [7]. Upstream material and energy flows were characterized using secondary sources and LCA databases [8-12].

D. Model assumptions

The 10x10 mm² die yield of 86% used in this study followed the Murphy model [13]. A line yield of 90% was assumed, which correlates to the line yield used in [5]. The same utilization, idle, and downtime for all Fab tools were assumed following the recommendation from SEMI S23 [14]. The SEMI S23 recommended energy conversion factors (ECFs) were assumed for the generation of fab utilities [14]. The total electrical consumption of the virtual fab facilities was



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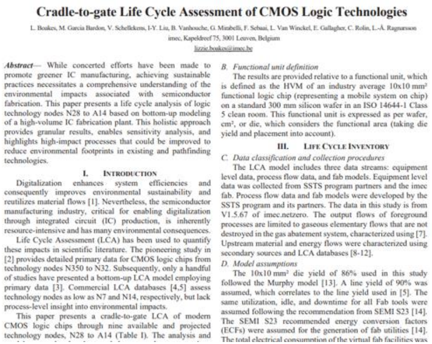

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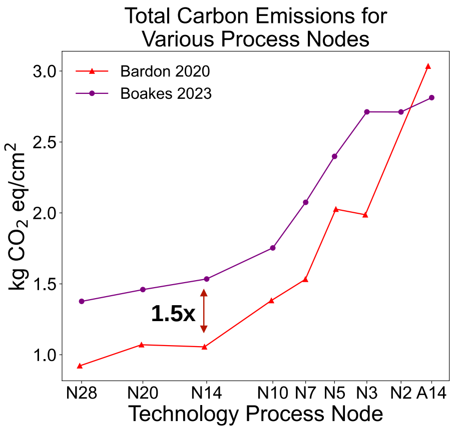

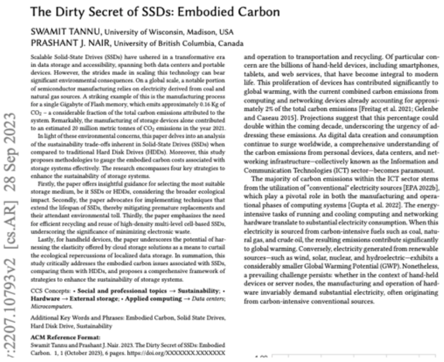

The Dirty Secret of SSDs: Embodied Carbon

SWAMIT TANNU, University of Wisconsin, Madison, USA
PRASHANT J. NAIR, University of British Columbia, Canada

Scalable Solid-State Drives (SSDs) have ushered in a transformative era in data storage and accessibility, spanning both data centers and portable devices. However, the strides made in scaling this technology can bear significant environmental consequences. On a global scale, a notable portion of semiconductor manufacturing relies on electricity derived from coal and natural gas sources. A striking example of this is the manufacturing process for a single Gigabyte of Flash memory, which emits approximately 0.16 Kg of CO_2 – a considerable fraction of the total carbon emissions attributed to the system. Remarkably, the manufacturing of storage devices alone contributed to an estimated 20 million metric tonnes of CO_2 emissions in the year 2021.

In light of these environmental concerns, this paper delves into an analysis of the sustainability trade-offs inherent in Solid-State Drives (SSDs) when compared to traditional Hard Disk Drives (HDDs). Moreover, this study proposes methodologies to gauge the embodied carbon costs associated with storage systems effectively. The research encompasses four key strategies to enhance the sustainability of storage systems.

Firstly, the paper offers insightful guidance for selecting the most suitable storage medium, be it SSDs or HDDs, considering the broader ecological impact. Secondly, the paper advocates for implementing techniques that extend the lifespan of SSDs, thereby mitigating premature replacements and their attendant environmental toll. Thirdly, the paper emphasizes the need for efficient recycling and reuse of high-density multi-level cell-based SSDs, underscoring the significance of minimizing electronic waste.

Lastly, for handheld devices, the paper underscores the potential of harnessing the elasticity offered by cloud storage solutions as a means to curtail the ecological repercussions of localized data storage. In summation, this study critically addresses the embodied carbon issues associated with SSDs, comparing them with HDDs, and proposes a comprehensive framework of strategies to enhance the sustainability of storage systems.

CCS Concepts: • **Social and professional topics → Sustainability**; • **Hardware → External storage**; • **Applied computing** → *Data centers*; *Microcomputers*.

Additional Key Words and Phrases: Embodied Carbon, Solid State Drives, Hard Disk Drive, Sustainability

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and operation to transportation and recycling. Of particular concern are the billions of hand-held devices, including smartphones, tablets, and web services, that have become integral to modern life. This proliferation of devices has contributed significantly to global warming, with the current combined carbon emissions from computing and networking devices already accounting for approximately 2% of the total carbon emissions [Freitag et al. 2021; Gelenbe and Caseau 2015]. Projections suggest that this percentage could double within the coming decade, underscoring the urgency of addressing these emissions. As digital data creation and consumption continue to surge worldwide, a comprehensive understanding of the carbon emissions from personal devices, data centers, and networking infrastructure—collectively known as the Information and Communication Technologies (ICT) sector—becomes paramount.

The majority of carbon emissions within the ICT sector stems from the utilization of "conventional" electricity sources [EPA 2022b], which play a pivotal role in both the manufacturing and operational phases of computing systems [Gupta et al. 2022]. The energy-intensive tasks of running and cooling computing and networking hardware translate to substantial electricity consumption. When this electricity is sourced from carbon-intensive fuels such as coal, natural gas, and crude oil, the resulting emissions contribute significantly to global warming. Conversely, electricity generated from renewable sources—such as wind, solar, nuclear, and hydroelectric—exhibits a considerably smaller Global Warming Potential (GWP). Nonetheless, a prevailing challenge persists: whether in the context of hand-held devices or server nodes, the manufacturing and operation of hardware invariably demand substantial electricity, often originating from carbon-intensive conventional sources.

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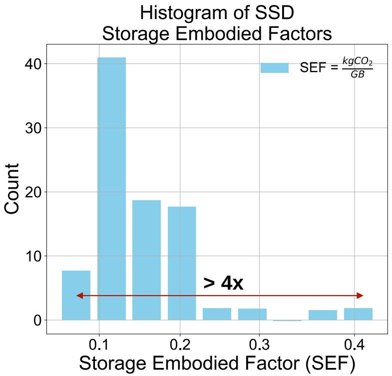

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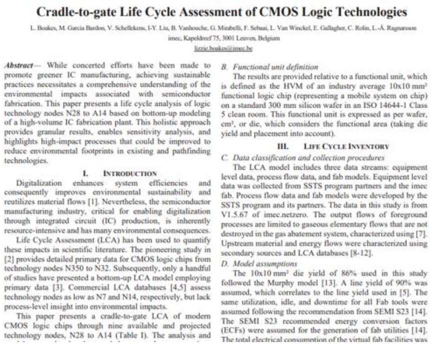
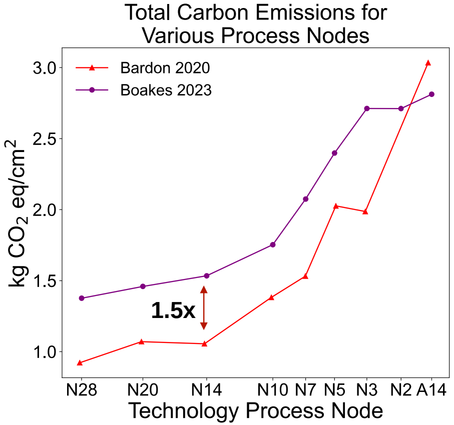
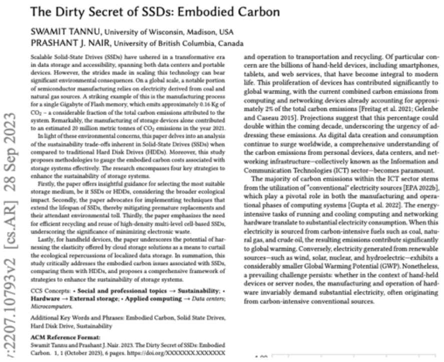
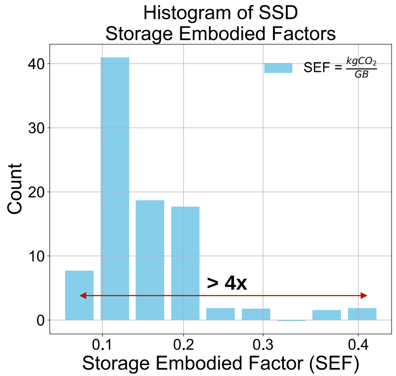








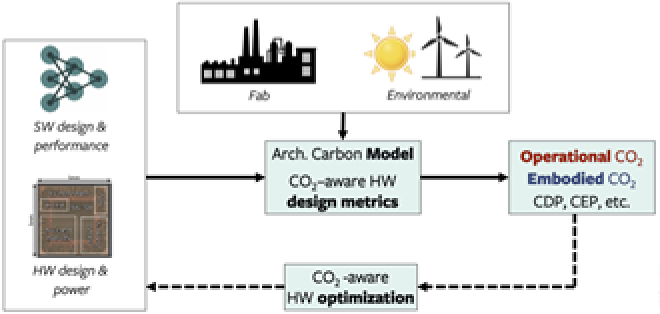
Open research questions:

- What magnitude uncertainty exists across all IC components?
- What degree of uncertainty exists in embodied versus operational carbon?
- How do we consider uncertainty in carbon-aware hardware design to enable robust sustainable computing decisions?

**Attend our group's talk "Understanding the Implications of Uncertainty in Embodied Carbon Models for Sustainable Computing" (Session 4)*

This work: ACT

Develop the model	Case studies



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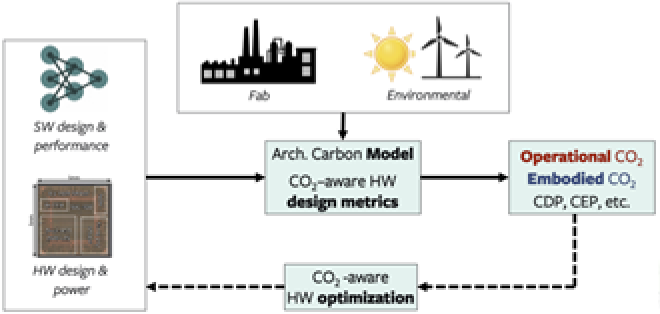

More details in the paper!

- **Modeling parameters** and industry **sources** for data
- **Carbon-aware metrics** for early DSE (e.g., EDP, CDP, CEP)
- Detailed **comparison** against industry LCA’s
- Reuse case study: impact of **reconfigurable accelerators** (FPGA’s)
- Recycle case study: Enabling **second life** & SSD provisioning

Thank you!

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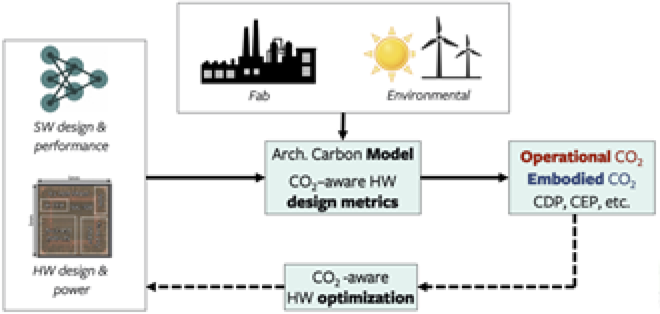
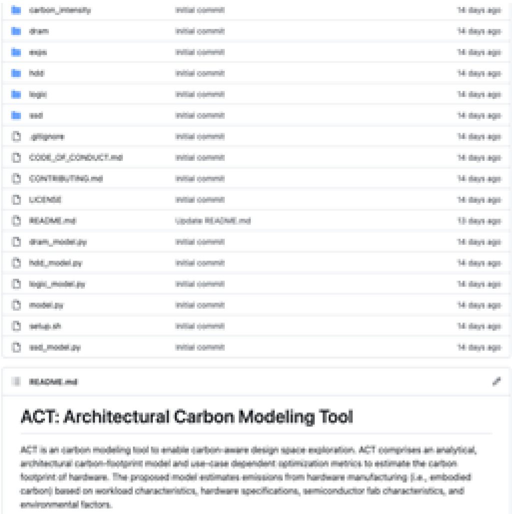


Case studies

Open-source!



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ACT Tutorial: Today

Time	Topic
1:00 – 1:15pm	Welcome to the ACT tutorial!
1:15 – 1:30pm	Motivation: Understanding the source of computing's emissions
1:30 – 2:15pm	Overview of ACT: An Architectural Carbon Modeling Tool
2:15 –2:45pm	**Hands-on ACT demo's**
2:45 – 3:00pm	Extending ACT
3:00 – 3:30pm	Coffee break