JTAG Test Access Port Controller

It is the interface used for JTAG control. The IEEE standard defines four mandatory TAP signals and one optional TRST signal:

1. **TDI** (Test Data Input) → It is used to feed data serially to the target.
2. **TDO** (Test Data Output) → It is used to collect data serially from target.
3. **TCK** (Test Clock) → It is the clock to the registers.
4. **TMS** (Test Mode Select) → It controls the TAP controller state transitions.
5. [Optional] **TRST** (Test Reset) → It resets the TAP controller.

- **TAP Controller**

It controls the JTAG operation. It is basically a 16-state Finite State Machine (FSM) whose state transitions are controlled by the TMS signal as shown in Figure 2. The TAP controller can change state only at the rising edge of TCK and the next state is determined by the logic level of TMS and the present state.

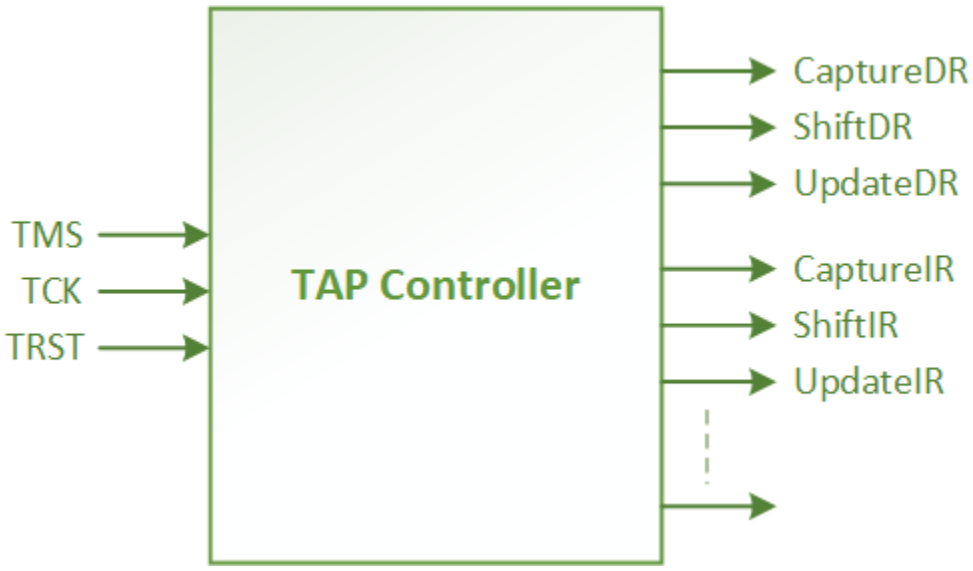

Figure 1: A top level view of TAP Controller

Figure 1 shows a very basic top-level view of TAP controller. TMS, TCK and the optional TRST signals go to a 16-state FSM, which produces various control signals depending upon the FSM's state. These output signals include dedicated control signals for Instruction Register (IR): CaptureIR, ShiftIR, UpdateIR and generic control signals for all Data Registers (DR): CaptureDR, ShiftDR, UpdateDR along with other control signals.

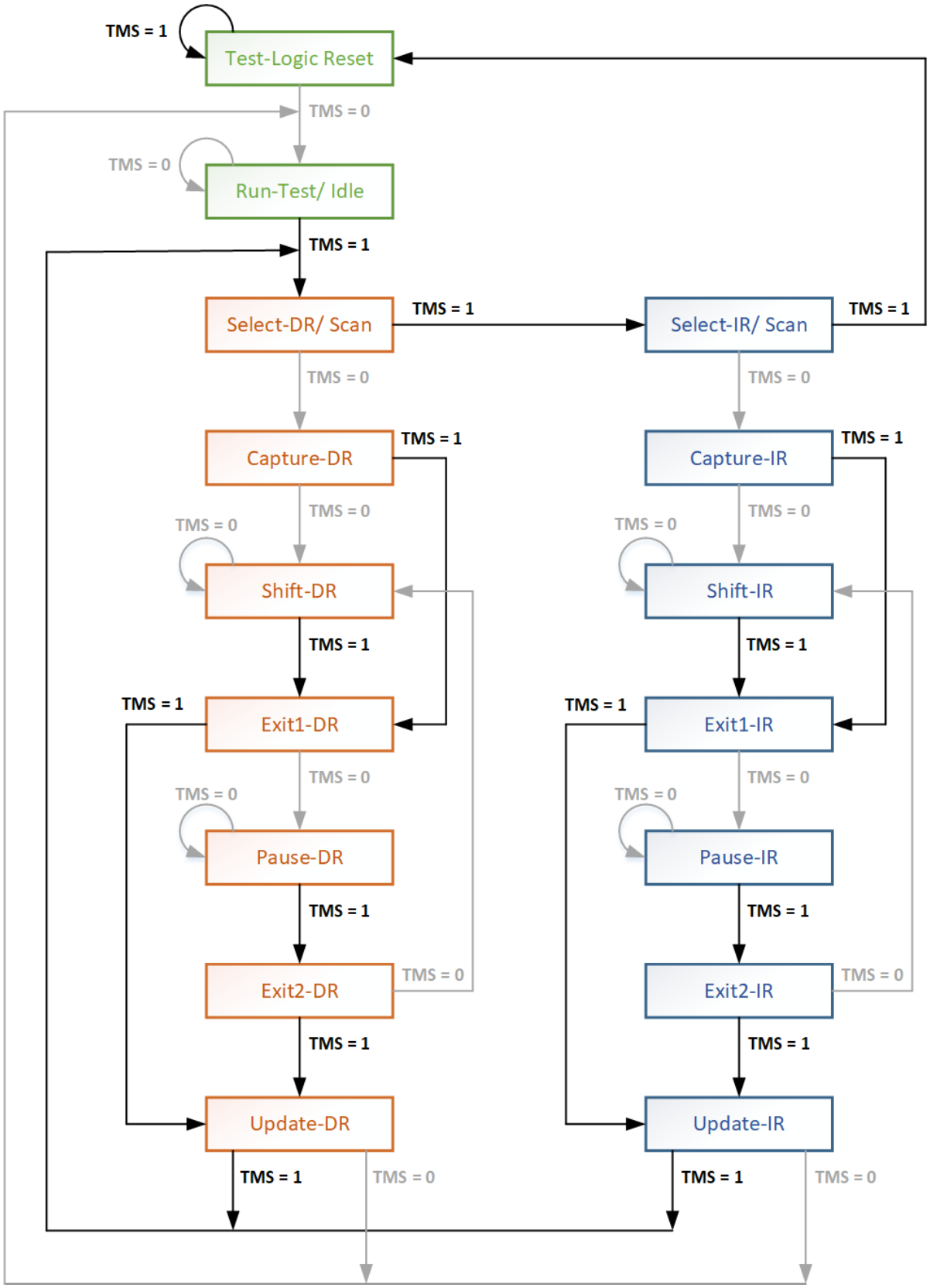

Figure 2: State transition diagram of TAP Controller FSM

A brief description about the different states of the TAP controller:

- **Test-Logic-Reset:** It resets the JTAG circuits. Whenever the TRST (optional) signal is asserted, it goes back to this state. Also notice that in whatever state the TAP controller may be at, it will go back to this state if TMS is set to 1 for 5 consecutive TCK cycles. Thus, if we don't have the TRST signal then we can still reset the circuit.

- **Run-Test/Idle:** This is a state in which the FSM is waiting for some test operations to complete.

- **Select-DR/Scan and Select-IR/Scan:** This is a temporary state to allow the test data sequence for the corresponding Register (the IR in Select-IR/Scan state and the selected DR in Select-DR/Scan state) to be initiated.

- **Capture-DR and Capture-IR:** In this state, data can be loaded in parallel to the corresponding Register

- **Shift-DR and Shift-IR:** In this state, the required test data is loaded (or unloaded) serially into (or from) the corresponding Register. If you refer the Figure 2, when the TAP controller is in this state, it will stay at this state as long as TMS=0. For each clock cycle, one data bit is shifted into (or out of) the selected Register through TDI (or TDO).

- **Exit1-DR and Exit1-IR:** All parallel-loaded (from the Capture-DR and Capture-IR state) or serial-loaded (from the Shift-DR and Shift IR state) data are held in the Register in this state.

- **Pause-DR and Pause-IR**: The FSM pauses its function here to wait for some external operation

- **Exit2-DR and Exit2-IR:** This state represents the end of the Pause-DR or Pause-IR operation and allows the TAP controller to go back to Shift-DR or Shift-IR state for more data to be shifted in (or shifted out).

- **Update-DR and Update-IR:** The test data stored in the first flop of Register (typically all the Registers have two flops for each bit, we will discuss about it later) is loaded to the second flop in this state.