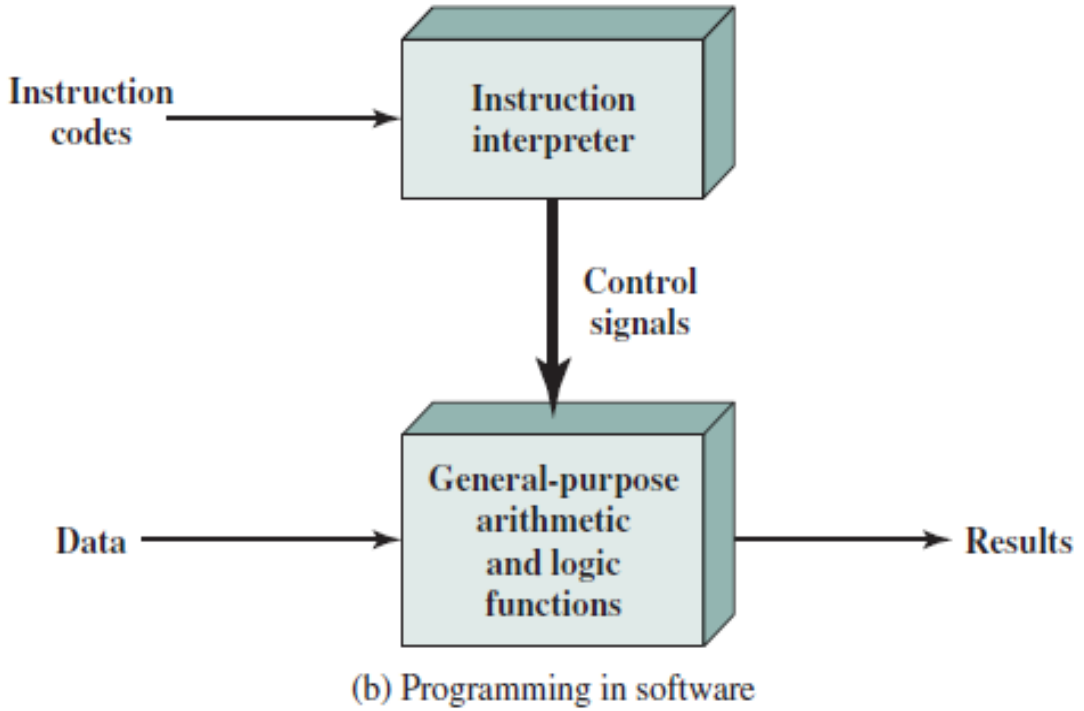
COMPUTER SYSTEM

Computer Components…

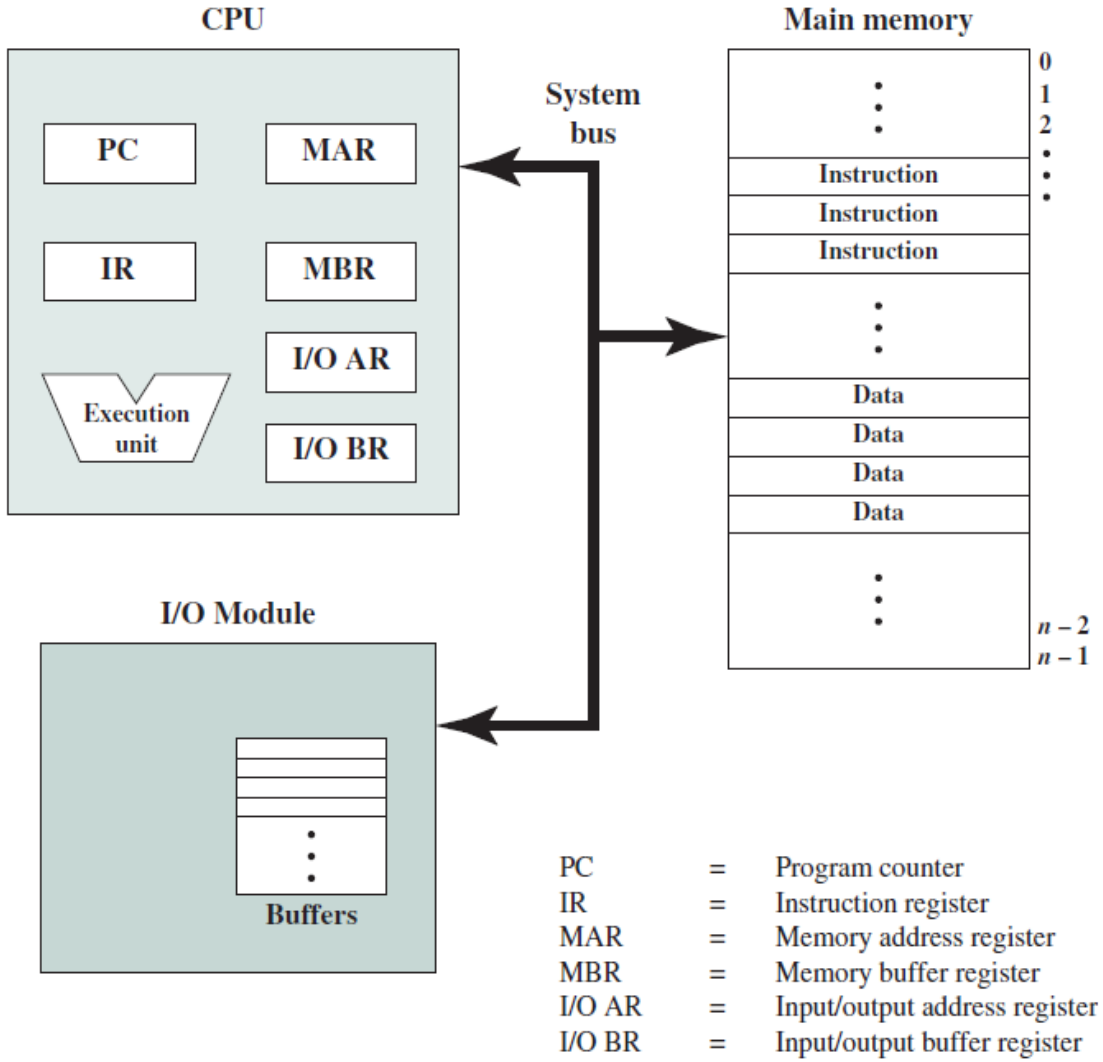
- All contemporary computer designs are based on concepts developed by John von Neumann.
- The von Neumann architecture and is based on three key concepts:
  - Data and instructions are stored in a single read–write memory.
  - Memory are addressable by location
  - Execution occurs in a sequential fashion from one instruction to the next.



(b) Programming in software

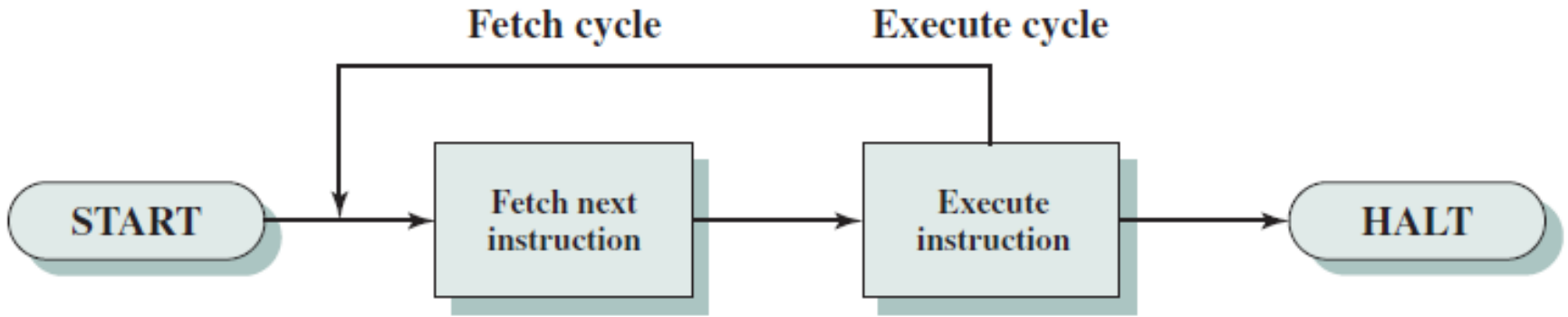
Computer Components

- The CPU exchanges data with memory. For this it uses two internal registers: **a memory address register (MAR)**, which specifies the address in memory for the next read or write, and **a memory buffer register (MBR)**, which contains the data to be written into memory or receives the data read from memory.
- An I/O address register (I/OAR) specifies a particular I/O device. An I/O buffer register (I/OBR) is used for the exchange of data between an I/O module and the CPU.



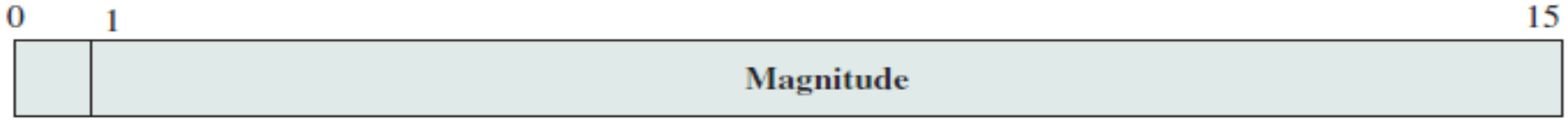
Computer Function

- Instruction processing consists of two steps: The processor reads (fetches) instructions from memory one at a time and executes each instruction.
- Program execution consists of repeating the process of instruction fetch and instruction execution.
- The processing required for a single instruction is called an instruction cycle which consist of the fetch cycle and the execute cycle.



Instruction Fetch and Execute…

(a) Instruction format



(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

Instruction Fetch and Ex

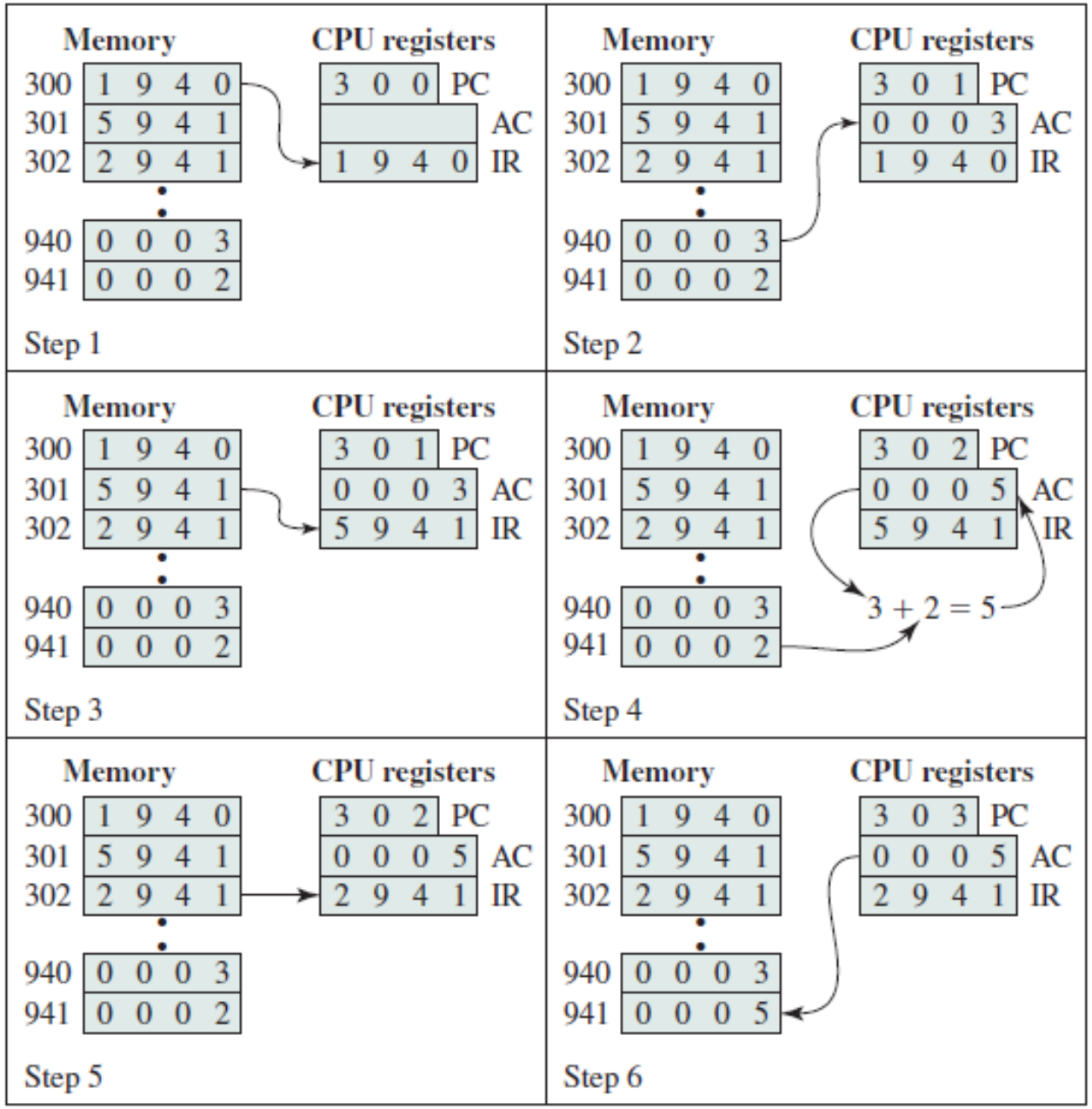


Figure 3.5 Example of Program Execution (contents of memory and registers in hexadecimal)

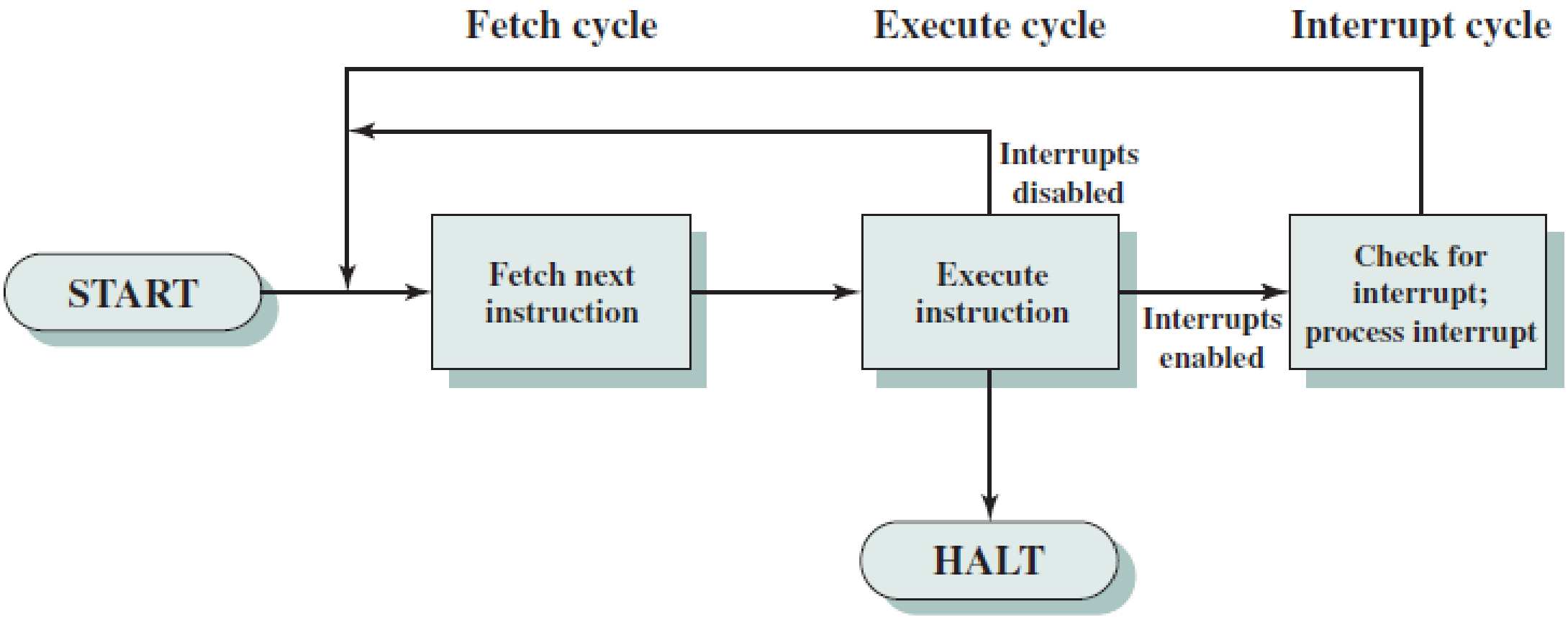
Interrupts…

- All the computers provide a mechanism by which other modules (I/O, memory) may interrupt the normal processing of the processor.

Table 3.1 Classes of Interrupts

Program	Generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.
Timer	Generated by a timer within the processor. This allows the operating system to perform certain functions on a regular basis.
I/O	Generated by an I/O controller, to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions.
Hardware Failure	Generated by a failure such as power failure or memory parity error.

Interrupts


Fetch cycle
Execute cycle
Interrupt cycle
Interrupts disabled
START
Fetch next instruction
Execute instruction
Interrupts enabled
Check for interrupt; process interrupt
HALT

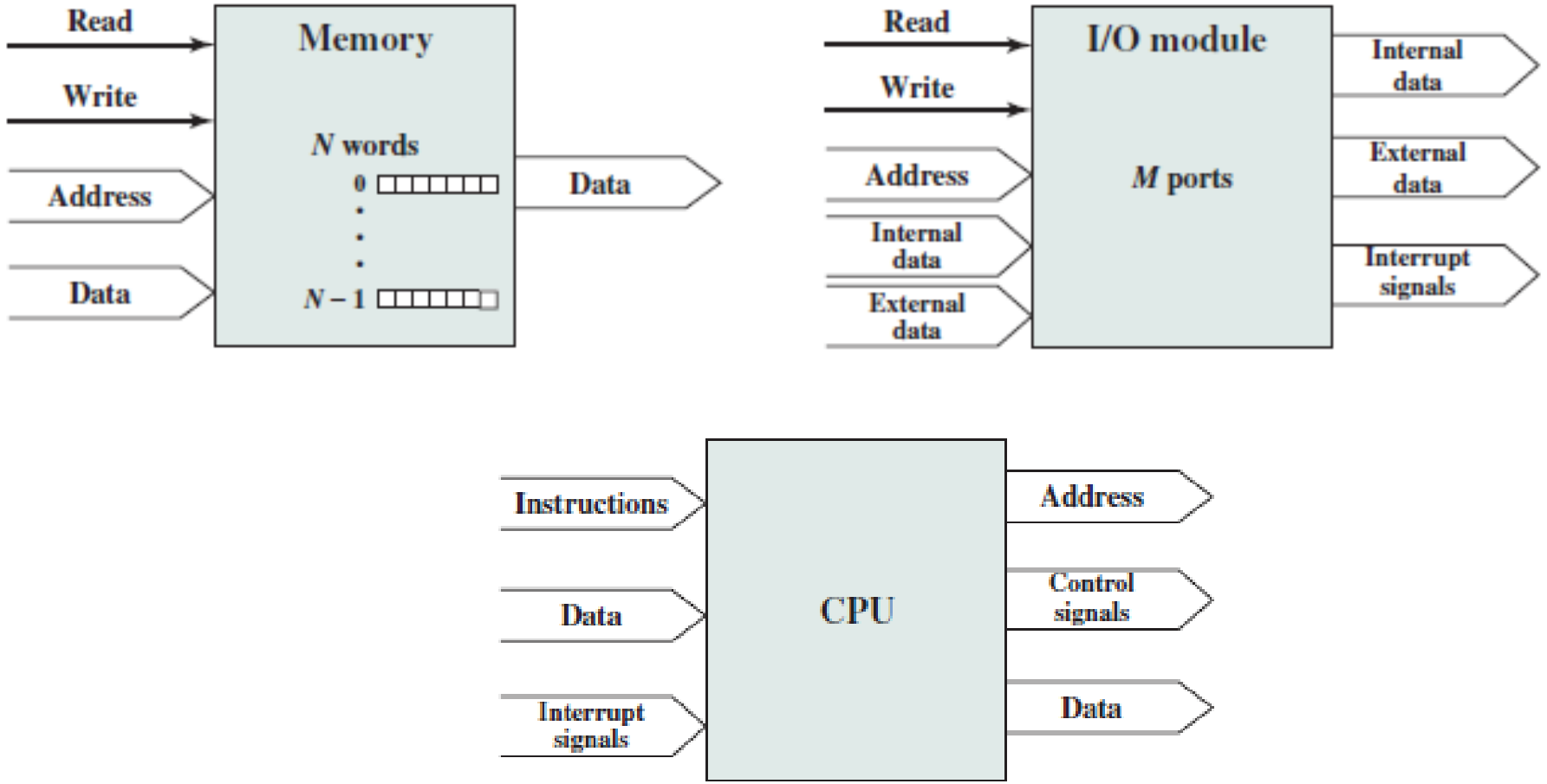
Interconnection Structures

- Computer consists of a set of components or modules of three basic types (processor, memory, I/O) that communicate with each other. The collection of paths connecting the these modules is called the interconnection structure.
- The most common are

  the **bus** and various multiple-bus structures

  point to point interconnection structures

Computer Modules



Data Transfer Types

- Memory to processor: The processor reads an instruction or a unit of data from memory.
- Processor to memory: The processor writes a unit of data to memory.
- I/O to processor: The processor reads data from an I/O device via an I/O module.
- Processor to I/O: The processor sends data to the I/O device.
- I/O to or from memory: An I/O module is allowed to exchange data directly with memory, without going through the processor, using direct memory access.

Bus Interconnection

- A bus is a communication pathway connecting two or more devices.
- A key characteristic of a bus is that it is a shared transmission medium.
- If two devices transmit during the same time period, their signals will overlap and become garbled.
- A bus consists of multiple communication pathways, or lines. Each line is capable of transmitting signals representing binary 1 and binary 0. For example, an 8-bit unit of data can be transmitted over eight bus lines.
- Computer systems contain different buses also called as System buses,
  - Data bus (32, 64, 128 bits)
  - Address bus (8, 16, 32 bits)
  - Control lines

Point-to-Point Interconnect

- At higher and higher data rates, it becomes increasingly difficult to perform the synchronization and arbitration functions in a timely fashion.
- Compared to the shared bus, the point-to-point interconnect has lower latency, higher data rate, and better scalability.
- Intel's QuickPath Interconnect (QPI), which was introduced in 2008.
  - Multiple direct connections:
  - Layered protocol architecture:
  - Packetized data transfer

PCI Express

- The peripheral component interconnect (PCI) is a popular high-bandwidth, processor-independent bus that can function as a peripheral bus.
- Compared with other common bus specifications, PCI delivers better system performance for high-speed I/O subsystems (e.g., graphic display adapters, network interface controllers, and disk controllers).
- PCI has been widely adopted and is finding increasing use in personal computer, workstation, and server systems.
- Accordingly, a new version, known as PCI Express (PCIe) has been developed.
- A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices, such as Gigabit Ethernet.