8087

- 8087 numeric data processor is also known as Math co-processor, Numeric processor extension and Floating point unit
- 1st math coprocessor designed by Intel to pair with 8086/8088
- Features:

Data types supported by 8087 - Binary integer
Real Numbers
Packed decimal number
Temporary real format

Follows IEEE Floating point standards
Very high processing speed

* Architecture

8087 Architecture is divided into 2 groups

i) Control Unit - handles all communication between the processor and memory (recieves and decodes instruction, reads and writes memory operands etc)

ii) Numeric Extension unit - handles all the numeric processor instructions (arithmetic, logical, transcendental etc)

\+ 8086 - 8087 Interfacing

There are mainly 7 chips in total

→ 8282 is for address
8 bit
$A_0 - A_{19}$ → Address Bus

→ 8286 is for data
8 bit
$D_0 - D_{15}$ → Data Bus (Bidirectional)

→ 8288 is bus controller
$\overline{MRDC}$ → Memory Read Command
$\overline{MWTC}$ → Memory write command
$\overline{AMWTC}$ → Advanced Memory write command
$\overline{IORC}$ → I/O Read Command
$\overline{IOWC}$ → I/O Write Command
$\overline{AIOWC}$ → Advanced I/O write Command

→ 8284 is Clock generator
CLK → shows time is passing
Reset
Ready
ALE (Address latch Enable)
SP (Slave program)
EP (Enable program)

→ 8259 is Programmable Interrupt Control (PIC)

In minimum mode, intercupt is directly given to 8086
MN / MX decides mode of processor
0 → Max mode 1 → Min mode

8086 → Master device
8087 → Slave device

When 8086 wants to give some task to 8087, it will check test pin
If test = 1, it will wait and if test = 0, task will be given

If tasks are continuously given, 8087 will stop the current task to do the recent task given by 8086 thereby creating garbage
But everytime test pin is not checked, only when instruction for 8087 is acknowledged
Escape bits = 1 0 1 1
When escape bit is encountered, 8086 will check for test pin

$\overline{RQ}$ / $\overline{GT}$ = Request and Grant
When 8087 wants to access the system bus, it will send request to 8086. 8086 will send grant signal

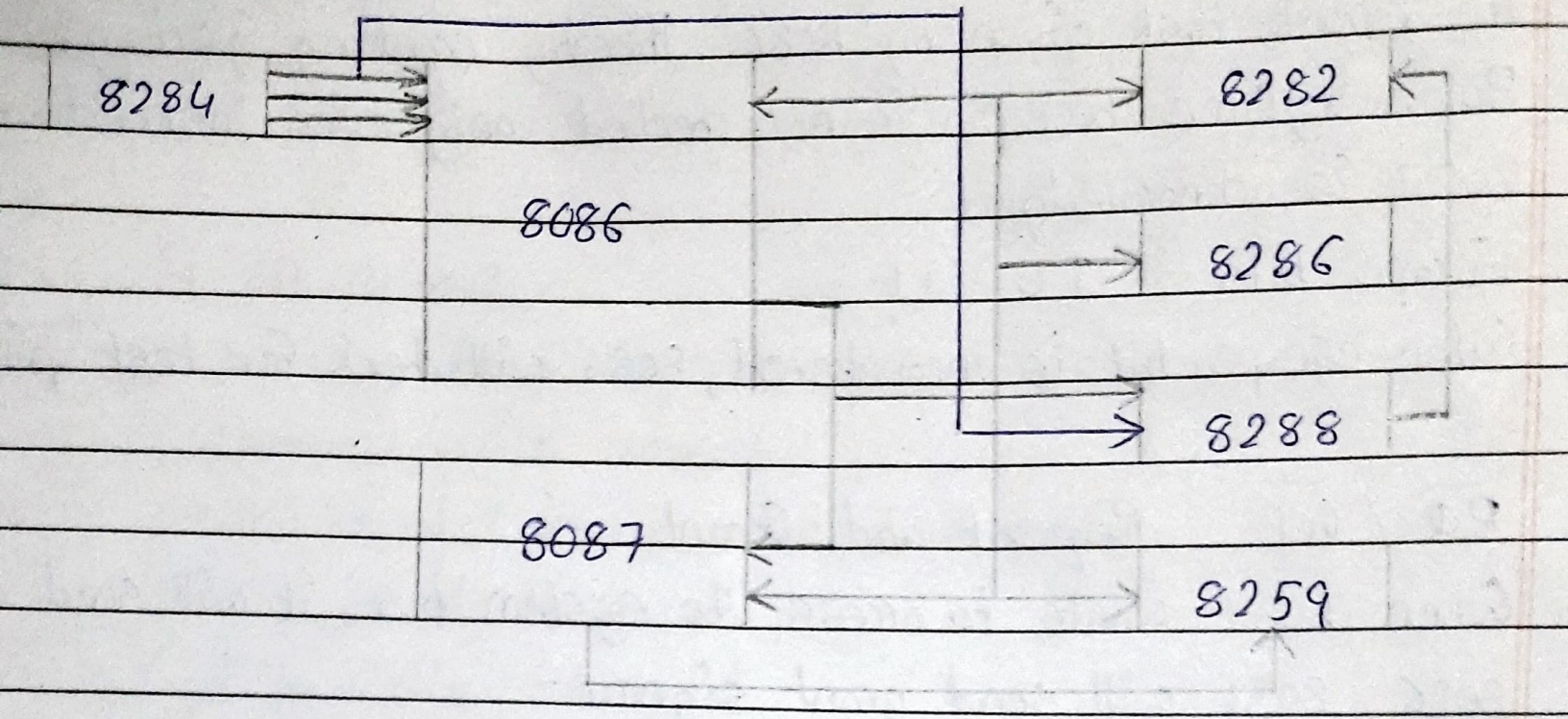
Status Signal

S_0	S_1	S_2	Queue Status
x	x	0	Unused
0	0	1	Unused
1	0	1	Memory Read
0	1	1	Memory Write
1	1	1	Passive

Queue Status Signal

QS_0	QS_1	Status
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

9BH is the opcode for 8088/86 ESCAPE instruction


8284
8282
8086
8286
8288
8087
8259

* Multiprocessor System

Multiple CPUs doing processing at the same time but they dont have their own memory element. They share a common memory. Peripheral and I/O devices are also shared

2 types:

1.) Symmetric Processing (Peer to Peer)

All processors have same amount of priviledge

Same amount of access on system busses

No one is dependent on other

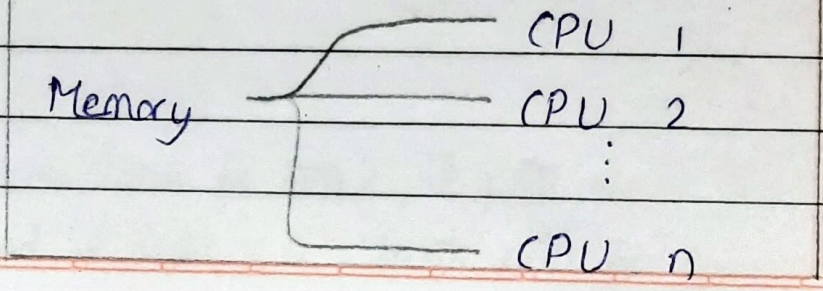
2.) Asymmetric Processing (Master - Slave)

Slave is dependent on master

Works on SIMD → single instruction

Multiple dataset

How is Multiprocessing accomplished?



* MMX Technology: MultiMedia eXtension
Multiple Math eXtension
Matrix Math eXtension

Step up multimedia and communications
Uses Parallelism and is compatible with existing intel system

Features:
- Single Instruction Multiple Data (SIMD) Technique
- 57 new instructions
- Eight 64 bit wide MMX registers
- 4 new data types: Packed byte (8 8-bit element)
Packed word (4 16-bit element)
Packed doubleword (2 32-bit element)
Quadword (1 64-bit element)

Detection:
Detection of MMX Technology on an Intel microprocessor is done by executing CPUID instruction and checking a set bit

Application:
Conditional select
Chroma keying
Vector dot product
Matrix multiply
24 bit color
Image dissolve

What is SIMD?
Single Instruction, Multiple Data (SIMD) units refer to hardware components that perform the same operation on multiple data operands concurrently.