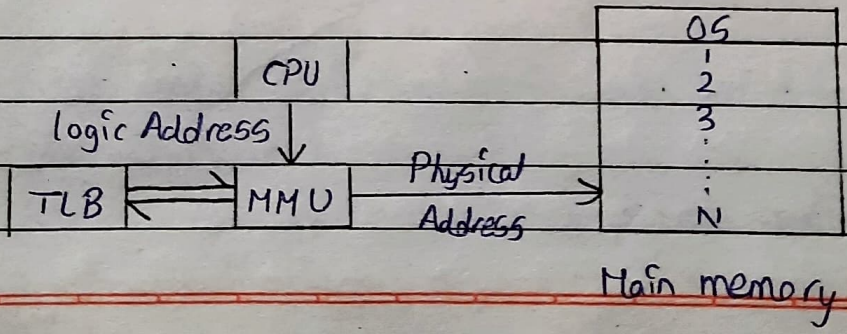
Pentium

32 bit microprocessor
8 memory banks
Virtual memory - Hard disk upto 64 TB
64 bit Data bus
32 bit Address bus
Physical memory - RAM 4 GB
Operating frequency 66 - 99 MHz
5 stage pipeline - 2 pipes
On chip floating point unit
On chip L1 cache
Branch prediction logic
2 way super scalar - u and v pipes

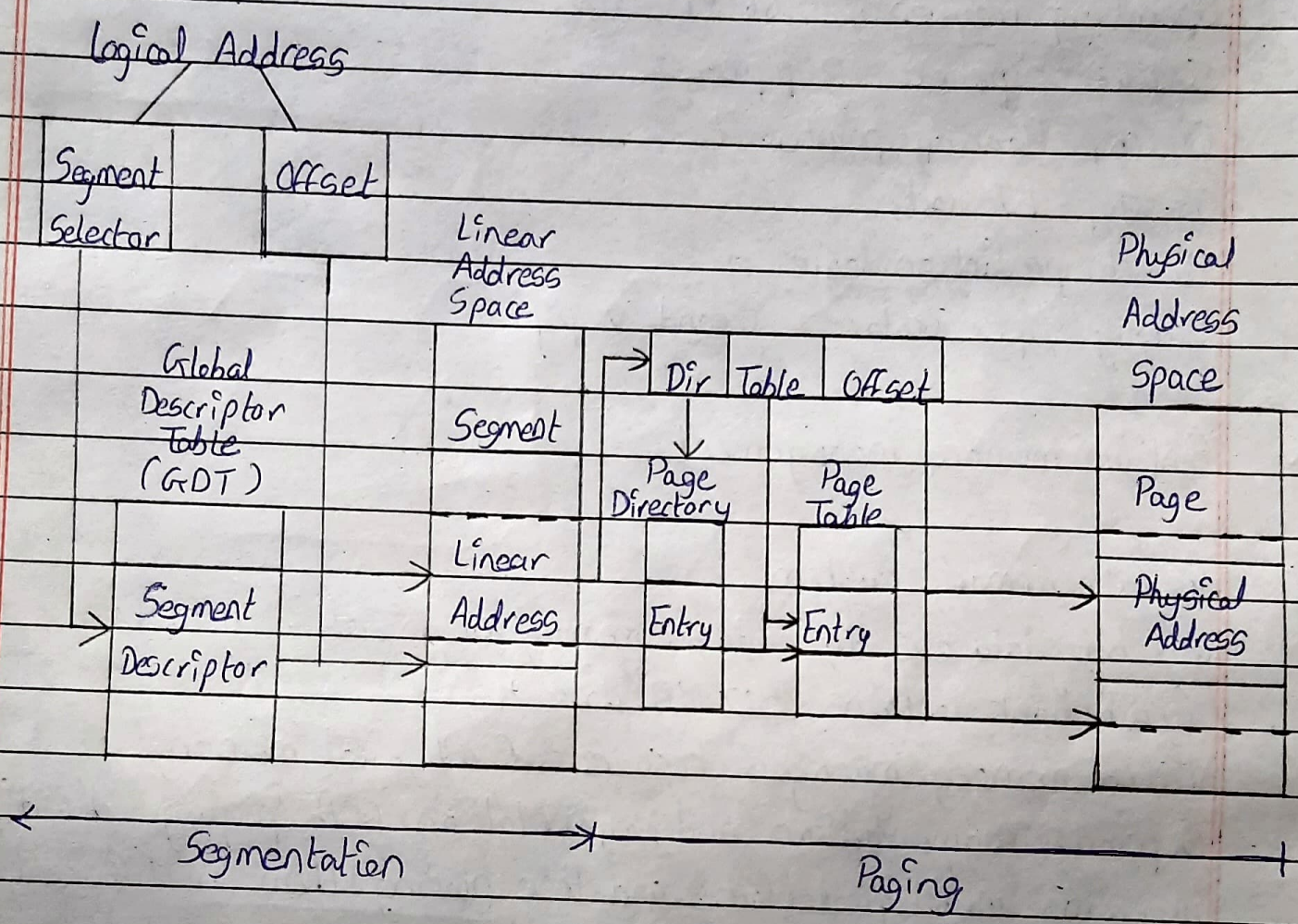
Pentium memory management

- 4 GB memory system
- 64 bit data bus to address memory organized in 8 banks (each bank contains 512 MB data)
- Virtual memory manages resource of Physical memory
- Supports segmentation and segmentation with paging - dividing programs into logical blocks and then placing them in different memory areas
- Memory protection : Protected mode (PM) allows multi tasking
  : Real mode (RM)

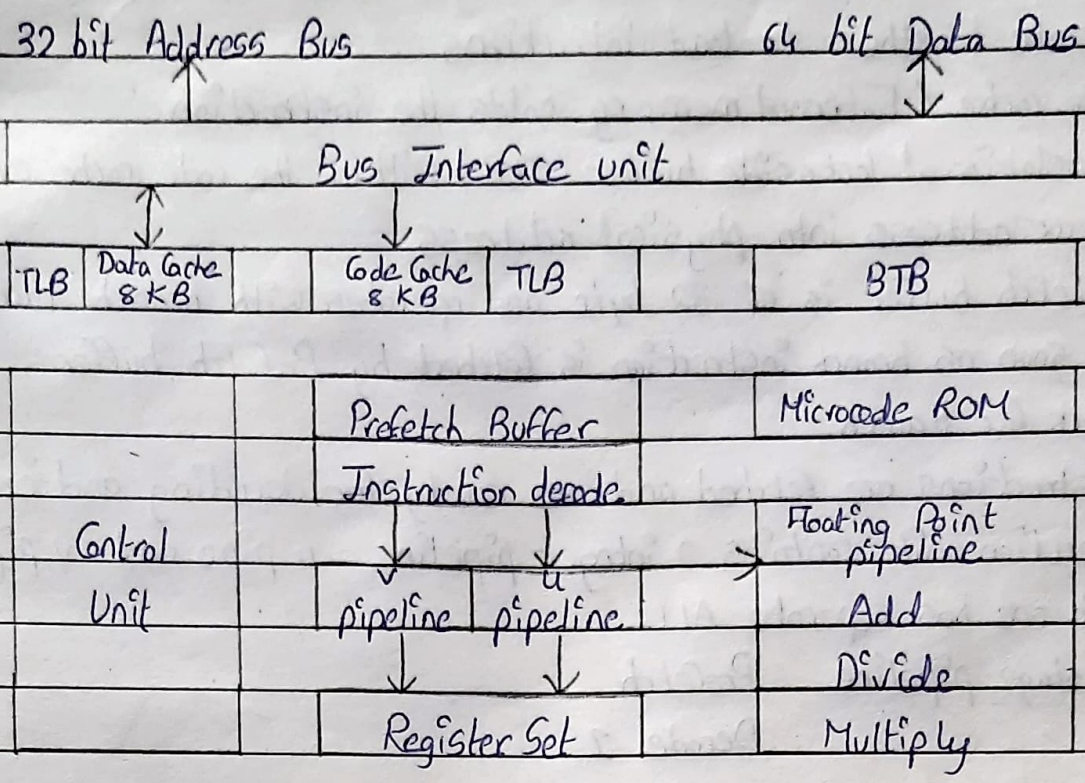


Memory management unit (MMU) / Paged memory management unit (PMMU) is a hardware component liable in handling different accesses to memory requested by CPU

Functions : Virtual memory management
Memory protection
Cache control
Bus arbitration
Bank switching



Architecture:



Various Fonctional units : Bus unit
Paging unit
Control ROM
Prefetch buffer
Execution unit with 2 pipeline (u and v)
Code cache
Data cache
Instruction decode
Branch target buffer
Dual processing logic
Interrupt controller

Bus unit sends control signal and fetches code and data from external memory and IO devices
External data bus size is 64 bit through which read and write cycles can be achieved.

- Paging unit provides optional extensions of 2-4 Mb page size
- Execution unit, Code cache, Branch target buffer and Prefetch buffers operate together to load intructions
- Code cache / External memory holds the instruction
- Translational lookaside buffer (TLB) within the code cache converts linear address into physical address
- Prefetch buffer is of 32 byte and operates with branch target buffer
- As soon as branch instruction is fetched by Prefetch buffer, BTB will check for branch
- Instructions are fetched and are ready for decoding and execution
- Execution unit contains 2 integer pipeline - u pipe and v pipe and each one has seperate ALU
- 5 stage pipeline
  - Prefetch
  - Decode 1
  - Decode 2
  - Execute
  - Writeback.
- u pipe executes all integer and floating point instruction
- v pipe executes simple integer and some floating point instruction
- Instruction fetch reads the instruction one at a time and stores them in the instruction queue
- If 2 instructions are independent of each other then u pipe and v pipe are assigned instructions individually so that execution can occur simultaneously
- If instructions are dependent then both are assigned to u pipe for execution
- Controlling of operations is provided by control ROM that has microcode within it and directly controls u pipe and v pipe
- Both data and code cache is organized in 2 way set cache
- Each cache has 128 sets and each set has 2 lines which are 32 bytes
- LRU mechanism handles cache replacement
- Code cache forms connection with prefetch buffer by a bus of 256 bit

- Data cache has 2 ports that are used simultaneously deal with 2 data references
- On-chip Advanced programmable interrupt controller manages interrupt and offers 8259A compatibility

- Assembler

Source Code (Assembly language) → Assembler → Object Code (Machine language)

Assembler is a program for converting instructions written in low-level assembly code into relocate machine code and generating along information for the loader
It generates instructions by evaluating mnemonics (symbols) in operation field and find the value of symbol and literals to produce machine code
2 types:

i) Single pass assembler: If assembler do all this work in one scan
ii) Multiple pass assembler: If assembler do all this work in multiple sca

Assembler divide tasks in 2 passes:

- Pass 1
Define symbols and literals
Keep track of location counter
Process pseudo operation

- Pass 2
Generate object code
Generate data for literals

- Debugger or Debugging Tool

- Software used to test and find bugs (errors) in other software
- Debuggers may use instruction set simulators, rather than running a program directly on the processor to achieve a higher level of control over its execution
- When a program crashes, debuggers show the position of errors in target program
- Most debuggers runs program in a step by step mode
- They can modify state of programs while they are running
- They can be CLI based and GUI based
- Features:
  Single stepping
  Break
  Tracking value of variables

* Bit slice processor

A bit slice processor in computer architecture is constructed from processor modules of smaller bit width
Each of these processes one bit field of an operand
Each processor module chip typically includes ALU and few registers

* Signal processing Processors

Digital signal in → Digital Processing → Digital signal out

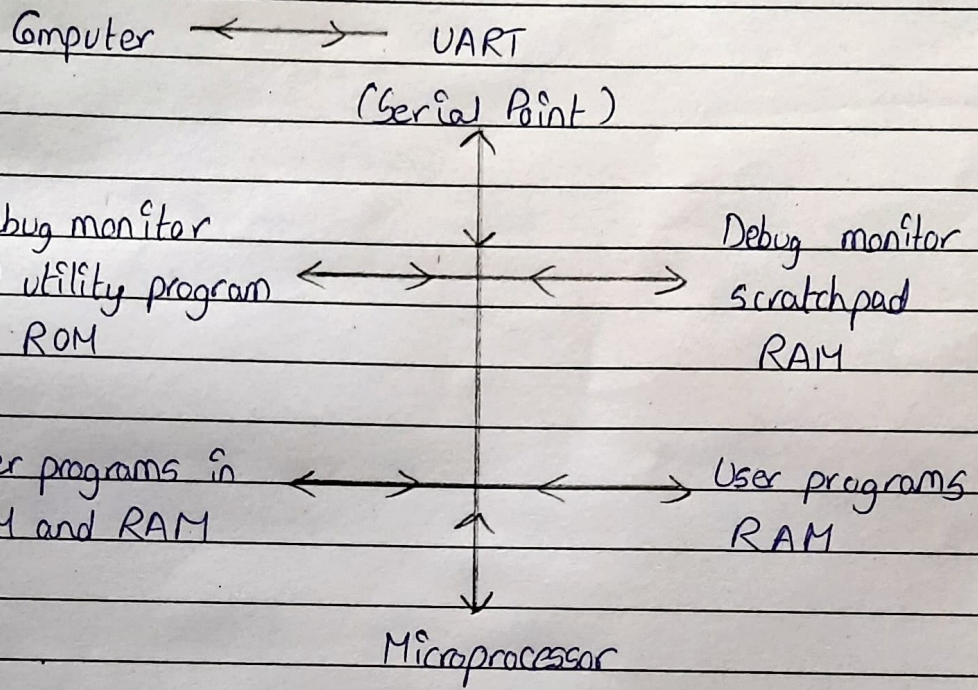
Analog signal in → ADC → Digital Signal Processing → DAC → Analog signal out

Digital Signal Processor (DSP)

Special type of microprocessor which is fabricated on metal oxide semiconductor integrated circuit

Used in Digital image processing, Telecommunication, Audio, Speech, Sonar, Radar

* Introduction to Development tools : Microprocessor Development System (MDS)



* Introduction to Development tools : Logic Analyzer

- Used for
  Debug and verify digital system operation
  Trace and corelate many digital signals
  Detect and analyse timing violations and transient on buses
  Trace embedded software execution
- 3 types : Portable
  PC based
  Modular

* Introduction to Development tools : In-circuit emulator

ICE (In circuit emulator) provides a window into the embedded system

Programmer uses emulator to load programs into embedded system, run them, view and change data used by system's software