Navrachana University

TEACHING PLAN

Computer Organization and Architecture (CS307)

Faculty	Gauravkumarsingh Gaharwar			Division	
Contact	gauravsinghg@nuv.ac.in	Office Hours	Friday: 03.00 pm to 04.00 pm		
School	School of Engineering and Technology				
Program	BTech(CSE)				
Semester	Spring			Credits	3
Academic Year	2022-23				
Lecture time & Weekdays	Monday: 03.00 pm to 04.00 pm Tuesday: 02.00 pm to 03.00 pm Wednesday: 10.00 am to 11.00 am Wednesday: 11.00 am to 12.00 noon Wednesday: 02.00 pm to 03.00 pm Wednesday: 03.00 pm to 04.00 pm Friday: 10.00 am to 11.00 am	Location	506 511 506 506 507 511 507/502		
Pre-requisites	CSE 139: Introduction to computers and programming				
Course Description	This course teaches the Von-Neumann Architecture of computer system in detail. Students learn about internal components and peripherals of a computer system. Advanced topics such as parallel processing, multicore computers and graphic processing units are taught in this course.				
Course Abstract *					
Course Objectives	1. To teach basic organization of computer system. 2. To understand central processing unit. 3. Study of pipelining and vector processing. 4. Study of parallel processing. 5. Study of Control unit operation.				
Learning Outcomes	*After completing this course, student will be able to* *1. Comprehend organization of computer system and assembling of a computer* *2. To understand the Central Processing Unit.* *3. Identify performance issues and Design issues in parallel processing* 4. *Understand when to use a GPU co-processor*				
Typology of Course	Theory / Tutorial				
Course Outline (Units, Hours, Textbooks, Reference Books)	**Unit 1: INTRODUCTION TO COMPUTER SYSTEM** Computer organization and architecture, evolution, brief history, embedded systems, ARM architecture, Performance issues, Ahmdahl's Law, benchmarks and specification, computer components, functions, interconnection structures, Bus interconnection, PCI, Computer memory, cache memory, Internal memory, external memory, I/O modules, DMA, DCA, operating systems, Operating system support, Number systems, Computer Arithmetic, Positional Arithmetic, Binary system, Hexadecimal system, Digital Logic: Combinational circuits, gates, sequential circuits. **Unit 2: THE CENTRAL PROCESSING UNIT** Instruction sets: Characteristics and functions, types of operands, types of operations, intel x86. Instruction sets: Addressing modes and formats, Addressing mode, assembly				

	language. Processor structure and function: processor organization, register organization, ARM processor **Unit 3: PIPELINE AND VECTOR PROCESSING** Reduced instruction set computers: RISC pipelining, MIPS, SPARC, RISC v/s CISC, compiler based register organization. Instruction Level Parallelism and Superscalar processors: Design Issues, intel core microarchitecture, ARM Cortex. Vector Processing, Array Processors **Unit 4: PARALLEL ORGANIZATION** Parallel processing: Multiple processor organization, symmetric multiprocessor, Multithreading and chip microprocessors, clusters, non-uniform memory access, cloud computing Multicore computers: Hardware and software performance issues, multicore organization, heterogeneous multicore organization General purpose graphic processing unit: GPU v/s CPU, CUDA basics, intel generation 8 GPU. **Unit 5: THE CONTROL UNIT** Control Unit operation: Micro operations, hardwired implementation Microprogrammed control: Microinstruction sequencing, microinstruction execution
Pedagogy	Explaining each topic with and example and then allow students to solve similar type of problems
Expectations from Students *	Students should attend 100% classes Timely submission of assignments
Assessment / Evaluation	Class Tests, Class Participation, Assignment & Viva
Attendance Policy	The University expects 100% attendance, but a minimum 80% attendance is mandatory in each course to be eligible to appear for the end-semester examination of the course. a) Dean/Head of the School can recommend the attendance upto 15% in the course or courses for representing the university at any regional, national or international competition in the field of academics or sports or due to long duration ill-health or other emergency situations. Provost based on the case submitted by Registrar's Office with recommendation of the Dean/School head will take decision. b) For beyond 15% in any genuine cases, the decision to condone the attendance will be taken by the Provost on merits of the case. c) Documentary evidence is required to receive excusable absence and should be submitted to the Provost with the recommendation of the Dean/Head of the School. d) A student not meeting the attendance requirements in a course will not be allowed to appear for the regular end semester examination and will be awarded 'F' grade in that course. However, she/he may be permitted for re-examination. e) A student with very low attendance i.e. less than 65% in all courses during the current semester may not be allowed to appear for regular end semester examination. She/he will have to re-register all courses during the next academic year. f) Students playing individual sports or team sports at regional/national/international level with authorized sports body of the respective games will be exempted from attendance during match/competition days as well as during practice session/camps on producing relevant documents.
Project / Assignment Details *	
Course Material	**Reference Books:**

	1. Computer Organization and Architecture: Designing for Performance (10th Edition), William Stallings, Prentice Hall Pearson. 2. M. Morris Mano, Computer System Architecture, Pearson 3. Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization, Sixth Edition, PHI 4. M. Murdocca & V. Heuring, Computer Architecture & Organization, WILEY 5. John Hayes, Computer Architecture and Organization, McGrawHill
Additional Information *	

* These are optional fields.

Session Plan

Topic Title	Session No.	Topic & Subtopic Details	Readings, Cases, etc.	Activities*	Important Dates
Unit-I **INTRODUCTION TO COMPUTER SYSTEM**	L-1	Computer organization and architecture	Textbook – 1		
	L-2	evolution, brief history, embedded systems	Textbook – 1		
	L-3	ARM architecture, Performance issues	Textbook – 1		
	L-4	Ahmdahl's Law, benchmarks and specification	Textbook – 1		
	L-5	computer components, functions	Textbook - 1		
	L-6	interconnection structures, Bus interconnection	Textbook – 1		
	L-7	PCI	Textbook – 1		
	L-8	Computer memory, cache memory	Textbook - 1		
	L-9	Internal memory, external memory	Textbook – 1		
	L-10	I/O modules, DMA, DCA	Textbook – 1		
	L-11	operating systems, Operating system support	Textbook - 1		
	L-12	Number systems, Computer Arithmetic	Textbook – 2		
	L-13	Positional Arithmetic, Binary system, Hexadecimal system	Textbook – 2		
	L-14	Digital Logic: Combinational circuits	Textbook – 2		
	L-15	gates, sequential circuits	Textbook – 2		
Unit-II **THE CENTRAL PROCESSING UNIT**	L-16	Instruction sets: Characteristics and functions	Textbook - 1		
	L-17	types of operands	Textbook - 1		
	L-18	types of operations, intel x86.	Textbook - 1		
	L-19	Instruction sets: Addressing modes and formats	Textbook - 1		
	L-20	Addressing mode, assembly language.	Textbook - 1		
	L-21	Processor structure and function: processor organization	Textbook - 1		
	L-22	register organization, ARM processor	Textbook - 1		
Unit-III	L-23	Reduced instruction set	Textbook - 1		

PIPELINE AND VECTOR PROCESSING		computers			
	L-24	RISC pipelining, MIPS, SPARC	Textbook - 1		
	L-25	RISC v/s CISC, compiler based register organization.	Textbook - 1		
	L-26	Instruction Level Parallelism and	Textbook - 1		
	L-27	Superscalar processors: Design Issues	Textbook - 1		
	L-28	intel core microarchitecture, ARM Cortex	Textbook - 1		
	L-29	Vector Processing, Array Processors	Textbook - 1		
Unit-IV **PARALLEL ORGANIZATION**	L-30	Parallel processing: Multiple processor organization	Textbook - 1		
	L-31	symmetric multiprocessor, Multithreading and chip microprocessors	Textbook - 1		
	L-32	clusters, non-uniform memory access	Textbook - 1		
	L-33	cloud computing	Textbook - 1		
	L-34	Multicore computers: Hardware and software performance issues	Textbook - 1		
	L-35	multicore organization, heterogeneous multicore organization	Textbook - 1		
	L-36	General purpose graphic processing unit: GPU v/s CPU	Textbook - 1		
	L-37	CUDA basics, intel generation 8 GPU	Textbook - 1		
Unit-V **THE CONTROL UNIT**	L-38	Control Unit operation: Micro operations	Textbook - 1		
	L-39	hardwired implementation	Textbook - 1		
	L-40	Microprogrammed control	Textbook - 1		
	L-41	Microinstruction sequencing	Textbook - 1		
	L-42	Microinstruction sequencing	Textbook - 1		
	L-43	microinstruction execution	Textbook - 1		
	L-44	microinstruction execution	Textbook - 1		
	L-45	Viva	Textbook - 1		