Lab Assignment – 10

Counters

Objective:

- Realize a mod-8 ripple counter using JK flip-flops.
- Realize a mod-5 ripple counter using JK flip-flops.
- Realize a mod-8 synchronous counter using JK flip-flops.
- Realize a mod-5 synchronous counter using JK flip-flops.

Theory:

Ripple Counters and Synchronous Counters are of two types:

- Binary
- Non Binary

A binary counter counts N states where $N=2^k$ that is N can be expressed as a power of 2. However, in 'Non-Binary' counters the number of states is not the power of 2. A ripple counter is asynchronous in nature and thus all flip-flops do not use the same clock. A binary ripple counter can be made with JK flip-flops operating in toggle mode (J=K=1). A binary ripple counter can be made with negative edge triggered JK flip-flops where output Q of the i^{th} flip-flop is fed as the clock to the $i+1^{th}$ flip-flop. For ripple down counter Q' is fed as the clock to the next flip flop. For, non-binary ripple counters a feedback circuit is used and hence they are unpopular because there can be glitch due to gate delay. In case of synchronous counters, the same clock is fed to all the flip-flops. For mod-K synchronous counter the excitation table for JK flip-flop is found out, the state table is written and then the corresponding inputs like J_o, K_o, J_1, K_1, etc. are found out in terms of outputs that is Q_o, Q_o', Q_1, Q_1', etc. by simplifying Karnaugh Maps. For a mod-K counter $2^N >= K$, N flip-flops are used. N is the least integer satisfying the condition.

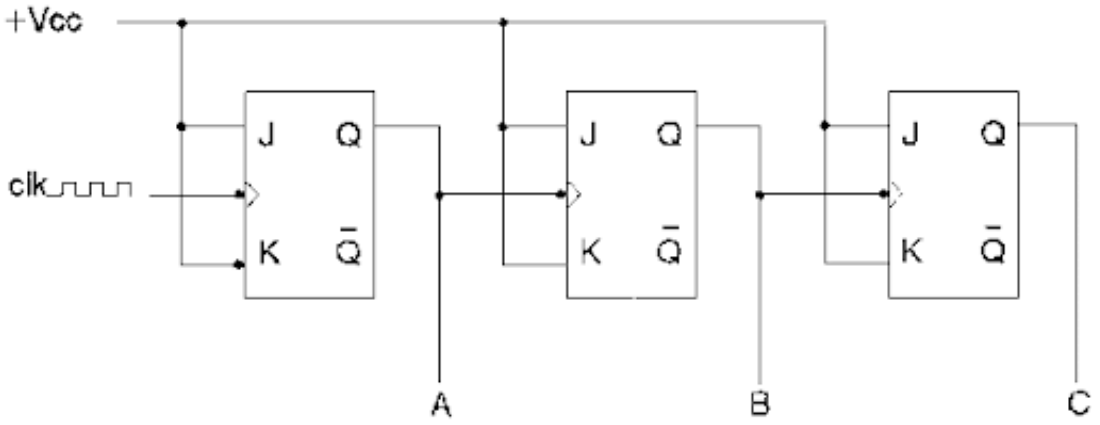
Components Required:

- 7476 ICs (dual JK flip-flops)
- AND,NOT and NAND gates
- Pulser
- Logical displays(LED)
- Logical Gates

1. To realize a mod-8 Ripple Counter using JK Flip-Flops:

To design a mod-8 ripple counter ($2^3 = 8$) we need 3 JK flip-flops. The flip-flops are operated in 'toggle' mode that is J=K=1 for all flip-flops. Ripple counter is asynchronous the flip-flops do not have same clock. The output of the flip-flop is fed as the clock to the next flip-flop. A master reset line is kept in order to reset all flip-flops. The outputs can be fed to a decoder to get the counter value in decimal.

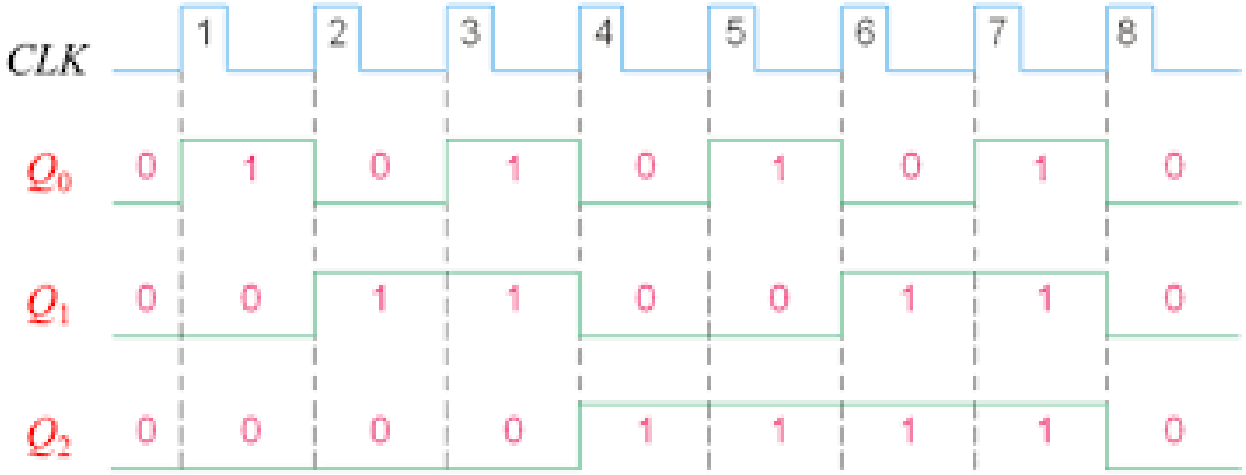
BLOCK Diagram:



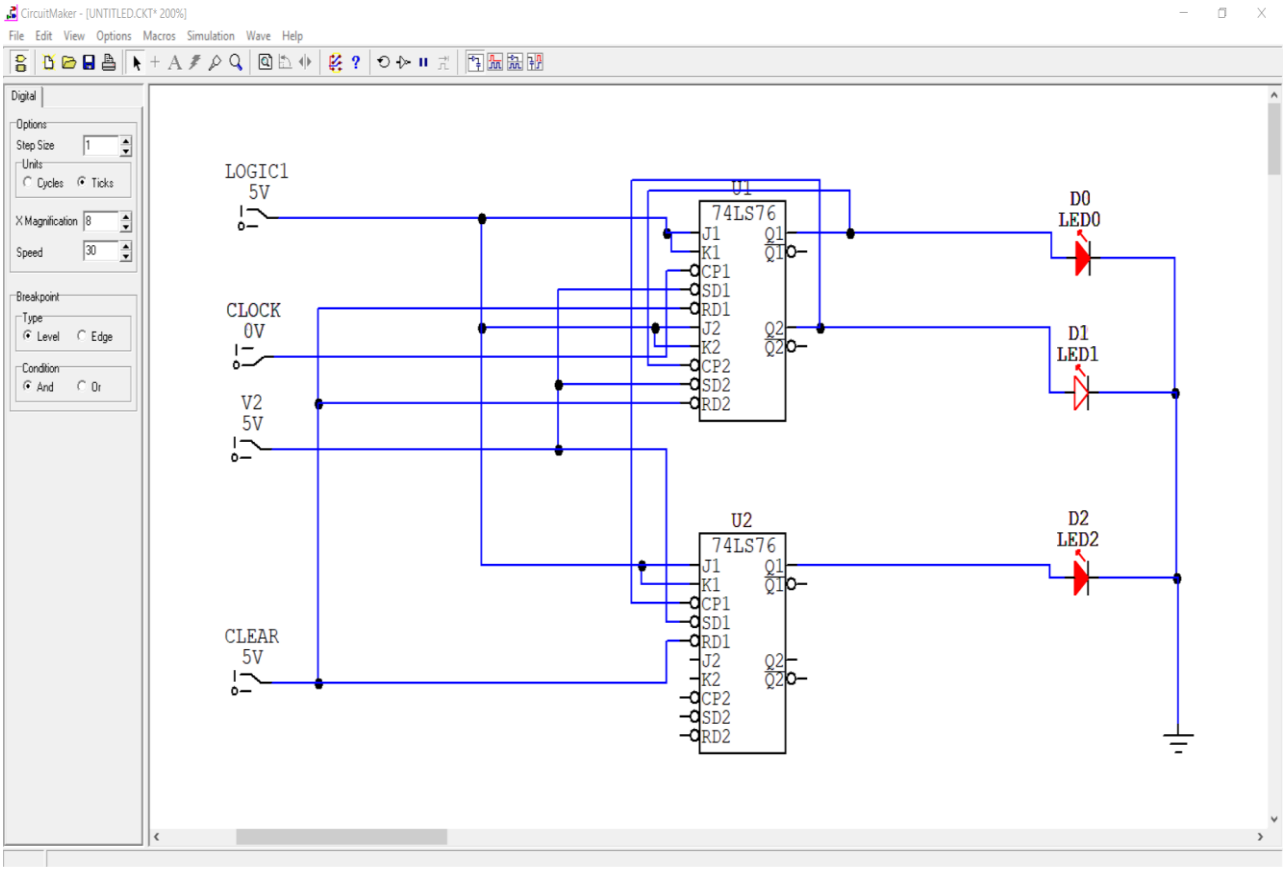
State Table:

State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
0	0	0	0

Timing Diagram:



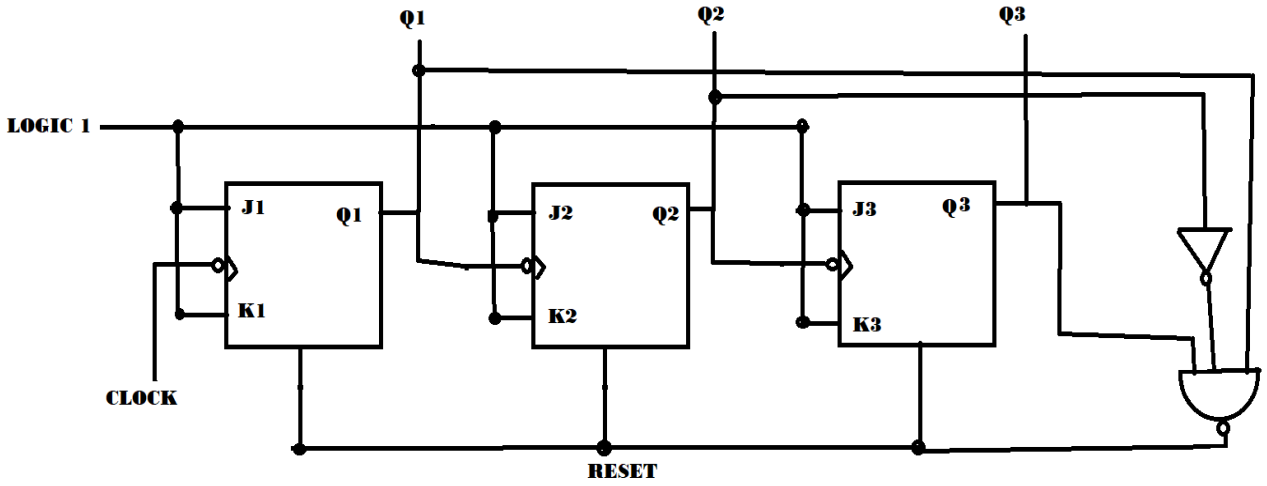
Simulation:



2. To realize a mod-5 Ripple Counter using JK Flip-Flops:

The circuit remains almost same. However here we use a feedback in order to count only 5 states [i.e., 0, 2, 3 and 4]. As soon as the counter state turns 5 i.e., (Q_2 =1, Q_1=0, Q_0=1) we use a NAND Gate to reset all the flip-flops. To accommodate the master-reset line we can AND it with the feedback since the reset inputs are active low. However, in this circuit there will be a glitch due to the propagation delay of the NAND and AND gates, and the state 5 i.e., (101) will be detected for a very short time. A decoder can be used to convert the output to decimal. The active-low 'preset' inputs are used to forcefully reset all flip flops.

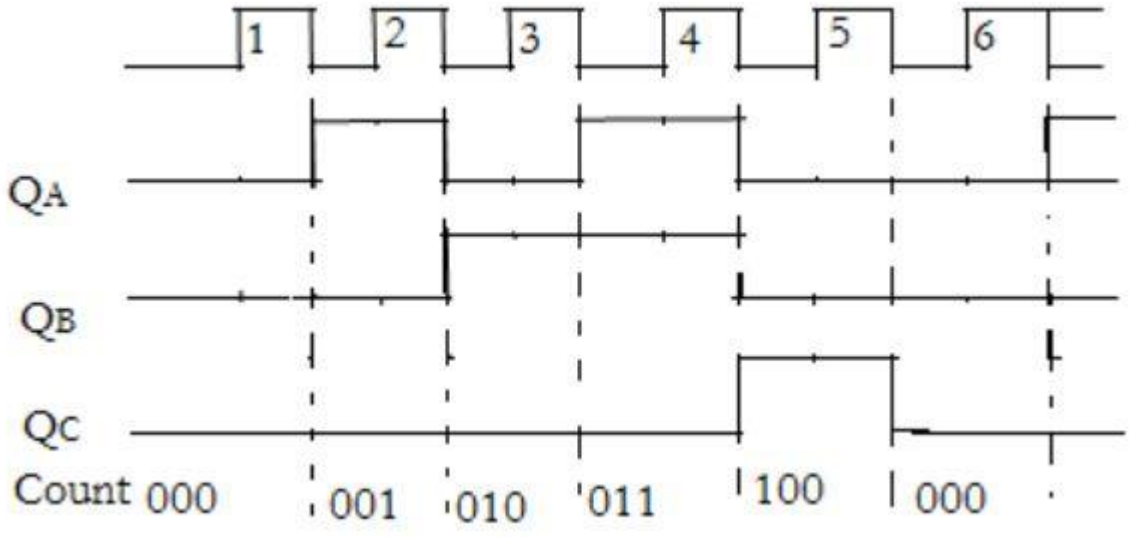
Circuit Diagram:



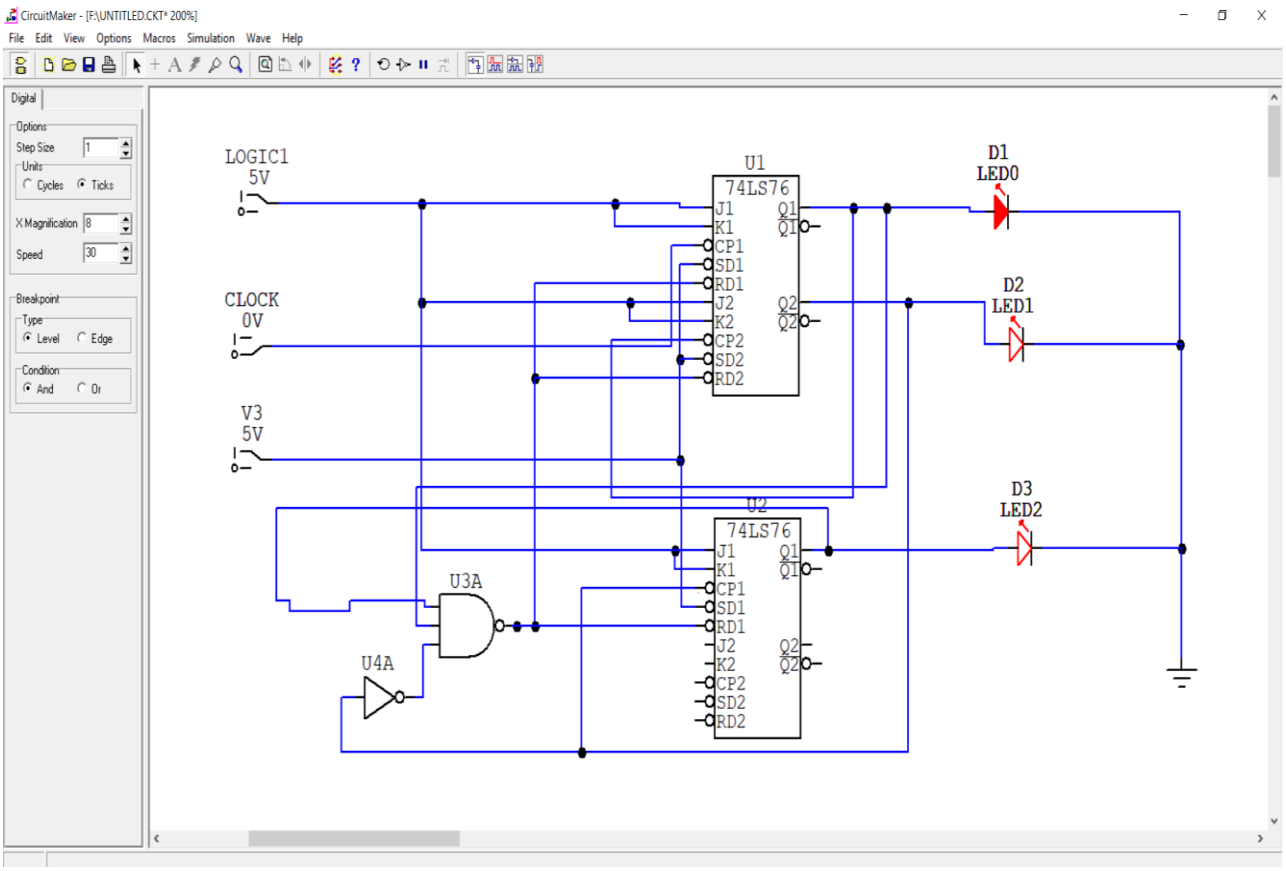
State Table:

State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
0	0	0	0

Timing Diagram:



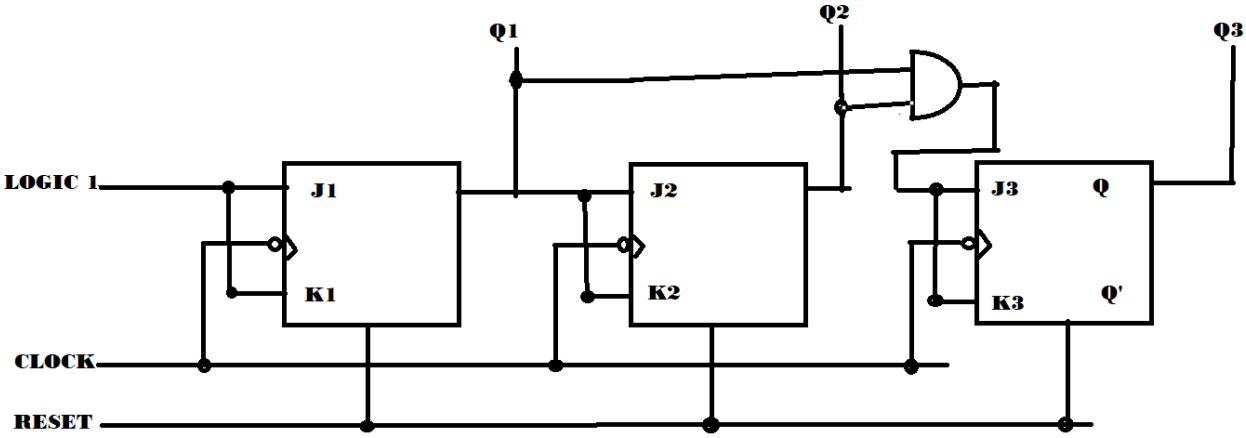
Simulation:



3. To realize a mod-8 Synchronous Counter using JK Flip-Flops:

Synchronous centers are those in which the same clock is fed yo all the flip flops. Mod 8 is a binary counter as 2^3 is 8 and hence requires 3 flip flops. First excitation table is written and then state transition table has to be found out. The inputs of flip-flops J0, J1, K0, K1 is then found accordingly to give the output of Q0, Q1, etc. by simplifying K-Maps. In general the output and input of a particular flip flop are passed through AND gates and fed as the input of the next Flip Flop.

Block Diagram:



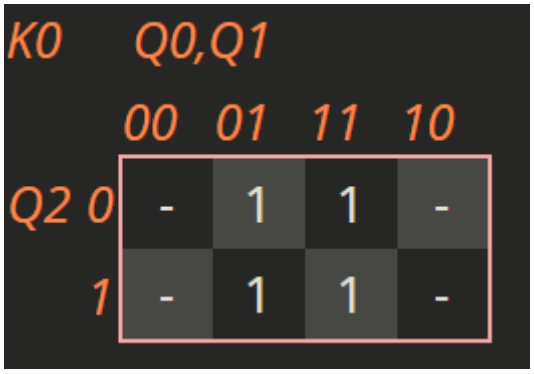
Excitation Table:

CLK	Qn	Qn+1	J	K
↑	0	0	0	X
↑	0	1	1	X
↑	1	0	X	1
↑	1	1	X	0

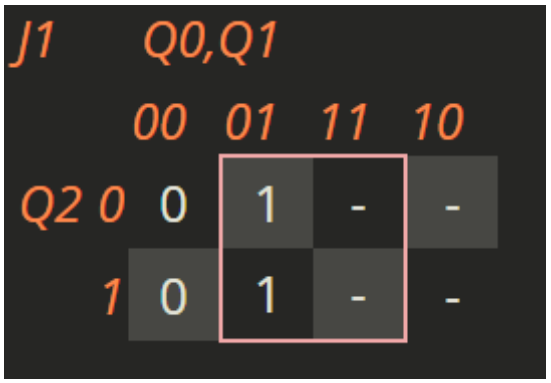
State Transition Table:

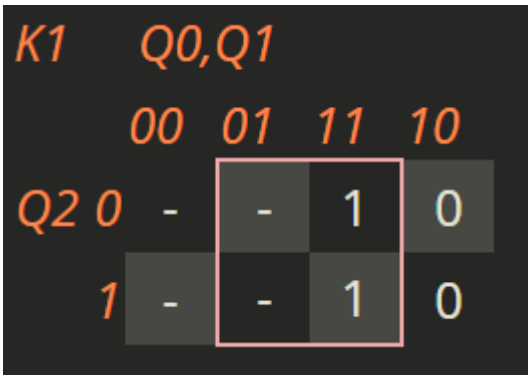
State	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	X	0	X	1	X
1	0	0	1	0	X	1	X	X	1
2	0	1	0	0	X	X	0	1	X
3	0	1	1	1	X	X	1	X	1
4	1	0	0	X	0	0	X	1	X
5	1	0	1	X	0	1	X	X	1
6	1	1	0	X	0	X	0	1	X
7	1	1	1	X	1	X	1	X	1
0	0	0	0	0	X	0	X	1	X

Karnaugh Maps:

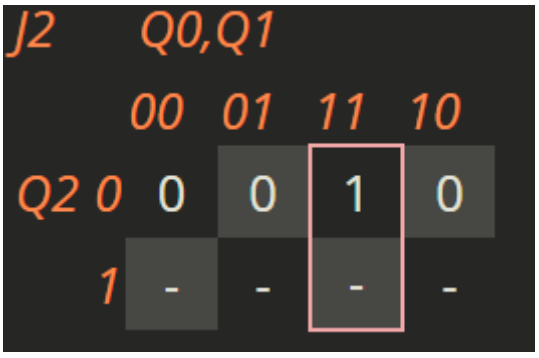


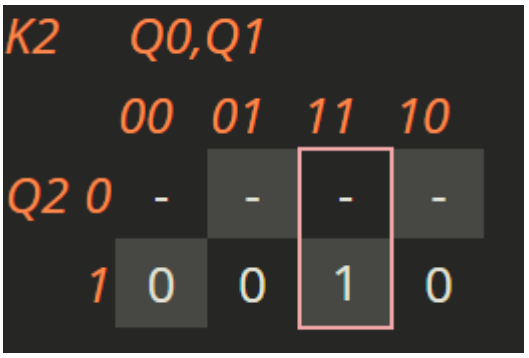
J0=1 K0=1





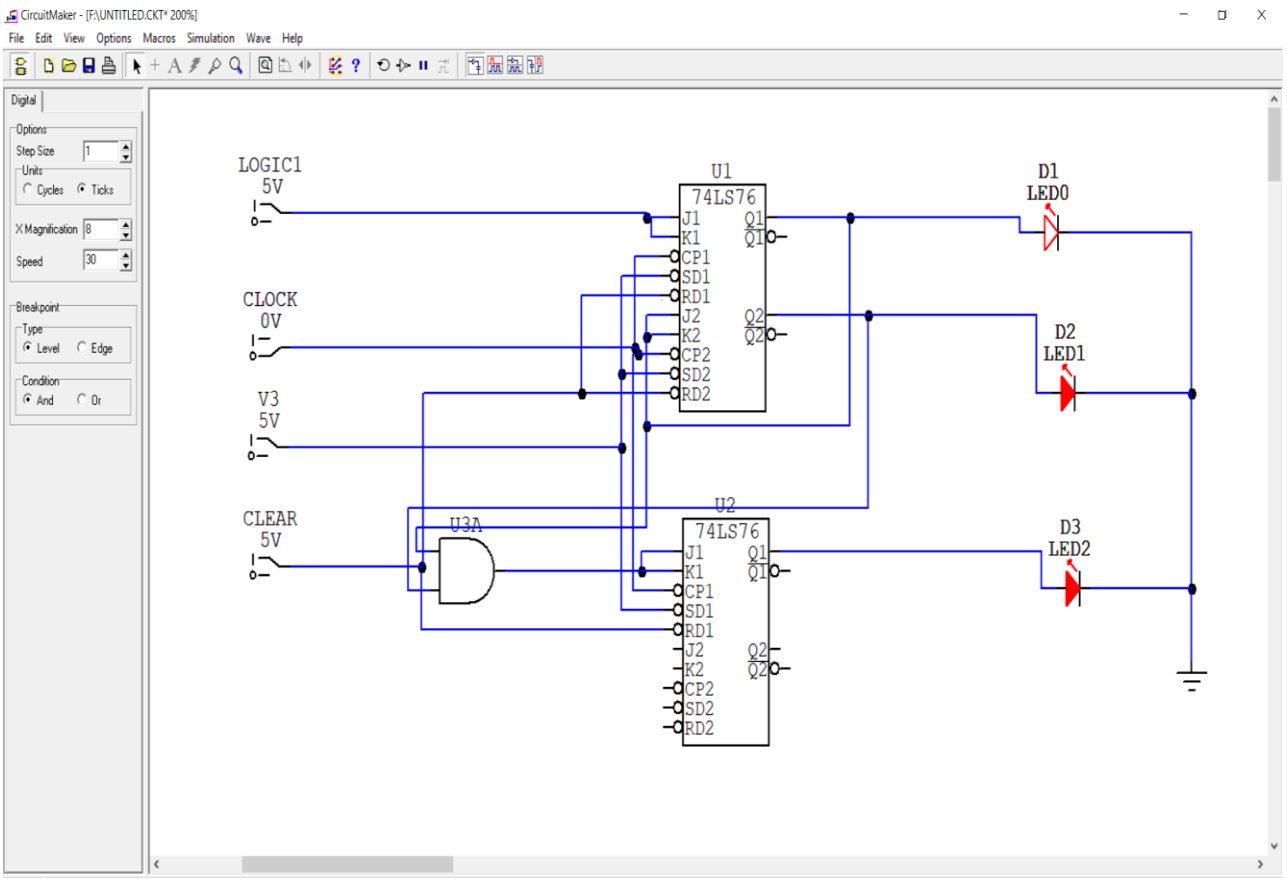
J1=Q_0 K1=Q_0





J2=Q_1Q_0 K2=Q_1Q_0

Simulation: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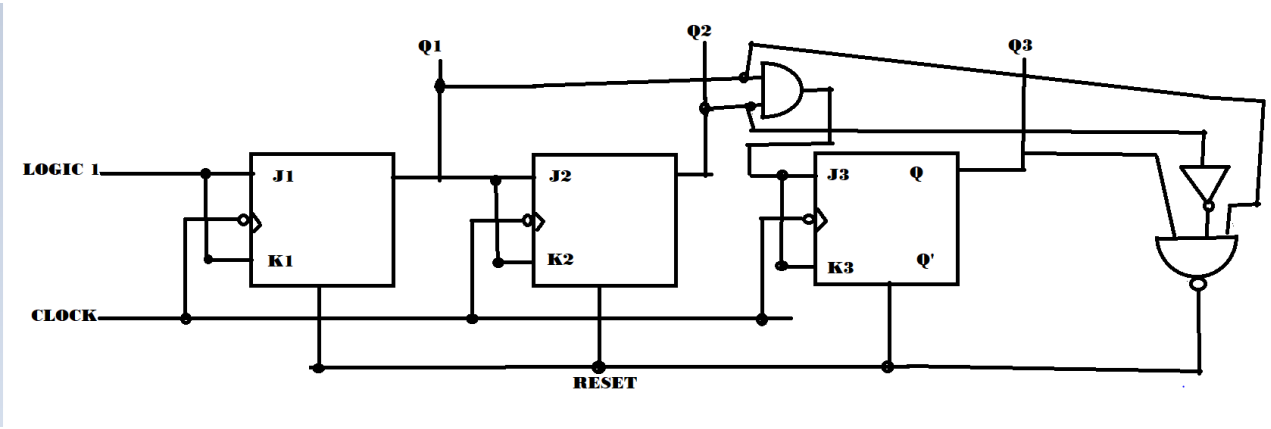
4. To realize a mod-5 Synchronous Counter using JK Flip-Flops:

Designing a mod 5 Synchronous Counter is similar to a mod 5 ripple counter. As 2^3 > 5, 3 JK flip flops are to be used. In such Non Binary Counters, Lockout is a possibility. When a counter is in working state, because of the noise spikes counter may find itself in some unused state (invalid state). Subsequent clock pulses may cause this counter to move from one unused state to other, resulting in counter never returning to the valid state. And the counter becomes useless. This condition is technically termed as Lockout. In such cases the counter has to be reset.

Circuit Diagram:



Excitation Table:

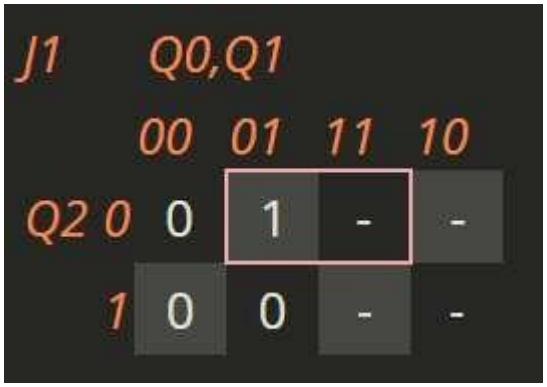
CLK	Qn	Qn+1	J	K
↑	0	0	0	X
↑	0	1	1	X
↑	1	0	X	1
↑	1	1	X	0

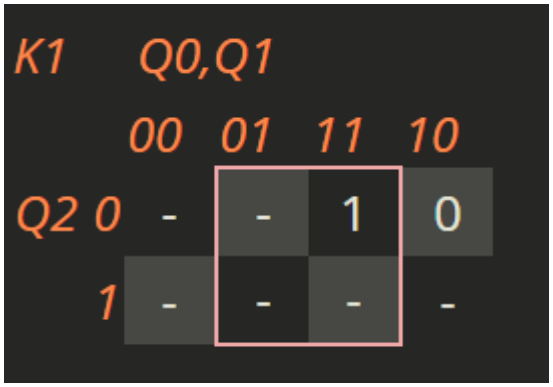
State Transition Table:

State	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	X	0	X	1	X
1	0	0	1	0	X	1	X	X	1
2	0	1	0	0	X	X	0	1	X
3	0	1	1	1	X	X	1	X	1
4	1	0	0	X	0	0	X	1	X
0	0	0	0	0	X	0	X	1	X
	1	0	1	X	1	0	X	X	1
0	0	0	0						
	1	1	0	0	X	X	1	X	1
0	0	0	0						
0	1 0	1 0	1 0	X	1	X	1	X	1

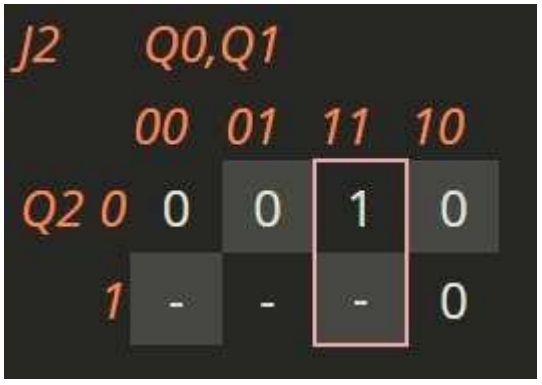
Karnaugh Maps:

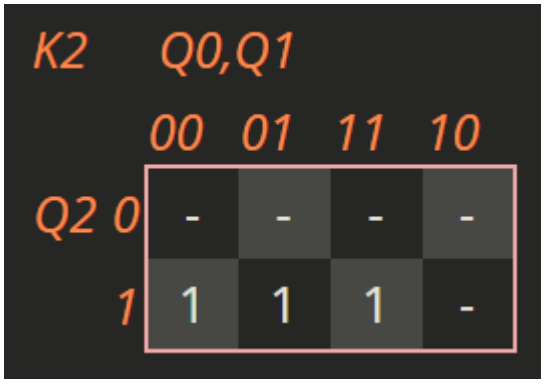
J0=Q_2' K0=1





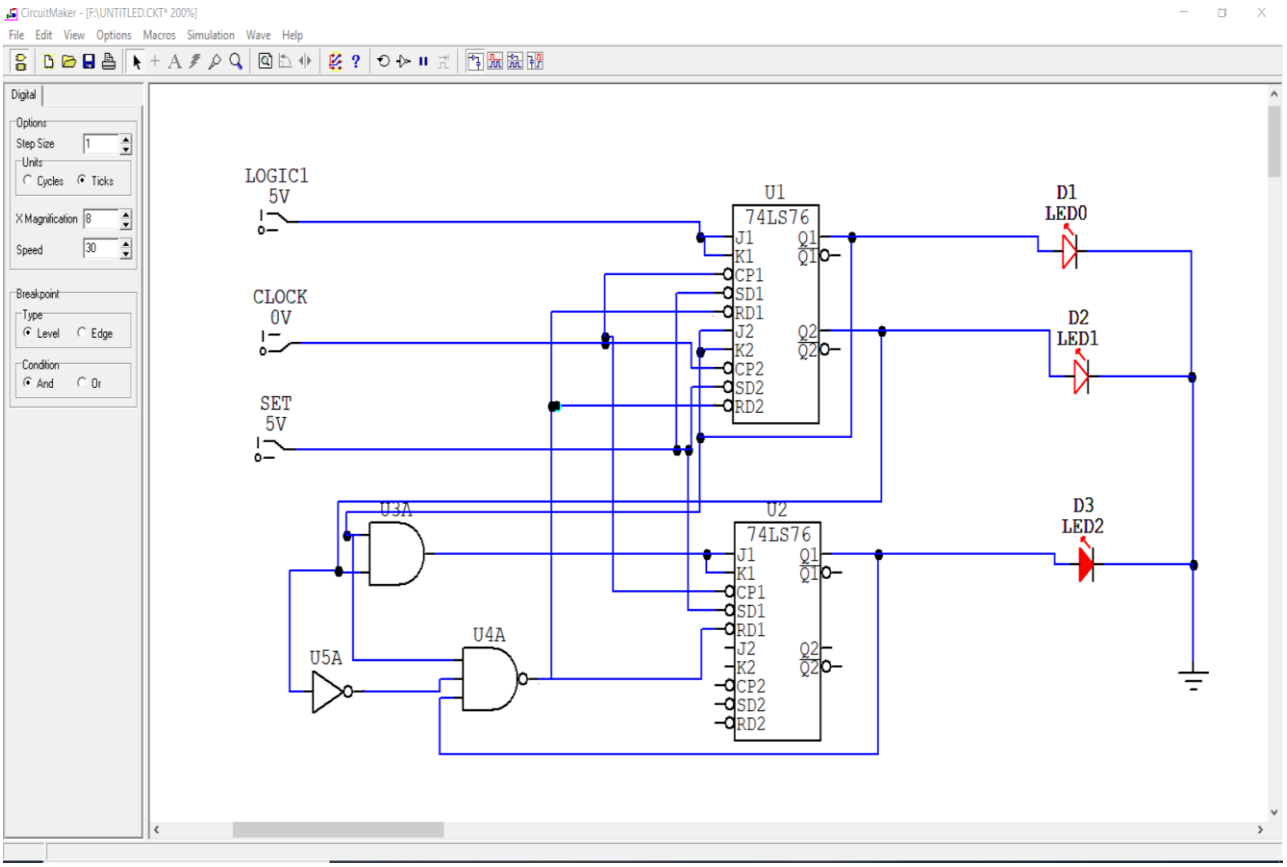
J1=Q_0Q_2' K1=(Q_0'Q_2')'





J2=Q_1Q_0 K2=1

Simulation :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U4A
U5A
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LED0
D2
LED1
D3
LED2

Conclusion:

- Counters are sequential logic devices that are activated or triggered by an external timing pulse or clock signal. A counter can be constructed to operate as a synchronous circuit or as an asynchronous circuit. With synchronous counters, all the data bits change synchronously with the application of a clock signal. Whereas an asynchronous counter circuit is independent of the input clock so the data bits change state at different times one after the other.
- **Modulus Counters**, or simply *MOD counters*, are defined based on the number of states that the counter will sequence through before returning back to its original value. For example, a 2-bit counter that counts from 002 to 112 in binary, that is 0 to 3 in decimal, has a modulus value of 4 (00 → 1 → 10 → 11, and return back to 00) so would therefore be called a modulo-4, or mod-4, counter. Note also that it has taken four clock pulses to get from 00 to 11.
- A common modulus for counters with truncated sequences is ten (1010), called MOD-10. A counter with ten states in its sequence is known as a decade counter. Decade counters are useful for interfacing to digital displays. Other MOD counters include the MOD-6 or MOD-12 counter which have applications in digital clocks to display the time of day.