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Course	**:**	**CMOS design**
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Lab Report-9

Aim:

Design of a 6T SRAM Cell.
1. Simulate schematic of 6T SRAM Cell in NgSpice.
2. Simulate layout of 6T SRAM Cell in Microwind.

Theory:

6T SRAM Cell:

SRAM means Static Random Access Memory.6T SRAM Cell consists of two crossly coupled inverters and access transistors to read and write the data.Output of both inverters is stable and it will retain the information as long as power supply is ON.SRAM is much faster when compared with the DRAM.there is no need for periodic refreshing of the circuit.

Read and Write operations:

→For Read and Write Operations Wordline should be 1.
→if Wordline = 0 it is Hold State for 6T SRAM Cell.
→For the Read operation the bit and $\overline{bit}$ will serve as outputs.
→For the Write operation the bit and $\overline{bit}$ will serve as inputs.

CMOS Circuit of 6T SRAM Cell:

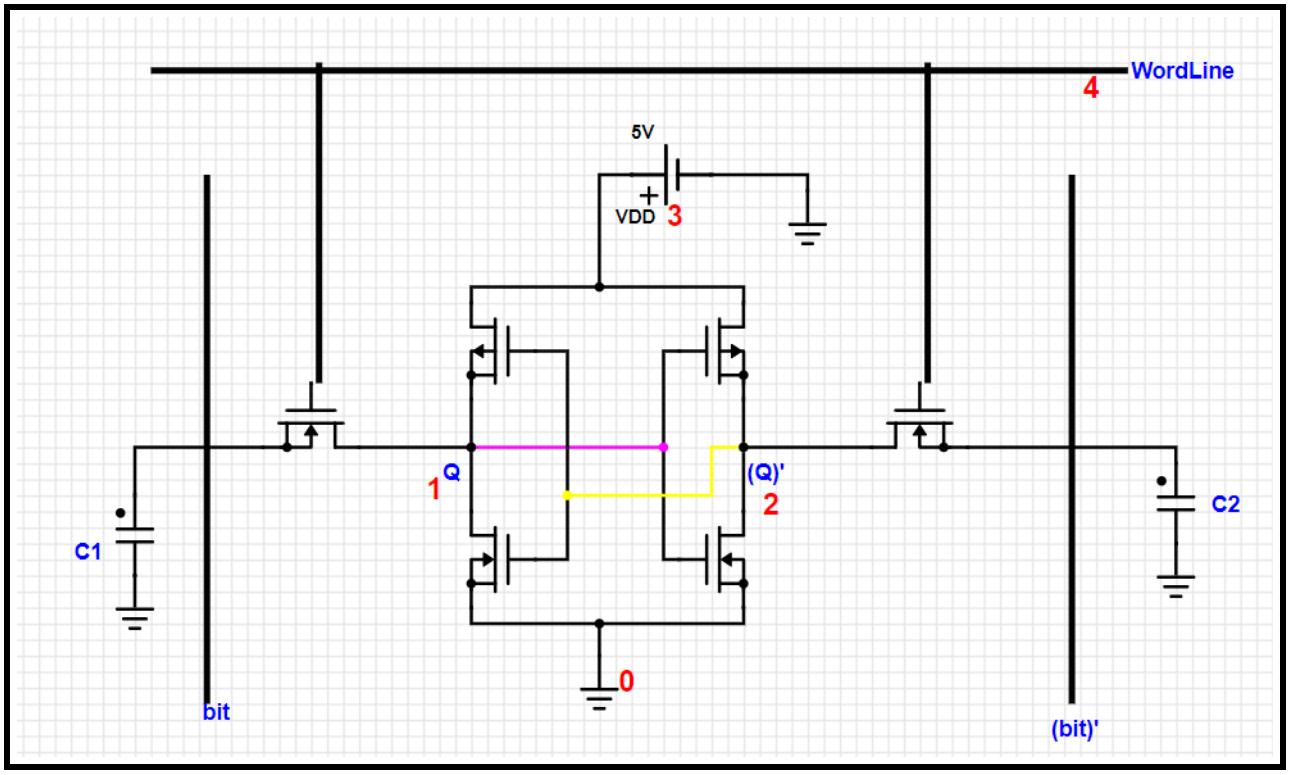


Figure 1: 6T SRAM Cell

In the figure, lets consider M1 is PMOS of inverter with Q, M2 is NMOS of inverter with Q, M3 is PMOS of inverter with $\overline{Q}$, M4 is NMOS of inverter with $\overline{Q}$, M5 is NMOS of left side with gate connected to wordline, M6 is NMOS of right side with gate connected to wordline.

Read Opeartion:

- Let's assume we have Q = 1 and $\overline{Q} = 0$ in the SRAM Cell and we have to read it.
- Wordline = 1 for reading.
- As we wanted to read the data the bit and $\overline{bit}$ lines will behave as Output lines.
- The Capacitors are precharged to VDD/2.
- As Q = 1, M4 is ON, Capacitor of $\overline{bit}$ side will get discharged through M6 and M4.
- Hence $\overline{bit}$ node voltage decreases.
- This values of bit and $\overline{bit}$ are sent to sense amplifier which contains a comparator.It compares the values,if $\overline{bit}$ voltage is less it will sense so that we have successfully read Q = 1.

Write Opeartion:

- Let's assume we have Q = 0 and $\overline{Q} = 1$ in the SRAM Cell and we have to write

1 into it.

- Wordline = 1 for writing.
- As we wanted to writing the data the bit and $\overline{bit}$ lines will behave as input lines.
- As we need to write Q = 1, so the $\overline{Q} = 0$, for this the $\overline{bit}$ will be grounded(simply where you have to write 0 make that line grounded).
- when $\overline{bit}$ line is grounded ,the voltage at $\overline{bit}$ decreases,the Transistors M1 and M2 will be affected.
- if the voltage goes below Vth of M2, M2 will turn off and Q will be equal to VDD i.e we have successfully written Q = 1.

Codes, Layouts and Outputs:

Note:In all the Circuit figure node number is displayed in red color.

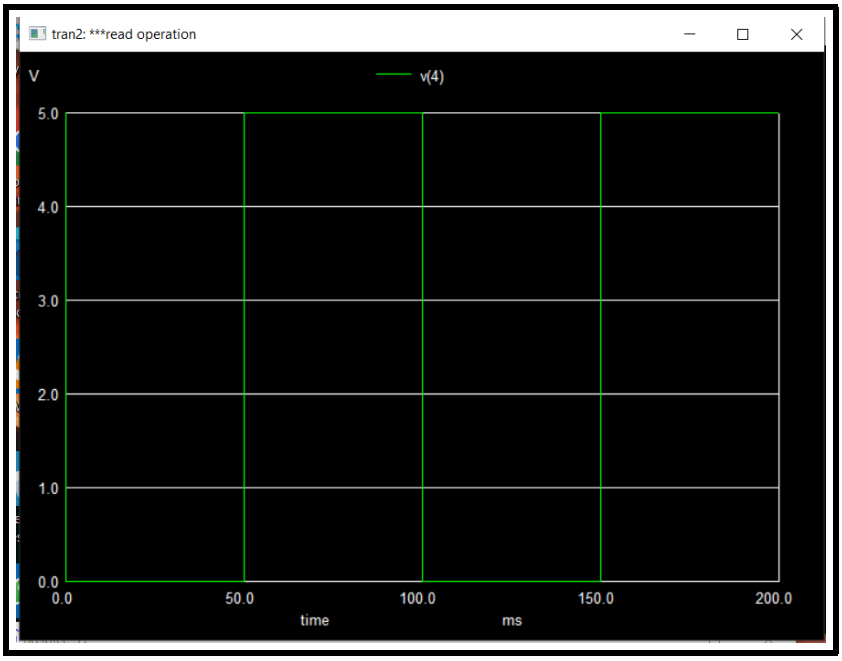
6T SRAM Cell:

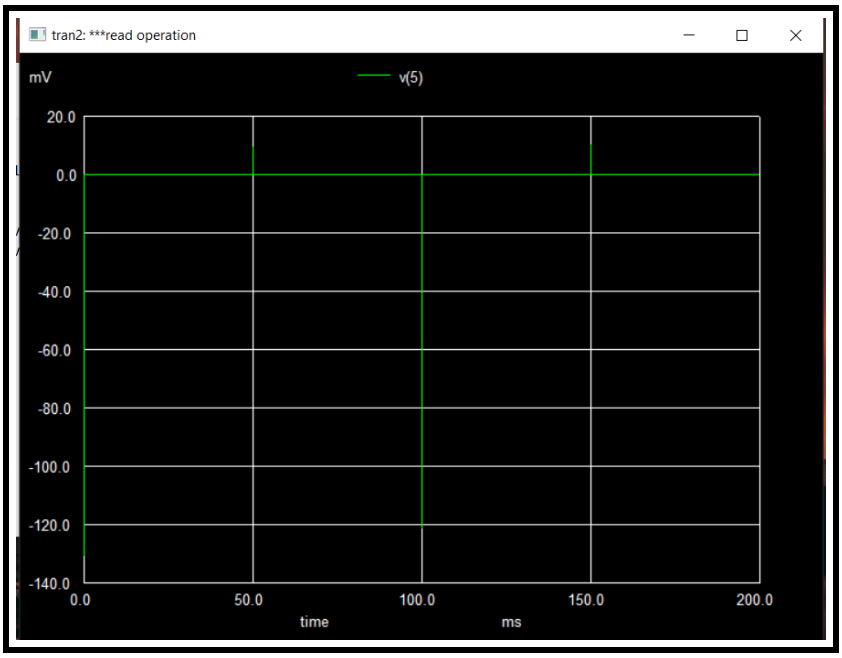
NgSpice Code for Read Operation:

```
***Read Operation
VDD 3 0 dc 5V
VQ 1 0 dc 0V
VQb 2 0 dc 5V
Vw 4 0 pulse(5 0 0 0 0 50ms 100ms)
C1 5 0 0.1p
C2 6 0 0.1p
.model nmod nmos level = 54 version = 4.7
.model pmod pmos level = 54 version = 4.7
M1 1 2 3 3 pmod w = 100u l = 10u
M2 1 2 0 0 nmod w = 100u l = 10u
M3 2 1 3 3 pmod w = 100u l = 10u
M4 2 1 0 0 nmod w = 100u l = 10u
M5 1 4 5 0 nmod w = 100u l = 10u
M6 2 4 6 0 nmod w = 100u l = 10u
.tran 0.01ms 200ms
.control
run
plot V(4)
plot V(5)
plot V(6)
.endc
```

```
.end
```

Ngspice Output for Read Operation:





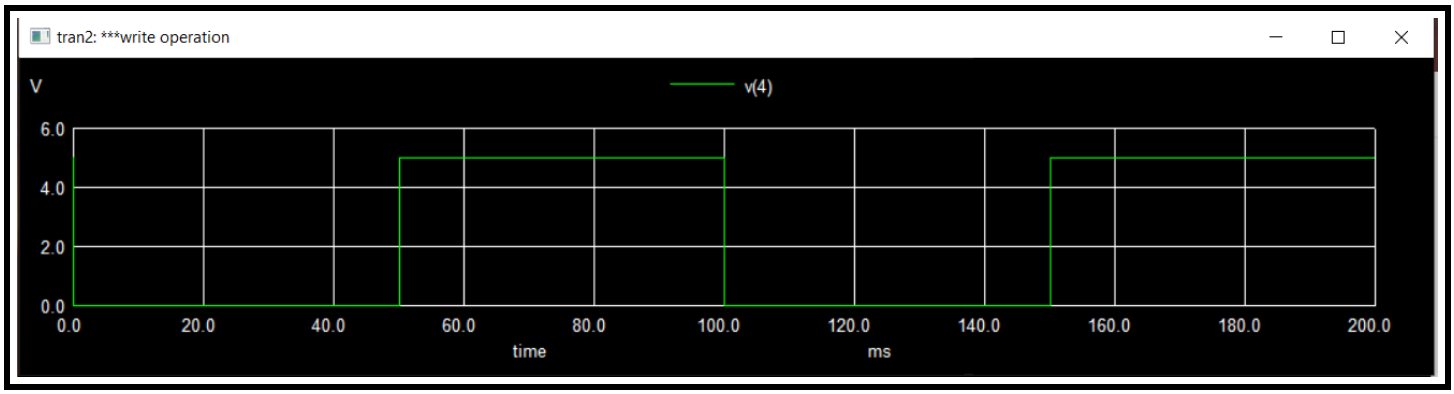
In above Output Images V(4) is wordline and V(5) is the bit line,as we can see in code we gave Q = 1 and we read it successfully as we see it in bit line.

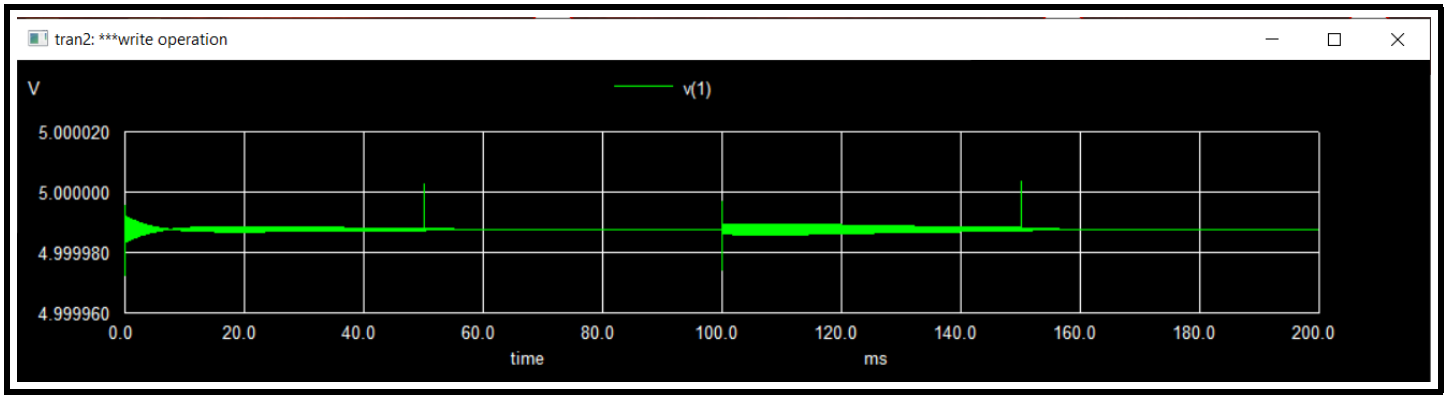
NgSpice Code for Write Operation:

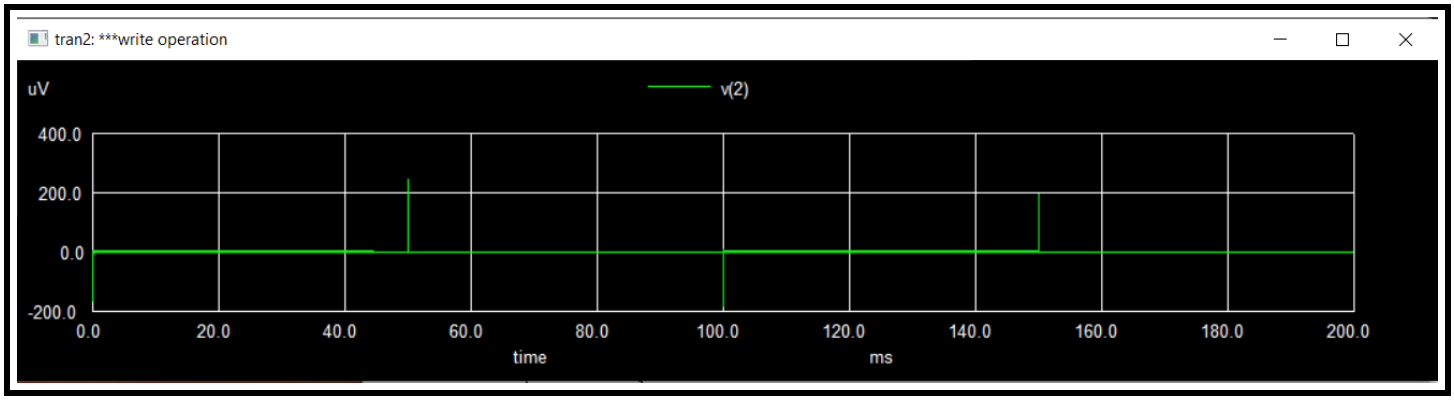
```
***Write Operation
VDD 3 0 dc 5V
Vbit 5 0 dc 5V
Vbitb 6 0 dc 0V
Vw 4 0 pulse(5 0 0 0 0 50ms 100ms)
```

```
C1 5 0 0.1p
C2 6 0 0.1
.model nmod nmos level = 54 version = 4.7
.model pmod pmos level = 54 version = 4.7
M1 1 2 3 3 pmod w = 100u l = 10u
M2 1 2 0 0 nmod w = 100u l = 10u
M3 2 1 3 3 pmod w = 100u l = 10u
M4 2 1 0 0 nmod w = 100u l = 10u
M5 1 4 5 0 nmod w = 100u l = 10u
M6 2 4 6 0 nmod w = 100u l = 10u
.tran 0.01ms 200ms
.control
run
plot V(4)
plot V(1)
plot V(2)
.endc
.end
```

Ngspice Output for Write Operation:







In above Output Images V(4) is wordline, V(1) is the Q and V(2) is the Qbar.We have Successfully written Q = 1 by making $\overline{bit}$ as ground(0).so we performed Write Operation.

Read Opeartion:

Microwind Layout:

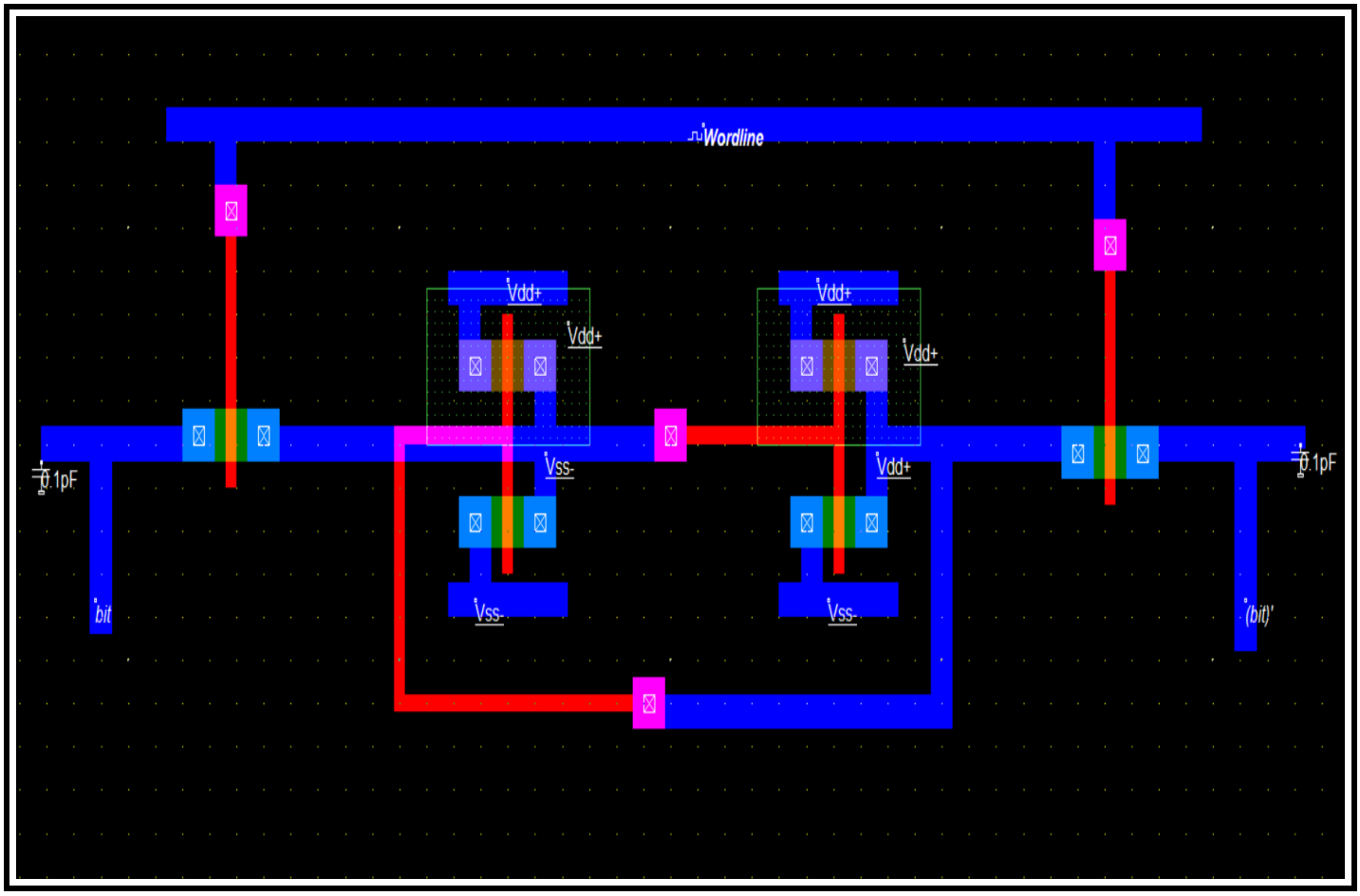


Figure 2: Microwind Layout of 6T SRAM Cell

Simulation Output of Microwind Layout:

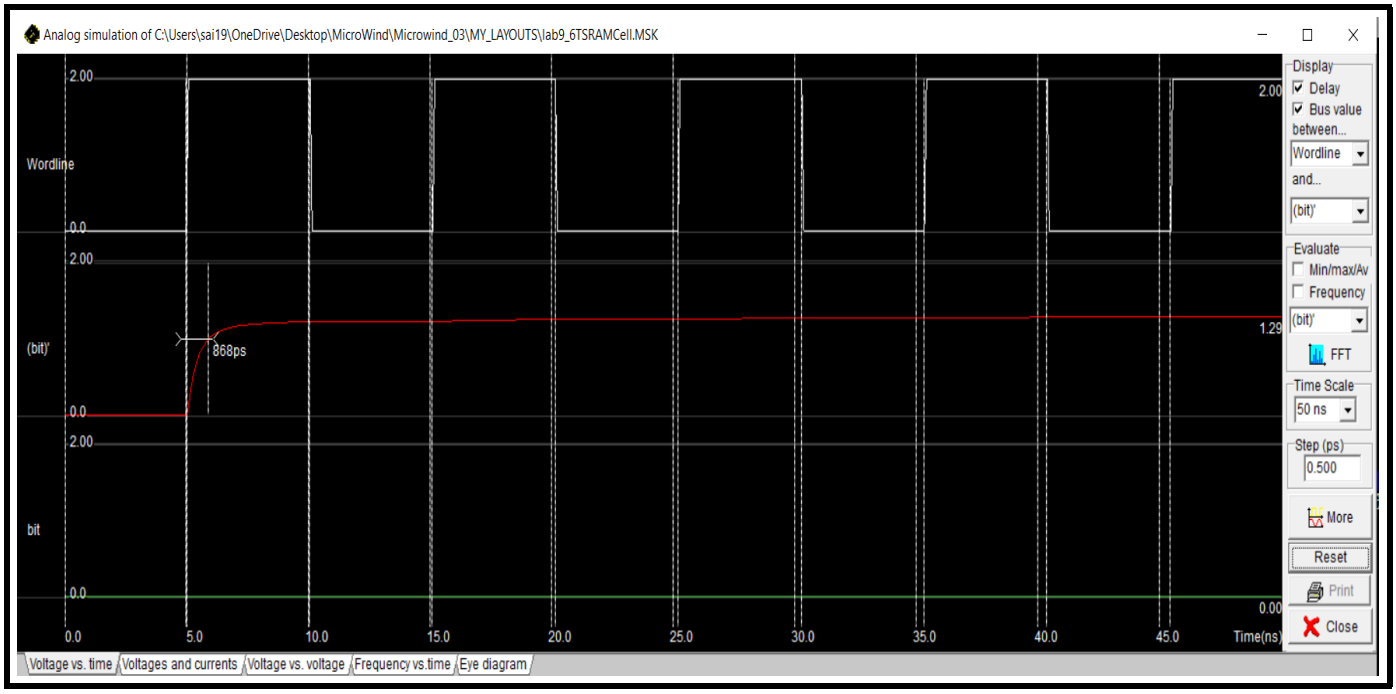


Figure 3: Microwind Layout Output of 6T SRAM Cell

Wrire Opeartion:

Microwind Layout:

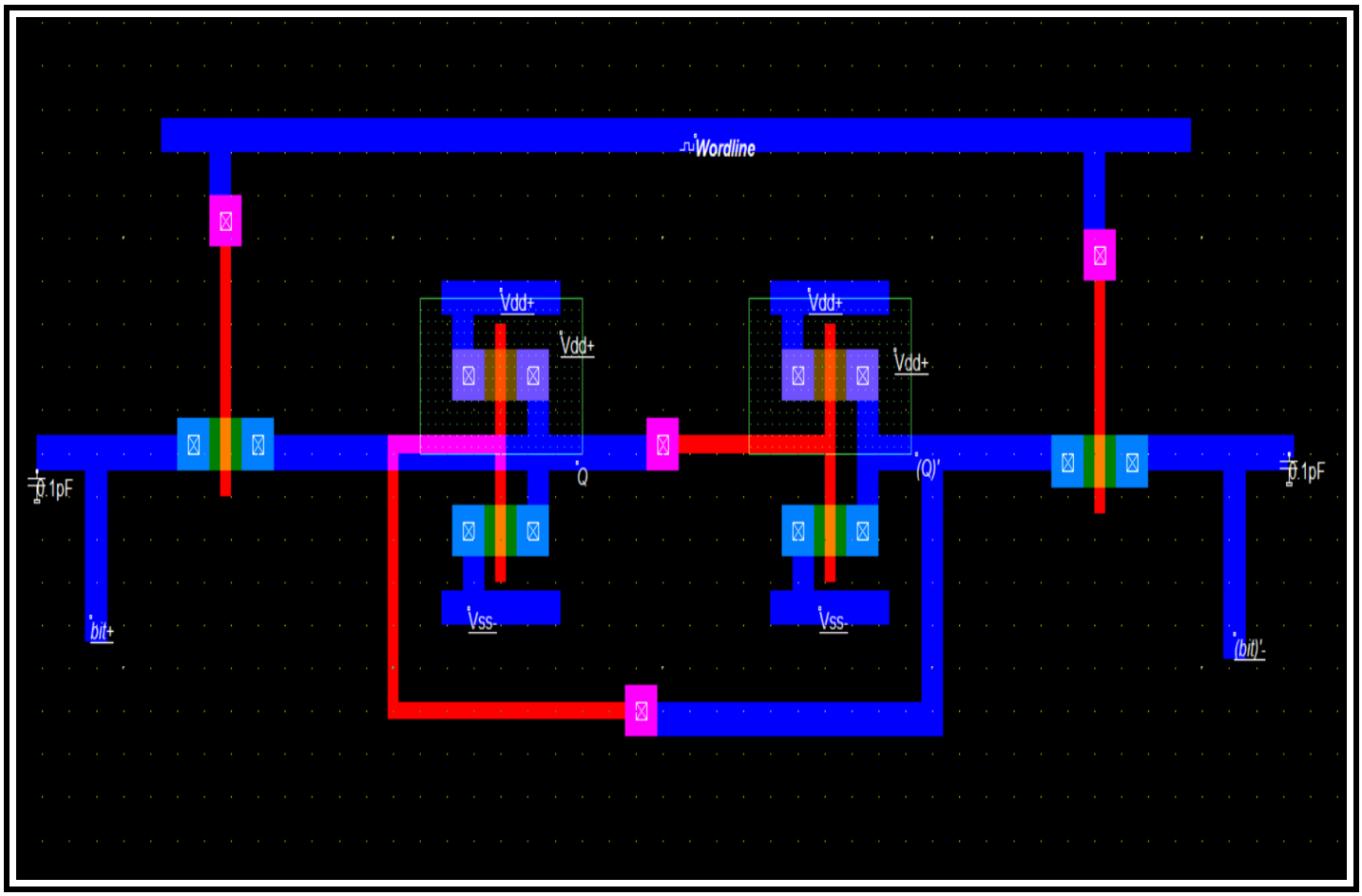


Figure 4: Microwind Layout of 6T SRAM Cell

Simulation Output of Microwind Layout:

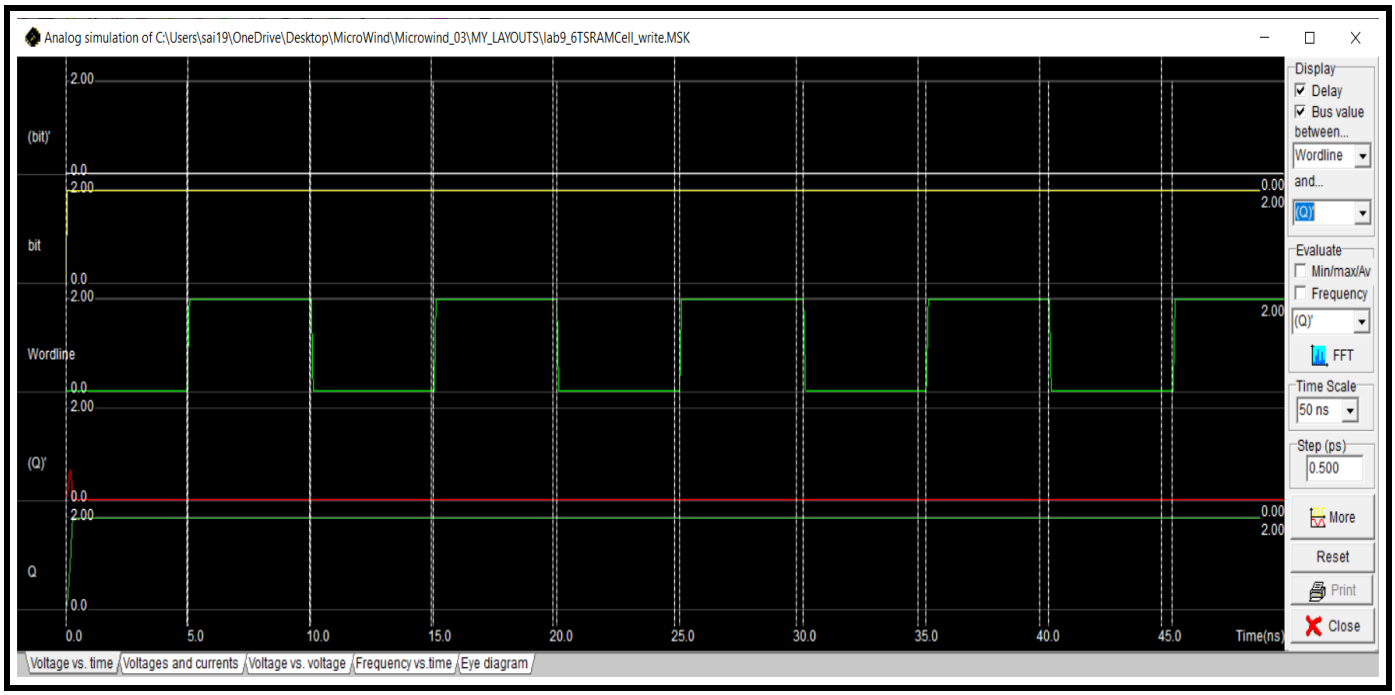


Figure 5: Microwind Layout Output of 6T SRAM Cell

Conclusion:

In this lab section, we designed 6T SRAM Cell,we designed circuit of 6T SRAM Cell using NgSpice and designed its Layout in Microwind,and verified both outputs of NgSpice and Microwind Layout.we performed both Read and Write Operations.