INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
NAGPUR

Name : M.Saikumar
Roll.No : BT19ECE073
Course : CMOS design
Instructor : Dr.Paritosh Peshwa

Lab Report-8

Aim:

Design of a CMOS full adder.
1. Simulate schematic of full adder in NgSpice.
2. Simulate layout of full adder in Microwind.

Theory:

Full Adder:

A full adder circuit is central to most digital circuits that perform addition or subtraction. It is so called because it adds together two binary digits, plus a carry-in digit to produce a sum and carry-out digit.1 It therefore has three inputs and two outputs.A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

Equations of Sum and Carry of Full Adder:

$$Sum(S) = A \oplus B \oplus C_{in}$$

$$CarryOut(C_{out} = AB + BC_{in} + AC_{in}$$

Implementation of Full Adder by CMOS Logic:

If we implement the Sum and CarryOut individually by CMOS Logic it will be complex and bulky,so we have to reduce the circuit,one way is to get Sum equation which have CarryOut in it,

lets start with Sum equation,

$$S = A \oplus B \oplus C_{in}$$

$$S = ABC + A\overline{B}\,\overline{C_{in}} + \overline{A}B\overline{C_{in}} + \overline{A}\,\overline{B}C_{in}$$

$$S = ABC + A[\overline{A}\,\overline{B} + \overline{B}\,\overline{C_{in}} + \overline{A}\,\overline{C_{in}}] + B[\overline{A}\,\overline{B} + \overline{B}\,\overline{C_{in}} + \overline{A}\,\overline{C_{in}}] + C_{in}[\overline{A}\,\overline{B} + \overline{B}\,\overline{C_{in}} + \overline{A}\,\overline{C_{in}}]$$

$$S = ABC + (A + B + C_{in})[\overline{A}\,\overline{B} + \overline{B}\,\overline{C_{in}} + \overline{A}\,\overline{C_{in}}]$$

here $[\overline{A}\,\overline{B} + \overline{B}\,\overline{C_{in}} + \overline{A}\,\overline{C_{in}}] = \overline{C_{out}}$

Therefore,

$$S = ABC + (A + B + C_{in})C_{out}$$

Digital Circuit of Full Adder:

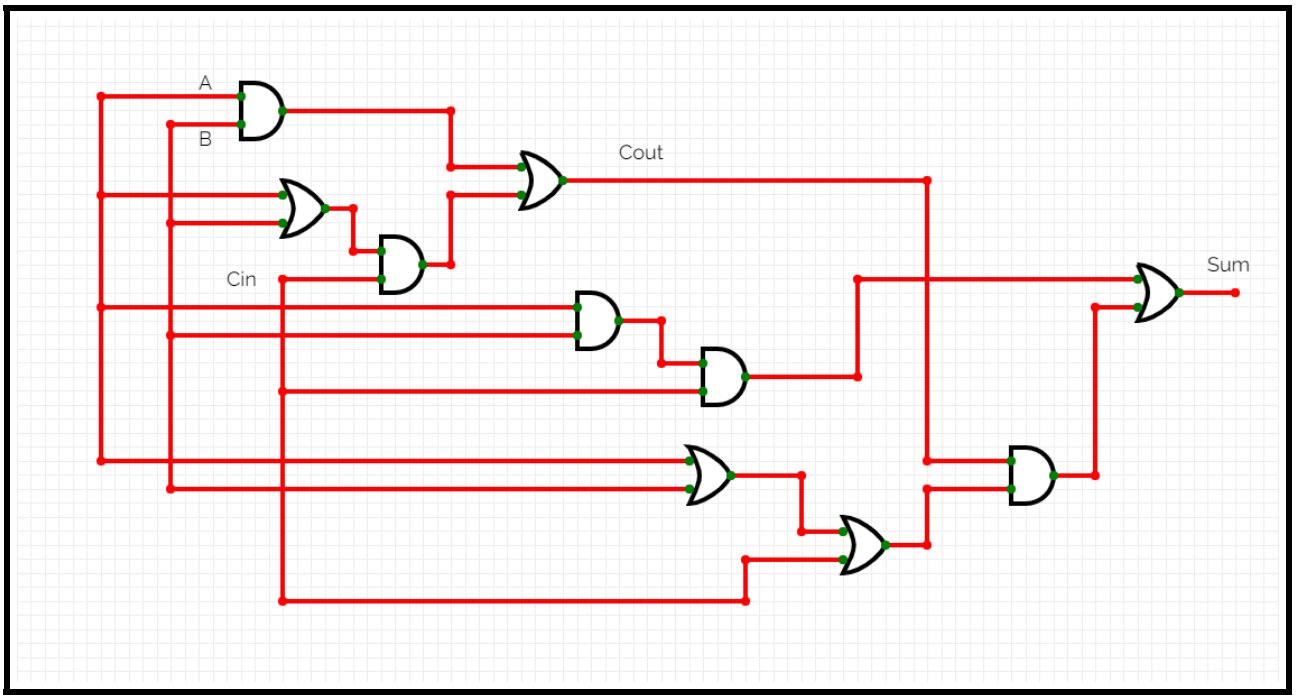


Figure 1: Full Adder's Digital Circuit

Truth Table of Full Adder:

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 2: Truth Table of Full Adder

Circuits, Layouts and Outputs:

Note:In all the Circuit figure node number is displayed in red color.

Full Adder:

Circuit:

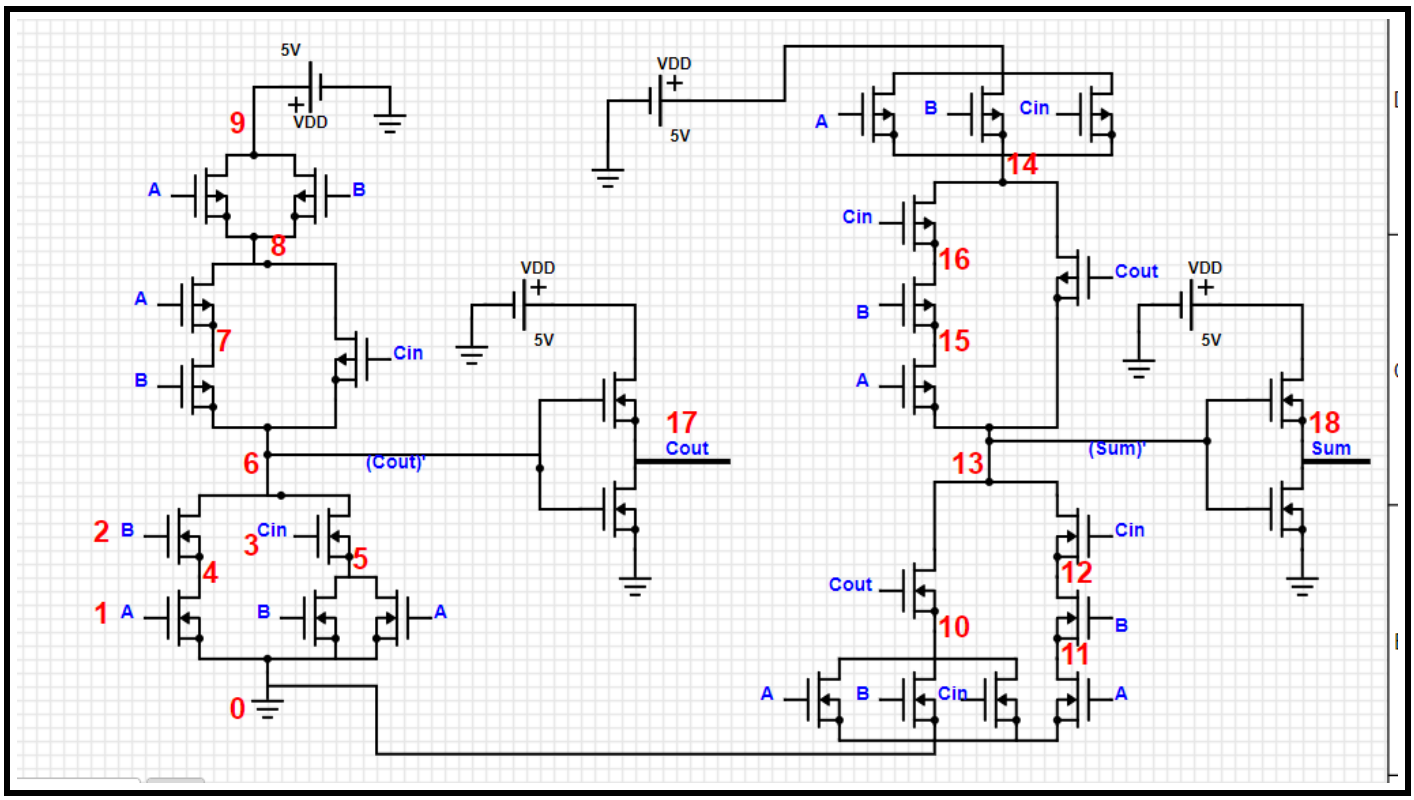


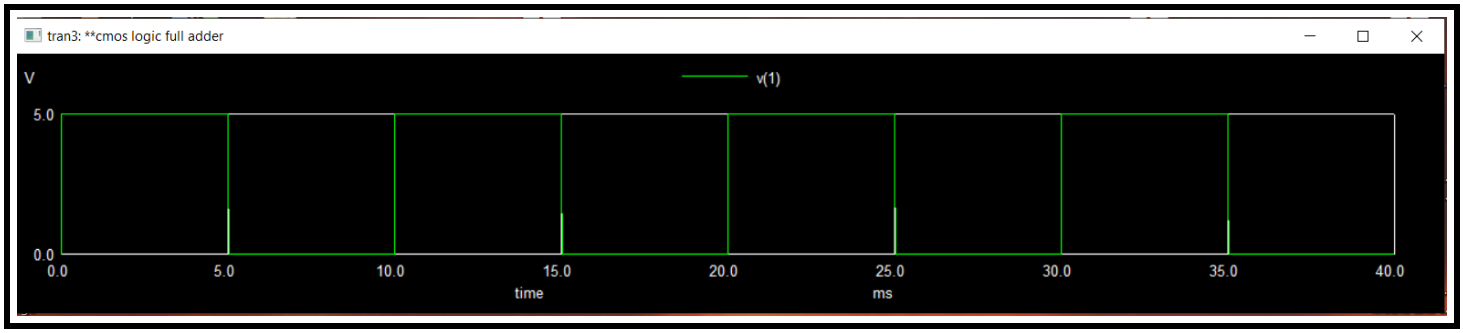
Figure 3: CMOS Circuit of Full Adder

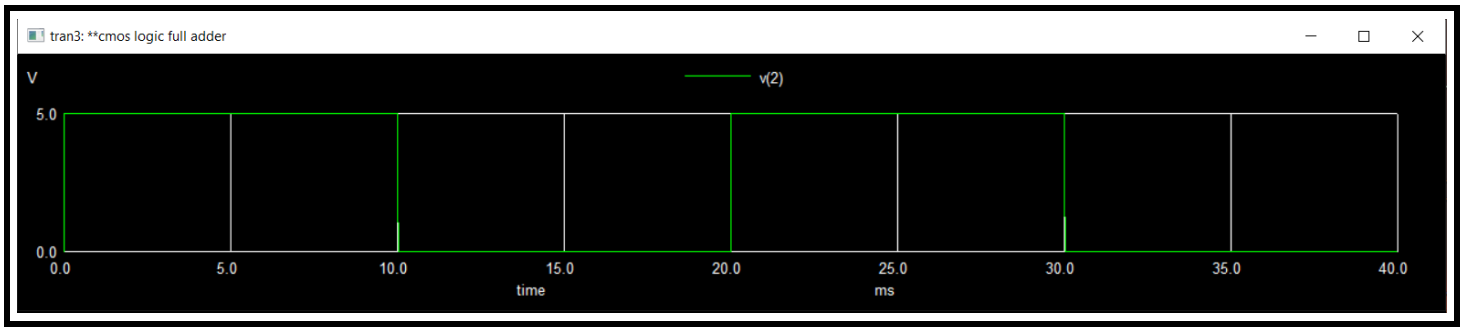
NgSpice Code:

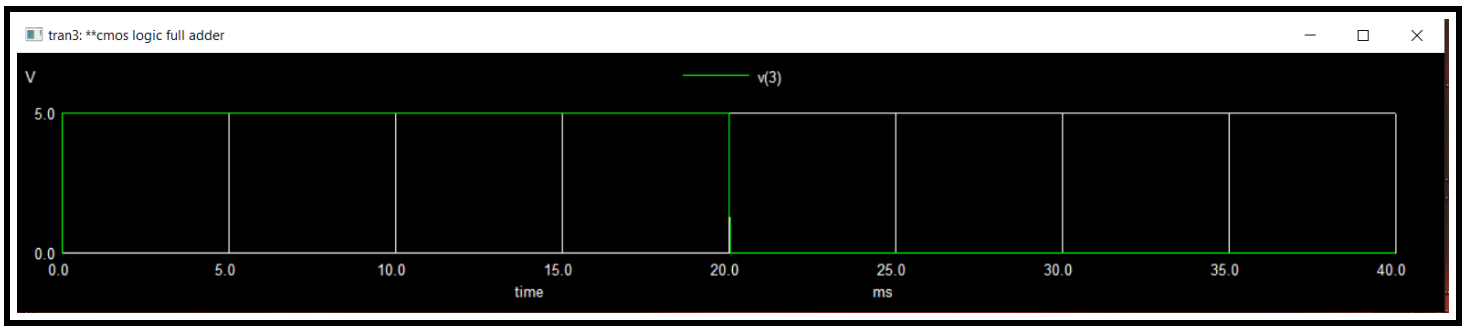
```
**CMOS Logic Full Adder
VDD 9 0 dc 5V
VA 1 0 pulse(0 5 0ns 0ns 0ns 5ms 10ms)
VB 2 0 pulse(0 5 0ns 0ns 0ns 10ms 20ms)
VCin 3 0 pulse(0 5 0ns 0ns 0ns 20ms 40ms)

.model nmod nmos level = 54 verison = 4.7
.model pmod pmos level = 54 verison = 4.7

MCoutbarNA1 4 1 0 0 nmod w = 100u l = 10u
MCoutbarNB1 6 2 4 0 nmod w = 100u l = 10u
MCoutbarNCin 6 3 5 0 nmod w = 100u l = 10u
MCoutbarNA2 5 1 0 0 nmod w = 100u l = 10u
MCoutbarNB2 5 2 0 0 nmod w = 100u l = 10u
MCoutbarPA1 7 1 8 9 pmod w = 50u l = 10u
```

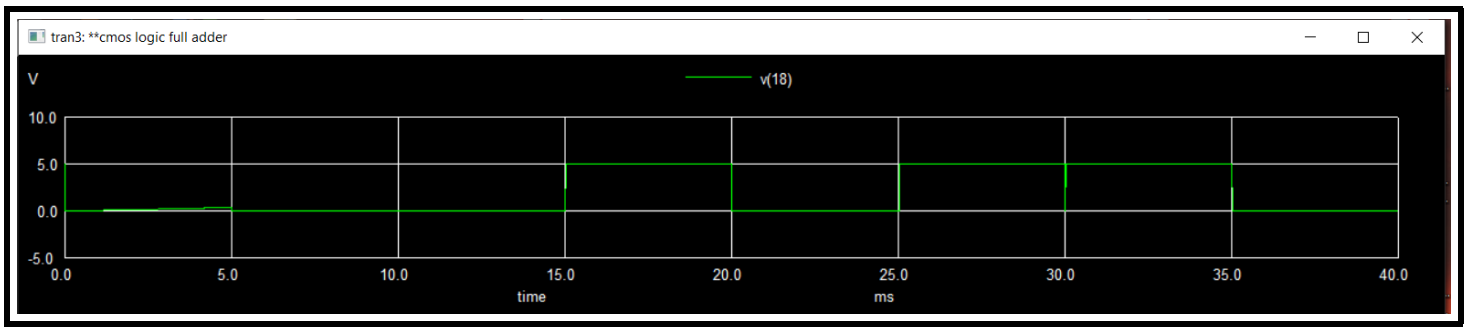
```
MCoutbarPB1 6 2 7 9 pmod w = 50u l = 10u
MCoutbarPCin 6 3 8 9 pmod w = 50u l = 10u
MCoutbarPA2 8 1 9 9 pmod w = 50u l = 10u
MCoutbarPB2 8 2 9 9 pmod w = 50u l = 10u

MCoutInverterN 17 6 0 0 nmod w = 100u l = 10u
MCoutInverterP 17 6 9 9 pmod w = 50u l = 10u

MSumbarNA1 10 1 0 0 nmod w = 100u l = 10u
MSumbarNB1 10 2 0 0 nmod w = 100u l = 10u
MSumbarNCin1 10 3 0 0 nmod w = 100u l = 10u
MSumbarNA2 11 1 0 0 nmod w = 100u l = 10u
MSumbarNB2 12 2 11 0nmod w = 100u l = 10u
MSumbarNCin2 13 3 12 0 nmod w = 100u l = 10u
MSumbarNCout 13 6 10 0 nmod w = 100u l = 10u
MSumbarPA1 13 1 15 9 pmod w = 50u l = 10u
MSumbarPB1 15 2 16 9 pmod w = 50u l = 10u
MSumbarPCin1 16 3 14 9 pmod w = 50u l = 10u
MSumbarPA2 14 1 9 9 pmod w = 50u l = 10u
MSumbarPB2 14 2 9 9 pmod w = 50u l = 10u
MSumbarPCin2 14 3 9 9 pmod w = 50u l = 10u
MSumbarPCout 13 6 14 9 pmod w = 50u l = 10u

MSumInverterN 18 13 0 0 nmod w = 100u l = 10u
MSumInverterP 18 13 9 9 pmod w = 50u l = 10u

.tran 0.01ms 40ms
.control
run
plot V(1)
plot V(2)
plot V(3)
plot V(17)
plot V(18)
.endc
.end
```

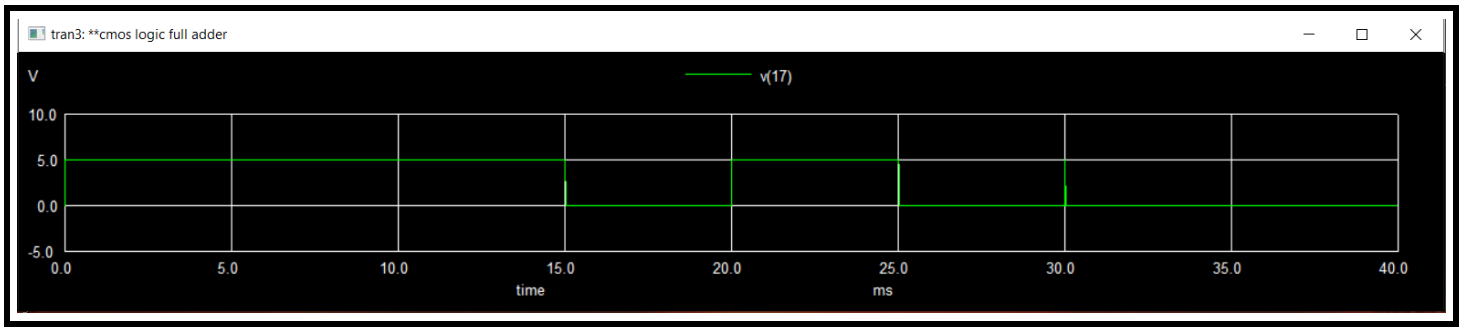
Ngspice Output:











In above Output Images V(1), V(2), V(3), V(18) and V(17) are A, B, C_{in} , Sum(S) and CarryOut(C_{out}) respectively

Microwind Layout:

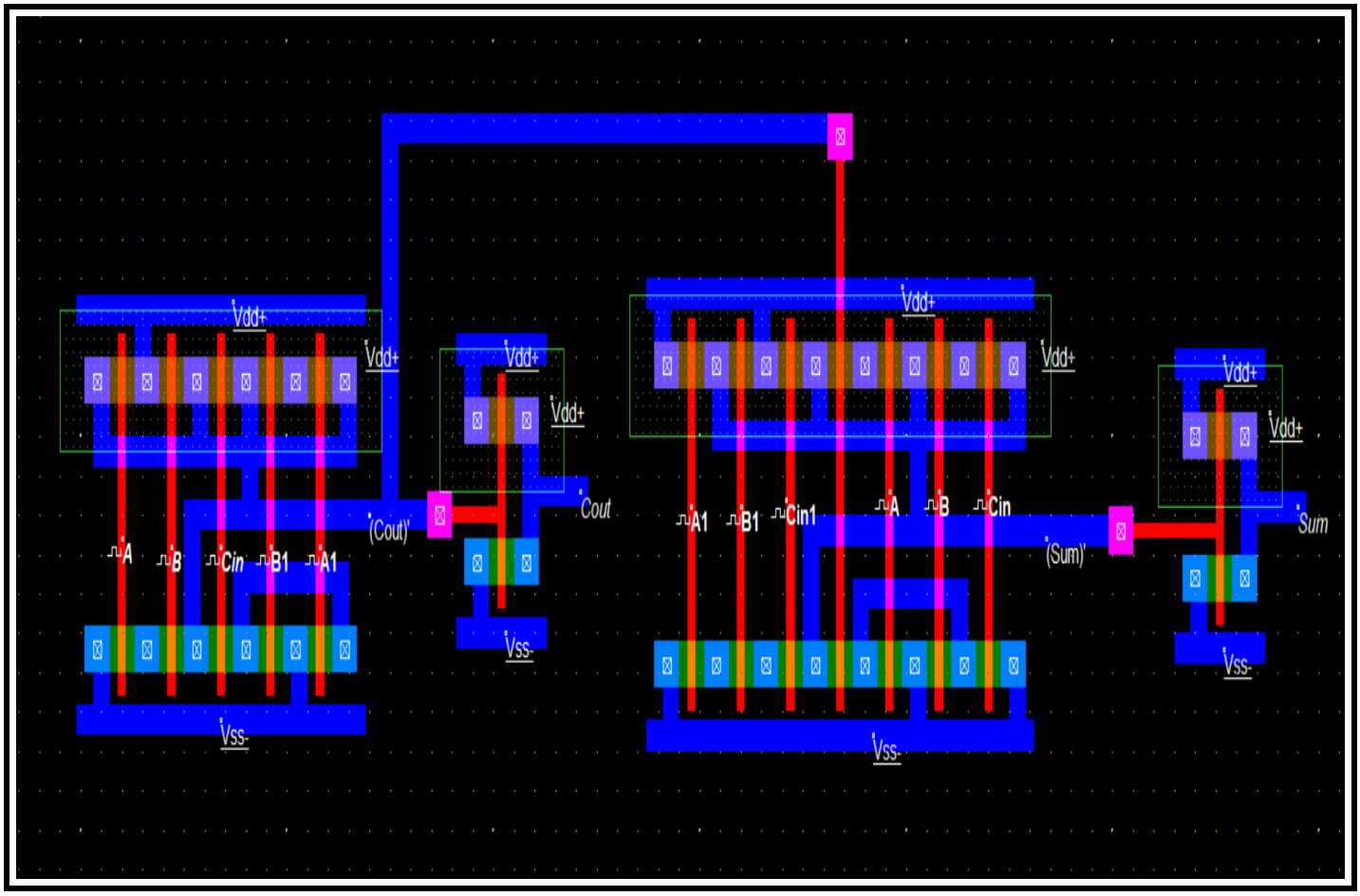


Figure 4: Microwind Layout of Full Adder

Simulation Output of Microwind Layout:

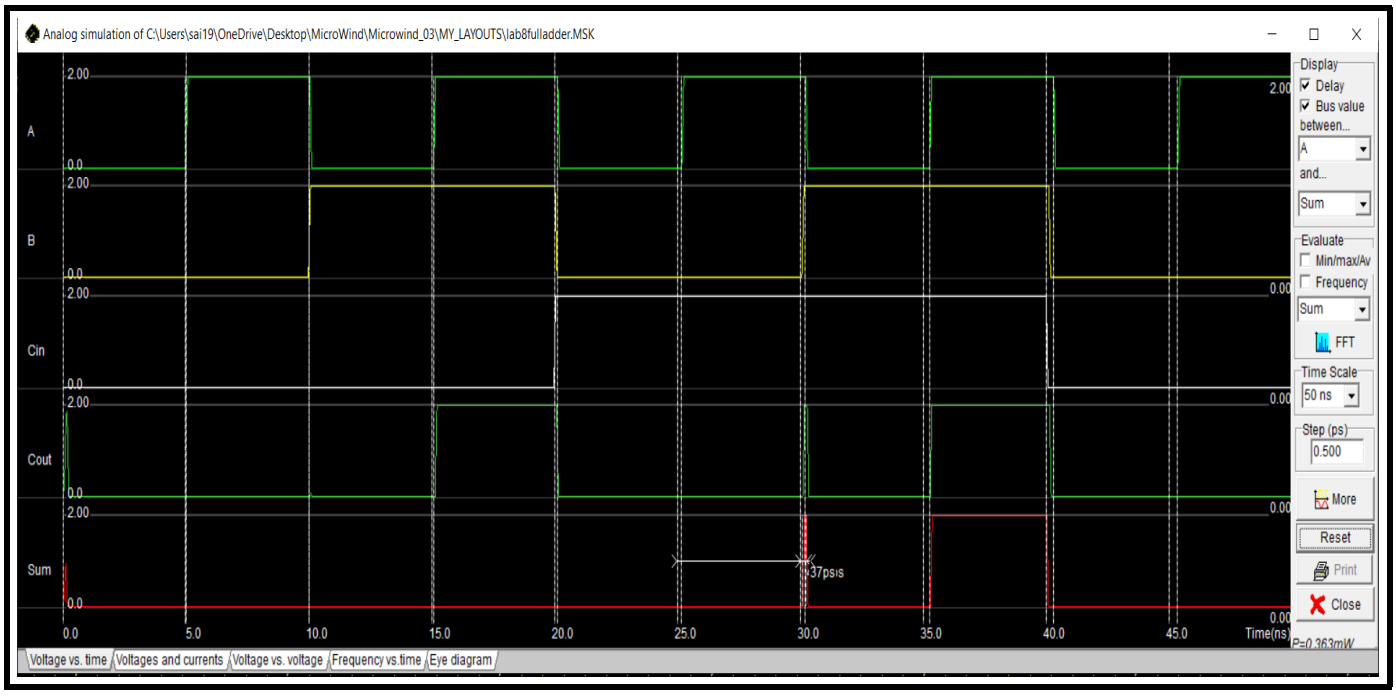


Figure 5: Microwind Layout Output of Full Adder

Conclusion:

In this lab section, we designed CMOS logic of full Adder ,we designed circuit of CMOS full adder using NgSpice and designed its Layout in Microwind,and verified both outputs of NgSpice and Microwind Layout with the Truth Table of FullAdder.