

Chapter - 2) 16 Bit Microprocessor : 8086

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Introduction: 8086 is the first 16-bit microprocessor developed in 1978 by Intel Corporation. 8086 is a 16-bit, H-MOS microprocessor. It is available in 40 pin IC and operate in 5 volts DC supply. Its electronic circuitry consists of 29000 transistors, it is implemented in N-channel silicon gate technology and available in three versions i.e. 8086 (5 MHz), 8086-2 (8 MHz), 8086-1 (10 MHz).

8086 has 20-address lines using which we can interface $2^{20} = 1\text{ MB}$ of memory means it can address upto 1 MB memory. Out of 20 address lines 16-address lines are multiplexed with data lines and named as AD0-AD15. Remaining 4 address lines are also multiplexed with status signals.

Salient features of 8086 microprocessor:

- 1) Provides 20 address lines so 1MB of memory can be addressed.
- 2) Multiplexed 16-bit address and databus, AD0-AD15 to minimize number of pins on IC.
- 3) Operating clock frequencies are 5MHz, 8MHz, 10MHz.
- 4) Arithmetic operation can be performed on 8-bit or 16-bit signed or unsigned data including multiplication and division.
- 5) Can operate in single processor and multiprocessor configuration i.e. operating modes.
- 6) Instruction set is powerful, flexible and can be programmed in high level language like C-Language.
- 7) Provides 256 types of vectored software interrupts.
- 8) Provides 6 byte instruction queue for pipelining of instruction execution.
- 9) Generates 8-bit of 16-bit I/O address so it can access maximum 64K I/O devices.
- 10) Operate in maximum and minimum mode to achieve higher performance level.

- 1) Supports 24 operands addressing modes
 2) Supports multiprogramming.
 3) Provides separate instruction for string manipulation.

Pin description of 8086:

(contd.)

GND	1	40	Vcc
AD0	2	39	AD15 ← Multiplexed Address/Data pin
AD1	3	38	A16/S3
AD2	4	37	A17/S4
AD3	5	36	A18/S5
AD4	6	35	A19/S6
AD5	7	34	BHE /S7
AD6	8	33	MN/MX ← Select minimum/max mode
AD7	9	32	RD
Multiplexed address & data bus			
AD8	10	31	RQ/GTO (HOLD)
AD9	11	30	RQ/GT1 (HLDA)
AD10	12	29	LOCK (WR)
AD11	13	28	S2 Maximum mode (M/I0)
AD12	14	27	S1 Minimum mode (DT/R)
AD13	15	26	S0 (DEN)
AD14	16	25	QSO (ALE)
NMI	17	24	QSI (INTA)
INT18	18	23	Test
CLK	19	22	Ready
GND	20	21	Reset

① ADO-AD15 : These lines are time multiplexed bi-directional address/data bus. During t1 clock cycle of the bus cycle, they carry lower order 16-bit address and during t2, t3, t4, they carry 16-bit data. So ADO-AD7 lines carry lower order byte of data and AD8-AD15 carry higher order byte of data.

② RD(READ) : It is an active low read signal issued by the processor to indicate that the processor is performing the READ operation with memory or I/O depending on the status of M/I0 signal. This signal is used to READ devices which are connected to 8086 local bus and remain tri-stated during Hold Acknowledge.

③ READY : This is an acknowledgement from the slower I/O device or memory. It is an active high input signal when HIGH, it indicates that peripheral device is ready to transfer data.

④ RESET : It is a system reset. When this signal goes high, processor enters into reset state and terminate the current activity and start execution from FFFF0H. This signal is active high signal and must be active for at least 4-clockcycles.

⑤ INTR (Interrupt request) : This is a level triggered interrupt request input last clock cycle of each instruction to determine the availability of the request. If any interrupt request is occurred, the processor enters the interrupt acknowledge cycle.

⑥ NMI : This is an edge triggered input interrupt request which causes a type to interrupt. The NMI is not maskable by software. It is an edge triggered interrupt request which can be generated by external logic or software. It is a non-maskable interrupt.

(7) TEST : This signal is used to test the status of maths processor. 8087. The busy pin of 8087 is connected to the test pin of 8086. The input signal is examined by ~~one~~ instruction. If TEST signal goes low, execution will continue else the processor remains in the idle state.

(8) CLK (Clock Input) : This clock input provides the basic timing for processor operation and bus control activity. It is symmetrical square wave with 33% duty cycle. The range of frequency for different 8086 versions is from 5MHz to 10 MHz.

(9) Vcc & 5 volt power supply for the operation of internal circuit.

(10) GND : Ground for the internal circuit.

(11) BHE / S7 (Bus High Enable / Status) :

BHE	A0	Word/Byte Access
0	0	Whole word from even address
0	1	Upper byte from / to odd address
1	0	Lower byte from / to even address
1	1	None

A0 = 0 → even address

A0 = 1 → odd address

Note : Lower data byte is on even address

Upper data byte is on odd address

The Bus High Signal is used to indicate transfer of data over higher order D8-D15 databus as shown in above figure. It goes low for the data transfer over D8-D15 and

is used to drive chip selects of odd address memory bank or peripherals. BHE in conjunction with A0 determines whether a byte or word will be transferred from / to memory location. The BHE/S7 is a time multiplexed line occurring t2 to t4. The signal S7 is transmitted on this line.

(12) A15/S6, A13/S5, A11/S4, A10/S3 :

in odd memory side	S4	in S3, high : Segment register	t1 : t2 : t3 : t4	SS (segment register)
in odd memory side	0	0 : S5 (extra data segment register)		
in odd memory side	0	1 : S4 (stack segment)		
1	0	CS (code segment) or name		
1	1	DS (data segment)		

These are time multiplexed address and status lines. During t1 clock cycle, these lines carry upper 4 bit address and during t3 operation, these lines are low. During t2, t3 and t4, S3 and S4 carry status signals and these status lines are used to identify memory segments as shown in figure. SS is an interrupt enabled signal and is updated at the beginning of each clock cycle.

(13) MN/MX : This pin indicates the operating mode of 8086. There are two operating modes of 8086 i.e. minimum mode and maximum mode. When this pin is connected to Vcc, the processor operates in minimum mode and this pin is connected to ground, processor operates in maximum mode.

This status signal reflects the type of operation, being carried out by the processor and required by the bus controller Intel 8288 to generate all memory or I/O access control signals. These become active during t_4 of previous cycle and remain active during t_1 and t_2 of current cycle.

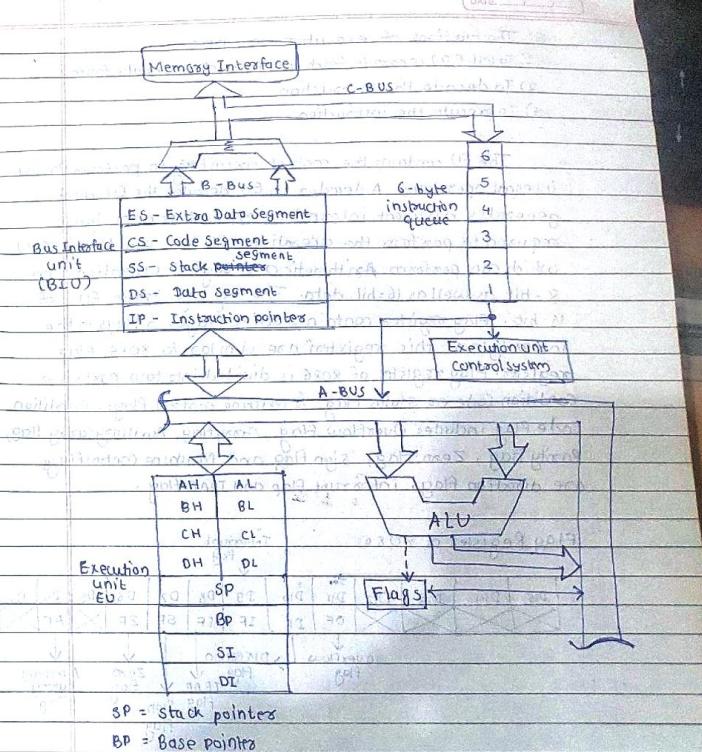
Pin 28: **LOCK**: This is an active low output signal used to prevent other system masters from gaining the system bus. While the lock signal is low, all interrupts are masked and MOIO request is not generated. Lock signal is generated by lock prefix instruction.

Pin 30, 31: **$\overline{RQ}_0/\overline{GT}_0$, $\overline{RQ}_1/\overline{GT}_1$** : These pins are used by other local bus master in maximum mode to gain the control of local buses at the end of processor's current bus cycle.

The pins $\overline{RQ}_0/\overline{GT}_0$ and $\overline{RQ}_1/\overline{GT}_1$ are bi-directional and $\overline{RQ}_0/\overline{GT}_0$ have higher priority than $\overline{RQ}_1/\overline{GT}_1$. After receiving request on these lines the CPU sends acknowledge signal on some lines.

Internal Architecture of 8086: As shown in figure, 8086 CPU is divided into two groups:

- 1) Execution unit (EU)
- 2) Bus Interface Unit (BIU)



SI = Source index

DI = Destination index

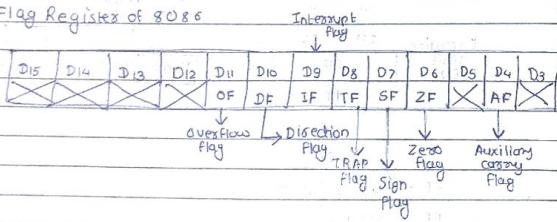
Architecture of 8086

The functions of execution unit are :

- 1) To tell BIU where to fetch the instruction or data from.
- 2) To decode the instruction
- 3) To execute the instruction.

The EU contains the control circuitry to perform various internal operations. A decoder in EU decodes the EU and generates different internal or external control signals required to perform the operation. EU has ~~an~~ 16-bit ALU which can perform Arithmetic and Logical operations on 8-bit as well as 16-bit data. The Flag register in EU is of 16-bit. Flag register contains 9 active flags. 6 flags in the lower byte of this register are similar to 8085 flag register. Flag register of 8086 is divided into two parts i.e. Condition Code or Status Flag & Machine control Flag. Condition Code Flag includes Overflow Flag, Carry Flag, Auxiliary carry Flag, Parity Flag, Zero Flag, Sign Flag and Machine control flags are direction flag, interrupt flag and TRAP flag.

Flag Register of 8086



Status Flag (Condition Code Flag):

- 1) **Carry Flag (CF, D0):** It is set to 1, if there is carry out of the MSB position i.e. resulting from an addition or borrow from subtraction.

- 2) **Zero Flag (ZF, D6):** It is set if the result of arithmetic or logical operation is zero else it will be reset.
 - 3) **Parity Flag (PF, D0):** This flag is used to indicate the parity of result. If the result of operation contains even number of 1's then parity flag is set and for odd number of 1's the parity flag is reset.
 - 4) **Sign Flag (SF, D3):** In a sign magnitude format, the sign of number is indicated by MSB bit. If the result of operation is known as negative, sign flag is set. The sign flag is replicated at bit 12 of MSB bit of result i.e. it is a copy of MSB bit of result.
 - 5) **Overflow Flag (OF, D7):** In case of the sign arithmetic operation, the overflow flag is set if the result is too large to fit in the number of bits available to accommodate it. The overflow flag has no significance in unsigned arithmetic operation.
 - 6) **Auxiliary carry flag (AF, D4):** If an operation performed in ALU generates a carry or borrow from lower nibble i.e. (D0-D3) to upper nibble (D4-D7), the AF flag is set if carry given by D3 bit, else it is reset.
- This is not a general purpose flag. It is used internally by the processor to perform binary to BCD conversion.

⇒ The three control flags:

- 1) **TRAP Flag (TF, D8):** It is used for single-step control. It allows user to execute one instruction of a program at a time for debugging. When TRAP flag is set, the program can be run in single-step mode.

STI → set interrupt flag
CLI → clear interrupt flag
STD → set direction flag
CLD → clear direction flag

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2) Interrupt flag (IF, DI): It is an interrupt enable/disable flag. If it is set, the maskable interrupt INTR of 8086 is enabled. And if it is reset, the interrupt is disabled. It can be set by executing instruction STI and can be cleared by executing CLI instruction.

3) Direction flag (DF, DI): The direction flag (DF) is used in string operation. If DF is set, string bytes are read or write from higher memory addresses to lower memory address. If DF is reset, the string bytes are read or write from lower memory addresses to higher memory address. DF can be set by executing STD instruction and can be reset by executing CLD instruction.

General Purpose register of 8086:

Execution unit (EU) contains eight 16-bit general purpose registers named as AX, BX, CX, DX, SP, BP, SI and DI. Out of these registers AX, BX, CX, DX can be used either as 8-bit registers i.e. (AL, AH), (BL, BH), (CL, CH), (DL, DH) or can be used as four 16-bit i.e. (AX, BX), (CX and DX). The AX register is called as 8-bit accumulator and AX is called as 16-bit accumulator. Some general purpose registers have special tasks such as CX is normally used as counter, BX can be used as a pointer and DX is used for I/O addressing to hold the I/O address. The other registers in EU are SP, BP, SI and DI. SP and BP are pointer registers which holds 16-bit off-set within the particular segment. SI and DI are the index registers.

During the execution of string related operation, the register SI is used to store the off-set of source data or storing in data segment while the register DI is used to store the off-set of destination in data or extra segment.

Bus Interface Unit (BIU):

Function of BIU

- Fetch the instruction or data from memory
- Write the data to memory
- Write the data to the port
- Read the data from the port

Various sections of the BIU are:

- Segment registers
- Instruction queue

① Segment registers: BIU has 4 segment registers of 16-bit each i.e. CS, DS, SS and ES. Following These registers act as memory pointer registers in 8086.

Code Segment register (CS register): It is used to address a memory location in the code segment of the memory where the op-code of program is stored.

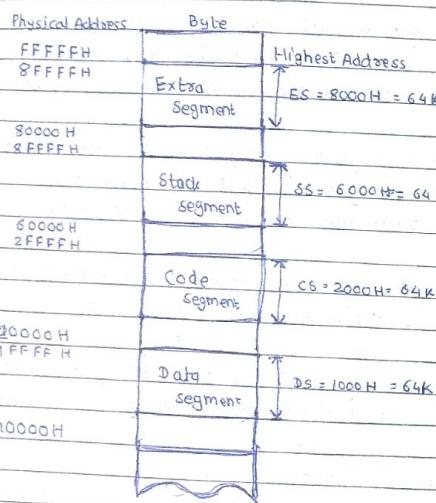
Data segment register (DS register): It points the data segment of the memory where data is stored.

Extra Segment register (ES register): ES register is used to address the additional data segment used to store data.

Stack segment register (SS register): It is used to point stack location in stack segment of the memory and is used to store data temporarily on the stack, such as contents of the CPU registers, flag registers, etc.

~~The default segment base and offset pair register are~~
CS: IP and SS: SP

- ② Instruction queue (IQ): To increase the execution speed, BIU fetches as many as 6-instruction bytes ahead to ~~time~~ time from memory. All the 6-bytes are then held in first in First Out 6-byte register called instruction queue IQ, then all bytes have to be given to EU one by one. This pre-fetching operation of BIU may be in parallel with execution of EU which improves the speed of execution of instruction.



The complete physical memory is divided into a number of logical segments in segmentation. Size of each segment is 64K bytes and addressed by the segment register i.e. CS, DS, ES and SS. The 16-bit content of segment register holds the starting address of a particular segment.

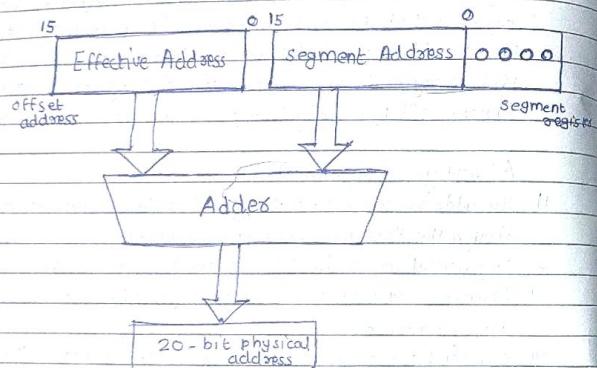
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The off-set address is 16-bit so the maximum off-set value will be FFFFH and hence the maximum size of any segment is $2^{16} = 64\text{ K}$ location. The CPU 8086 is able to address 1MB physical memory. The complete 1MB memory can be divided into 16-segments, each of 64KB size as shown. The address of the segment may be assigned as 0000H to F000H respectively. The offset address values are from 000H to FFFFH. So that the physical address range from 00000H to FFFFFH. The segment register contains the higher order of 16-bits of starting addresses for 4 memory segments i.e. data segment, code segment, data or extra segment, stack segment that the 8086 works with the particular time. The 16-bits offset or displacement is added is added to the 16-bits segment base register after shifting the content of it toward left by one digit to get 20-bit physical address.

Advantages of segmentation:

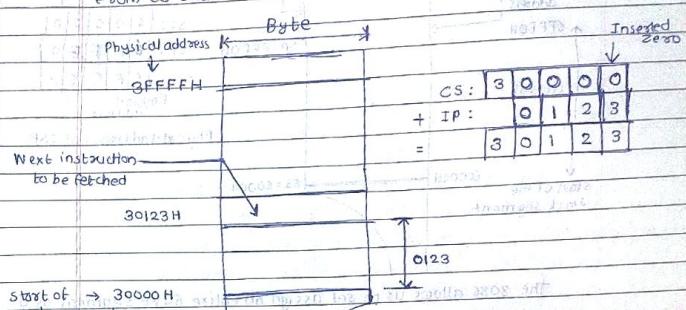
- 1) The address associated with any instruction or data is only 16-bits though the 8086 has 20-bit physical address.
- 2) Segmentation can be used in multilevel time shared system.
- 3) Programs and data can be stored separately from each other in segmentation.
- 4) We can have program of more than 64KB or data more than 64KB, by using more than one code or data segment. Segmentation makes it possible to write program which are position independent or dynamically relocatable.
- 5) Segmentation allows two processes to share data.
- 6) Segmentation allows you to extend the addressability of the processor.

Physical Memory Address Generation: The segment registers are used to hold 16-bit of starting address of 4 memory segments. But 8086 has 20-bit address bus so it can address any of $2^{20} = 1\text{MB}$ of memory. The address associated with any instruction or data byte is only 16-bit called as effective address or off-set or displacement or logical address. The logical addresses are used to calculate physical address. However the address outputted by BIU is 20-bit called as physical address.



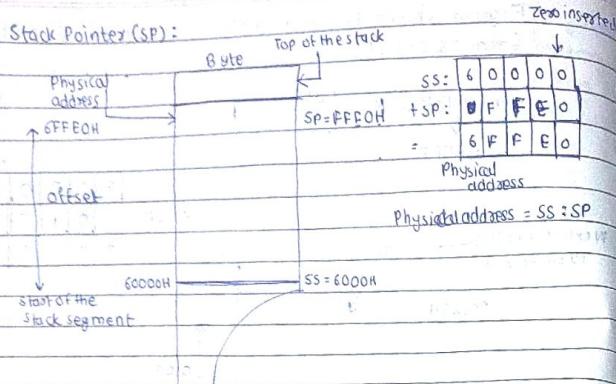
Instruction pointer (IP): The instruction pointer register holds the 16-bit address of the next code byte within the code segment. The values stored in IP is called as off-set or displacement. This off-set is added to the code segment register after shifting it by 4-bits which include base address of the code segment.

Figure shows the calculation of physical address from CS and IP



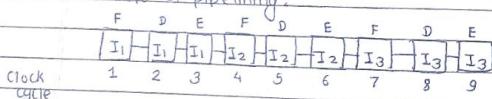
The values stored in IP is calculated called as off-set or displacement. Let us take CS=3000H and IP=0123H. Figure shows the calculation of physical address from CS and IP before adding the content of CS and IP. The content of CS is shifted by four bit positions. Now CS contains 3000H when shifted left by four bit positions, it gives 30000H which is base address of the code segment i.e. starting address. When we add off-set 0123H, the 30123H becomes 20-bit physical address of the next instruction byte to be fetched. 20-bit physical address is normally represented as CS:IP.

Stack Pointer (SP):



The 8086 allows us to set assign an entire 64 KB segment as a stack. Stack Pointer (SP) register holds the 16-bit offset of the top of the stack. The upper 16-bit of starting address of this segment is loaded in the stack segment (SS) register. Physical address of the stack is generated by adding the content of stack pointer (SP) to the stack segment (SS) base register during read or write operation with stack. So the content of SS segment is shifted left by 4 bits and then the content of SP register is added to it. For ex:- If SS contains 6000H and SP contains FFE0H after shifting SS register content by 4-bits to the left, the content is 6000H. After adding SP i.e. offset added to it, the resultant physical address for the top of the stack will be 6FFFE0H.

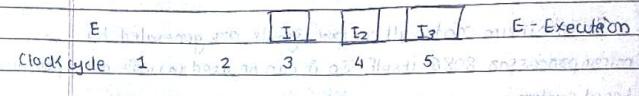
Concept of pipelining:



a) Non-pipelined processor
(Execution of 3 instructions)

F = Fetch D = Decode E = Execute

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Clock cycle 1 2 3 4 5

b) Pipelined execution of three instructions

The technique used to enable an instruction to complete with each clock cycle is known as pipelining. Normally, on a non-pipelined processor, nine clock cycles are required for fetch, decode and execute cycles for three instructions as shown in fig-a)

But on pipelined processor, the fetch, decode and execute operations are performed in parallel and only 5 clock cycles are required to execute the same three instruction as shown in fig-b). So pipelining improves the execution speed of processor.

In 8086, pipelining is implemented by providing 6-byte queue whereas three instructions can be stored in advance and then one by one, the instruction goes for decoding and execution. In this way, 8086 perform fetch, decode and execute operation in parallel i.e. in single clock cycle as shown in fig-b)

Advantages of pipelining:

- 1) Pipelining enables many instructions to be executed at the same time.
- 2) It allows execution to be done in fewer cycles.
- 3) Speeds up the execution speed of the processor.
- 4) More efficient use of the processor.

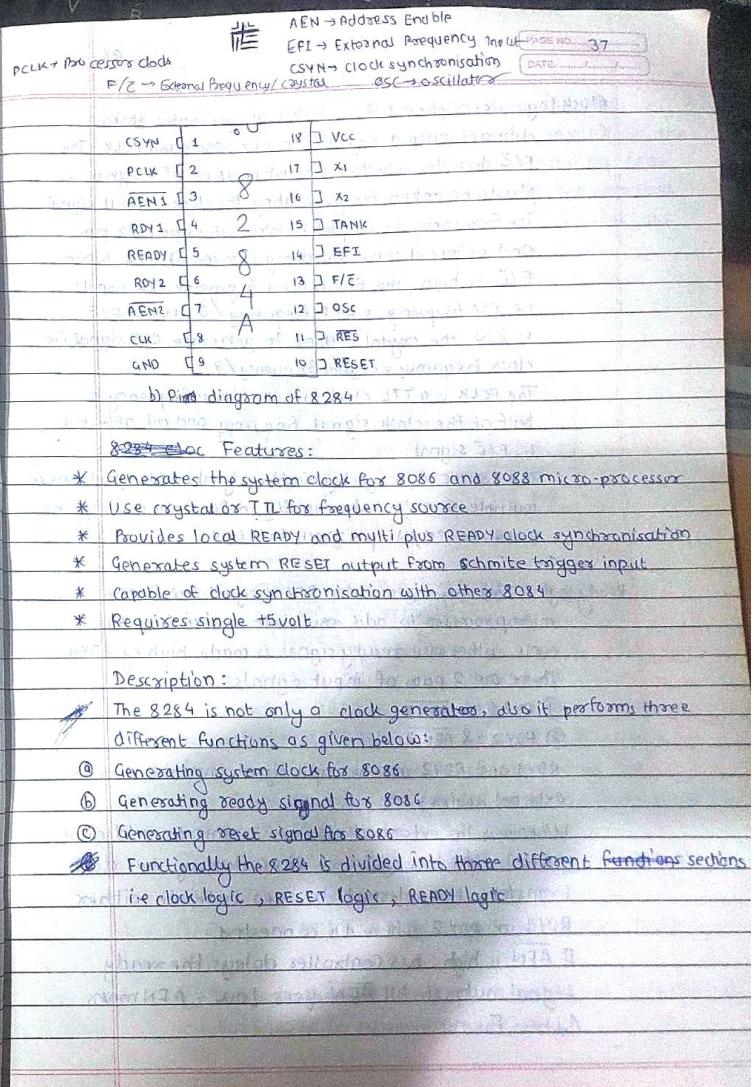
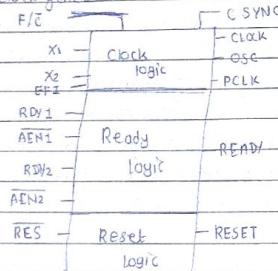
Operating modes of 8086 micro-processor:

- The microprocessor 8086 operates in two modes i.e
- Minimum mode (single-master mode)
 - Maximum mode (two-master mode)

In minimum mode, all control signals are generated by microprocessor 8086 itself. So it can be used in single microprocessor based system.

In maximum mode, all control signals are generated by bus-controller 8288 and not by microprocessor 8086. So it can be used in multiprocessor system when microprocessor based system contains external microprocessors like 8087. The pin no. 33 i.e MN/MX is used to set either minimum or maximum mode of microprocessor 8086 and also the function of pin number 24-31 will also be changed.

8284 clock generator:



Clock logic description: The clock logic generates three different output signals i.e. CLK, OSC and PCLK. The F/C decides whether crystal input or EPI signal should be taken for generating the clock output signal. The frequency of crystal is taken at X1 and X2 pins and external input frequency is taken at EPI. When F/C is high, the EPI is used to generate CLK signals i.e. $\text{CLK Frequency} = \text{EPI Frequency}/3$. When F/C is low, the crystal is used to generate CLK signal i.e. $\text{clock frequency} = \text{crystal frequency}/3$.

The PCLK is a TTL clock signal whose frequency is half of the clock signal frequency and not affected by F/C signal.

The CSYNC is a synchronization signal which synchronizes multiple 8284's but normally in PC we have only one 8284, so CSYNC pin grounded in PC.

Ready logic: This logic generates READY signal low for the microprocessors to add wait state in 8086/8088 bus cycle, otherwise ready signal is made high by 8284. There are 2 pairs of input signals:

- ① RDY1 & AEN1
- ② RDY2 & AEN2

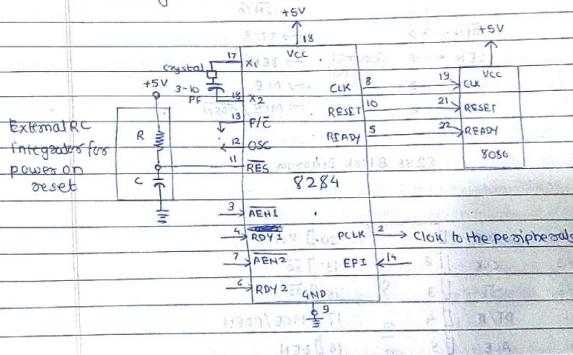
RDY1 and RDY2 are the input signals available from the external devices.

Whenever the external device wants to add wait state in the bus cycle of 8086 during the data transfer, the external devices activate either RDY1 or RDY2 where it is connected.

If AEN is high, bus controller delays the ready signal output till AEN goes low. AEN means Address Enable.

RESET logic: This logic generates RESET signal for 8086 microprocessor. When RES input pin is made low, the reset logic generates high active reset signal for 8086. In PC's, the RES input is connected to either power boot signal from SMPS or power on reset from RC low pass filters.

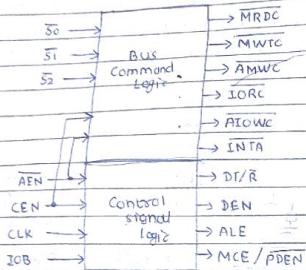
Interfacing 8284 with 8086:



8288 Bus controller: 8288 is a Bus controller IC used to generate different control signals necessary for interfacing memory and I/O devices in maximum mode of 8086. Functions of this IC are:

- ① Generate ALE signal to control the address latch 74LS373 or 8282.
- ② Generate DT/R and DEN signal transceivers 74LS245 or 8286.
- ③ Generate the READ/WRITE control signal on behalf of 8086/8088 in maximum mode.

Functionally 8288 consist of two different sections namely
Bus command logic and Control signal logic



8288 Block Diagram



Pin diagram of 8288

Signal description:

Input signals:

* S0 S1 S2 : STATUS INPUT PINS : These pins are the input pins from 8086 processors and 8288 decode this input to generate command and control signals at the appropriate time.

* CLK : CLOCK : This is a CMOS compatible input which receives a clock signal from 8284 clock generators and serves to establish when command / control signals are generated.

* AEN : ADDRESS ENABLE : AEN enables command output of 82C88 Bus Controller.

* CEN : COMMAND ENABLE : When this signal is low, all 8288 command outputs and the DEN & PDEN are forced to their inactive state. When this signal is high, these same output signals are enabled.

* IOB : INPUT/OUTPUT BUS MODE : When the IOB is strapped HIGH, the 82C88 functions in the I/O bus control. When it is strapped LOW, the 82C88 functions in the system bus mode.

Output signals:

* ALE : ADDRESS LATCH ENABLE : This signal serves to strobe an address into the address latches.

* DEN : DATA ENABLE : This signal serves to enable data transfers onto either the local or system data bus. This signal is active high.

* DT/R : DATA TRANSMIT/RECEIVE : This is output/input signal which establishes the direction of data flow through the transceivers. A high on this line indicates transmit (Write to I/O or memory) and a low indicates receive (Read from I/O or memory).

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- * **AIOWC : ADVANCED I/O WRITE COMMAND :** Bus Controller 8288 issues an I/O write command earlier in the machine cycle to give to I/O devices an early indication of write instruction.
- * **IOWC : I/O WRITE COMMAND :** This command line instructs an I/O device the data on the databus to send the data on databus. This signal is active low.
- * **IORD : I/O READ COMMAND :** This command line instructs an I/O device to drive its data onto the data bus. This signal is active low.
- * **AMWC : ADVANCED MEMORY WRITE :** The AMWC issues a memory write command earlier in the machine cycle to give memory devices an early indication of write instruction. AMWC is active low.
- * **MWTC : MEMORY WRITE COMMAND :** This command line instructs the memory to record the data present on the data bus. This signal is active low.
- * **INTA : INTERRUPT ACKNOWLEDGE :** This command line tells an interrupting device that its interrupt is acknowledged.

Bus Control logic:

PIO →

H J K L : []
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Bus status	8086 state	Command signal
00 01 10		INTA 11 Pin No. 14
00 00 00	Interrupt Acknowledge	IORD Address 13
00 00 01	Read I/O port	IOWC Address 11
00 01 00	Write I/O port	& AIOWC Address 12
01 00 10	Halt	None
11 00 00	Instruction Fetch	MRDC Address 7
11 00 01	Read Memory	MRDC Address 7
11 01 00	Write Memory	MWTC Address 9
11 10 00		AMWC Address 8
11 11 11	Passive	None

When 8086 performs a bus cycle, the appropriate command signal from 8288 becomes active low in t2 and remains low till the bus cycle is completed. The bus control logic is responsible for generating bus command signals in t2 state of every bus cycle of the CPU. It accept the bus status signals on S0, S1, S2 and decode this status signals to generate different control signals. When there is no bus cycle by the 8086, the command signals are inactive i.e. active high.

Control signal logic: The control signal logic is responsible for generating signal for controlling the hardware connected to 8086 address bus and data bus.

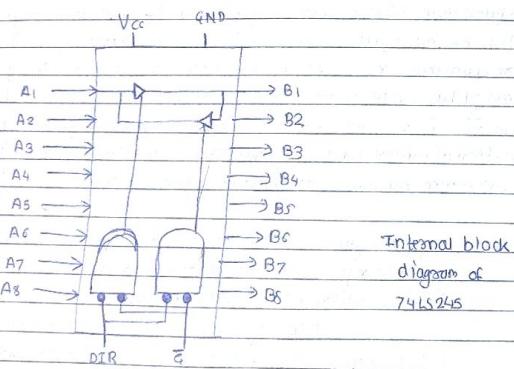
The DT/R signal is used to set the direction of data to the data bus transceivers like 74LS245 or 8286. When DT/R is high, the direction of data transfer is from 8086 to external device and DT/R is low, the direction of data transfer is from external device to 8086.

DEN signal indicated when the data bus is to be active. When DEN is high, data bus transceivers is enabled and when DEN is low, data bus transceiver is disabled and its outputs are tri-stated.

ALE signal is used to enable address latch during t1 of every buscycle of 8086.
MCE/PDEN (MASTER CASCADE ENABLE / PERIPHERAL DATA BUS ENABLER) is a dual function signal. This signal is used if more than 1 interrupt controller (8259A) is connected in cascade. If IOB is high, this pin will act as Peripheral data enable.

IF IOB IS HIGH LOW

74LS245 Bidirectional buffer:



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Vcc	G
DZR																						
A1	2																					
A2	3	7	15	16	17	18	19	20	1	2	3	4	5	6	7	8	9	10	11	12		
A3	4	5	16	17	18	19	20	1	2	3	4	5	6	7	8	9	10	11	12	13		
A4	5	6	17	18	19	20	1	2	3	4	5	6	7	8	9	10	11	12	13	14		
A5	6	7	18	19	20	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
A6	7	8	19	20	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
A7	8	9	20	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		
A8	9	10	21	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		
GND	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29		

Pin diagram of 74LS245

Enable pin 3 Discretion Control Data of data

High to Low → control DZR pin. Invert data flow
Low to High → control B-Bus to A-Bus
Low to Low → data flow from A-Bus to B-Bus
High to High → Isolation

Description: Bi-directional bus is used to increase the driving capability of data-bus and also called as active bus transceivers. The bi-directional buffers consist of 16 non-inverting buffers, 8 for each direction with tri-state outputs. The direction of data flow is controlled by DIR. When DIR pin is high, data flows from A-bus to B-bus. When DIR pin is low, data flows from B-bus to A-bus. The active low enable G and the DIR signals areanded to activate the bus lines. Each buffer can sink 24 milli Amperes and source 15 milli Amperes current.

74LS373 Octal latch

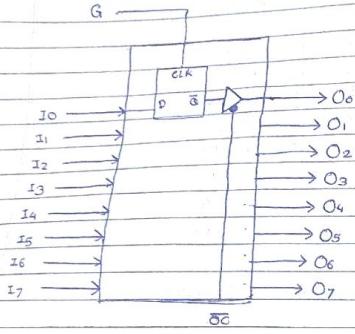
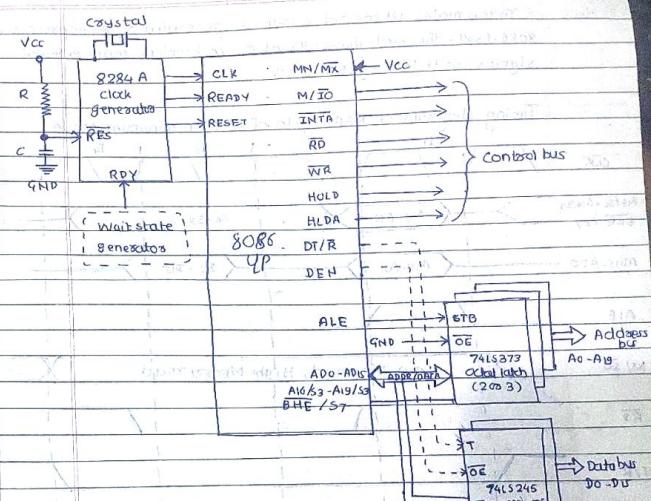


Figure shows the internal configuration of 74LS373. The eight latches are D-type latches indicating that when enable G is high, the Q output will follow D input. When enable G is low, the Q output will be latched at the level of data what is was at the input. The latch is controlled by Pclock CLK and buffer is controlled by \bar{Q}_C pin.

Minimum mode of 8086 Based system:

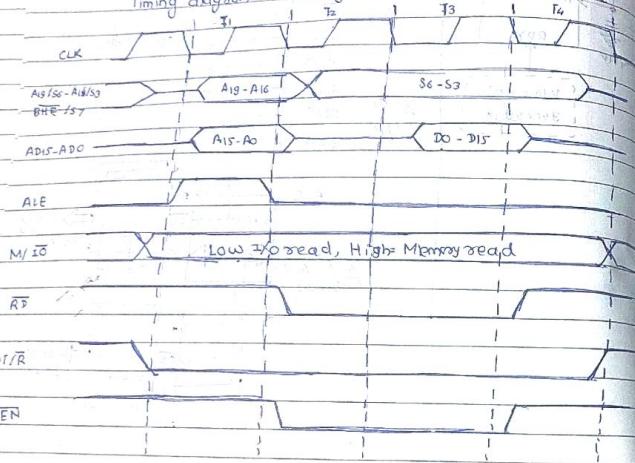


System configuration in minimum mode of 8086 CPU

The general 8086 system in minimum mode is as shown in figure. The working of minimum mode configuration can be described in terms of timing diagram which shows how and when different signals are generated by 8086. Timing diagram can be classified into two parts: Read bus cycle and Write bus cycle. In minimum mode, the 8086 based system, the microprocessor 8086 is operated by strapping its MN/MX pin to logic HIGH i.e. +5V/1T.

In this mode, all control signals are generated by microprocessor 8086 itself. The clock generator also synchronizes some external signals with the system clock.

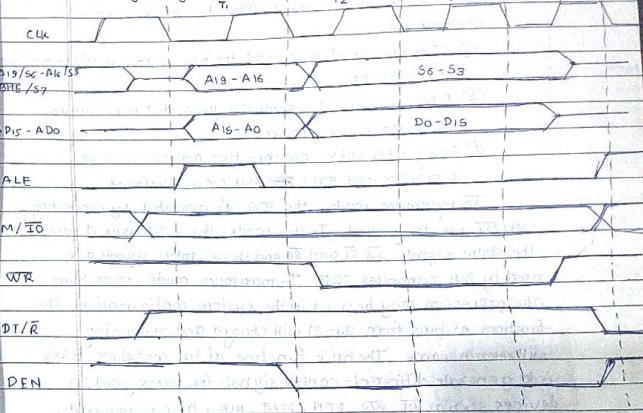
Timing diagram of READ cycle of 8086 in minimum mode



The read bus cycle begins in T₁ with the assertion of ALE and M/I_O signals. During the falling edge of ALE signal, the valid address is latched on the local address bus A₀-A₁₉. The BHE and A₀ signals address low, high or both bytes.

From T₁ to T₄, the M/I_O signal indicates a memory or I/O related operation. At T₂, the address signals are removed from the address bus and sent to the output to the latches which latches address on A₀-A₁₉ lines. The bus is then tri-stated. The control signal RD is activated in T₂ causes a addressed device to enable its data bus. After RD goes low, the valid data is available on the data bus.

Timing diagram of WRITE cycle of 8086 in minimum mode:



The write bus cycle begins in T₁ with the assertion of ALE signal and M/I_O signal. During the falling edge of ALE signal, the valid address is latched on the local address bus A₀-A₁₉. The BHE and A₀ signals is activated to read or write lower byte, higher byte or both bytes.

The M/I_O signal is used to distinguish between a memory or I/O related operation from T₁ to T₄ clock cycle. During T₂ clock cycle, the address signals are removed from the address bus and sends to the latches which latches address on A₀-A₁₉ lines. The control signal WR is activated in T₂ causes a addressed device to enable its data bus. After WR goes low, the valid data is available on the data bus from which it is written to the memory or I/O devices.

CEN = Cascade enable
 AEN = Address enable
 IOB = I/O bus

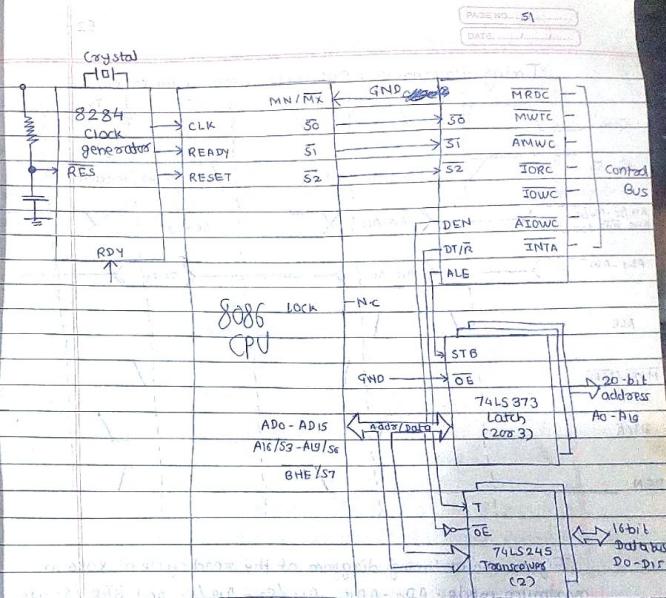
Maximum mode of 8086 based system:

Importance of maximum mode: Used in microprocessor environment.

- ② 8288 bus controller is used for bus control in multi-processor environment.
- ③ Advanced control signals are generated in maximum mode for slower devices.
- ④ Along with 8086, another two masters i.e. DMA controllers and 8087 ALU can be interfaced.

In maximum mode, the 8086 is operated by connecting MN/MX pin to ground. In this mode, the processor derives the status signals S2, S1 and S0 and these status signals are used by bus controller 8288. In maximum mode, more than one processor may be used in the system configuration. The functions of pins from 24-31 will change and remaining will remain same. The basic function of bus controller 8288 is to generate different control signals from memory and I/O devices such as RD, WR, DEN, DT/R, ALE. Also it generates the signals MRDC, MWTC, AMWC, IORC, ~~IOWC~~, AIOWC.

The AEN, IOB and CEN pins are especially useful for multiprocessor system. INTA pin is used to generate interrupt acknowledge. IORC and IOWC are used to read data from I/O device and write data from I/O devices respectively. The MRDC and MWTC are used as memory read and write signal. Beside this signals, AIOWC and AMWC advanced control signals are available to serve some purpose as IOWC and MWTC but are activated one clock pulse earlier.



Timing diagram of READ cycle in maximum mode

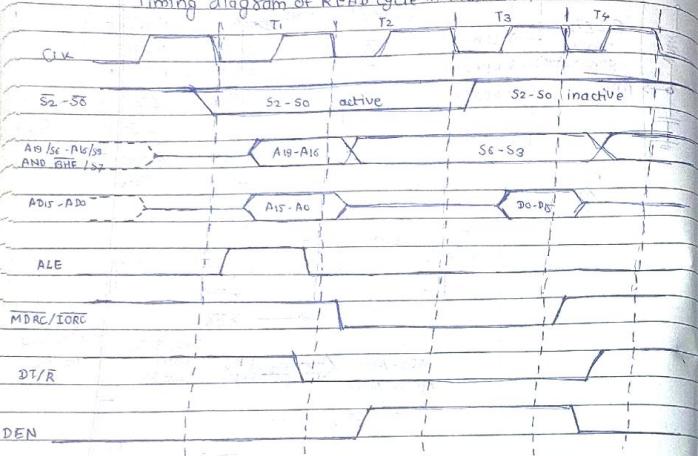


Figure shows timing diagram of the read cycle of 8086 in maximum mode. AD₁₅-AD₀, A₁₆/S₃-A₁₉/S₆ and BHE/S₇ are generated by the microprocessor during T₁ of read cycle. But DT/R, ALE, DEN and control signals IORC / MRDC are generated by 8288 bus controller after receiving status signals on status lines S₀, S₁ and S₂ in T₂ and T₃. The ALF is generated by 8288 during T₁ state of the read bus cycle. DT/R, DEN and MRDC or IORC are generated during T₂ state by bus controller 8288 and make data available on the data bus D₀-D₁₅.

Timing diagram of WRITE cycle in maximum mode

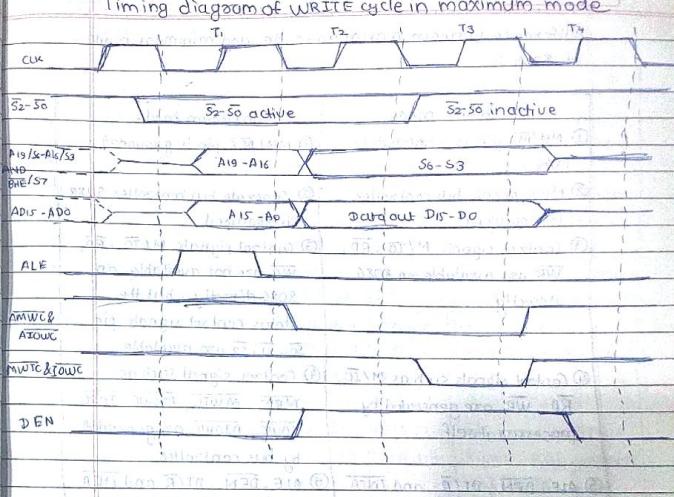


Figure shows timing diagram of the write cycle of 8086 in maximum mode. In this mode, the control signal MWTC or IOWC is generated by 8288 bus controller to write data to the memory or I/O device during T₂ state of the write bus cycle. AD₁₅-AD₀, A₁₆/S₃-A₁₉/S₆ and BHE/S₇ are generated by the microprocessor during T₁ of read cycle. But DT/R, ALE, DEN and control signals MWTC /IOWC are generated by 8288 bus controller after receiving status signals on status lines S₀, S₁ and S₂. The ALE is generated by 8288 during T₁ state of the read bus cycle. DT/R, DEN and MWTC or IOWC are generated during T₂ state by bus controller 8288 and make data available on the data bus D₀-D₁₅.

Difference between maximum mode and minimum mode of 8086:

Minimum mode	Maximum mode
① MN/MX pin is connected to Vcc	① MN/MX pin is grounded
② No separate bus controller is required	② Separate bus controllers 8288 is required
③ Control signals M/I _O , RD, WR are available on 8086 directly	③ Control signals M/I _O , RD, WR are not available on 8086 directly, but the status control signals pin 50, 51, 52 are available
④ Control signals such as M/I _O , RD, WR are generated by processor itself	④ Control signal such as MRDC, MWTC, AMWC, TARC, IOWC, AIOWC are generated by bus controller
⑤ ALE, DEN, DT/R and INTA signals are directly available	⑤ ALE, DEN, DT/R and INTA signals are not directly available and are generated by bus controller 8288
⑥ HOLD, HLDA signals are available	⑥ RD/GTO, RDI/GTI
⑦ Status of instruction queue is not available	⑦ Status of instruction queue is available on pins QSO & QSI

Difference between 8085 & 8086 4P:

No.	Parameters	8085 4P	8086 4P
1)	No. of address lines	Address bus is 16 bit $2^{16} = 64\text{ KB memory}$	Address bus is 20 bit $2^{20} = 1\text{ MB memory}$
2)	No. of data lines	Data bus is 8-bit hence it is called as 8-bit microprocessors	Data bus is 16-bit hence it is called as 16-bit microprocessors
3)	Registers	General purpose registers of 8-bit size	General purpose registers of 16-bit size
4)	Hardware interrupts	5 hardware interrupts i.e. TRAP, RST 3-5, RST 6-5, RST 7-5 and INTA.	Only two hardware interrupts i.e. NMI & INTR
5)	Behaviour of INTA after INTR	In response to INTR signal, 8085 generates three INTA pulses	In response to INTR signal, 8086 generates two INTA pulses
6)	Operating modes	Operates only in single mode	Operates in two modes i.e. maximum & minimum mode
7)	Instruction Queue	Instruction queue is not present	6-byte instruction queue is present
8)	Memory management technique	Do not support segmentation memory management technique	Support segmentation memory management technique
9)	Addressing mode	5 addressing modes	24 addressing modes
10)	Software interrupt	8 software interrupts i.e. RST 0 to RST 7	256 software interrupts i.e. INTO to INTFFH
11)	Pipeline	Does not support pipelining	Support pipelining to improve speed
12)	Frequency of operation	Operating frequency range is 500 kHz to 3 MHz	Operating frequency range is 5 MHz, 8 MHz and 10 MHz