

1. Description

1.1. Project

Project Name	PI_Drop_Tower
Board Name	NUCLEO-L432KC
Generated with:	STM32CubeMX 6.8.1
Date	05/30/2023

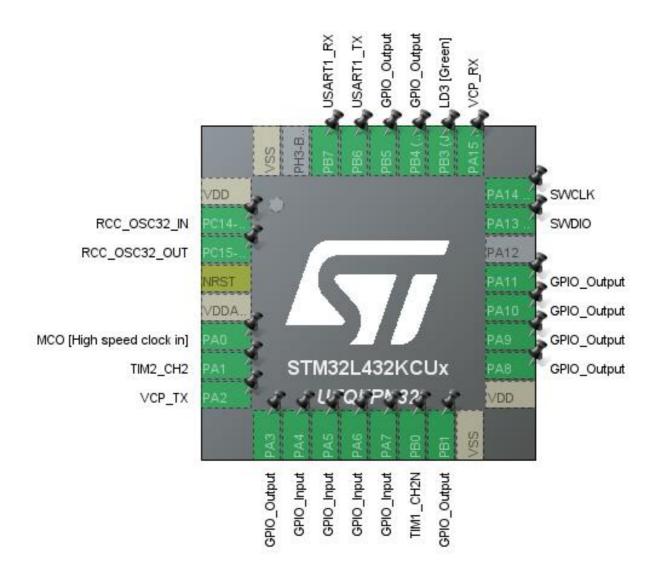
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x2
MCU name	STM32L432KCUx
MCU Package	UFQFPN32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

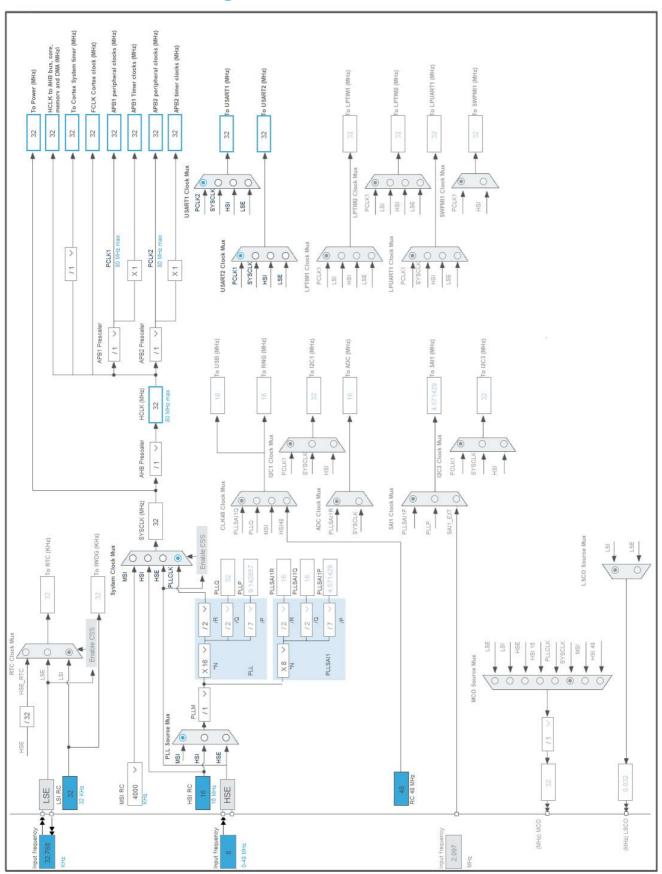


3. Pins Configuration

Pin Number UFQFPN32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
3	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	RCC_CK_IN	MCO [High speed clock in]
7	PA1	I/O	TIM2_CH2	
8	PA2	I/O	USART2_TX	VCP_TX
9	PA3 *	I/O	GPIO_Output	
10	PA4 *	I/O	GPIO_Input	
11	PA5 *	I/O	GPIO_Input	
12	PA6 *	I/O	GPIO_Input	
13	PA7 *	I/O	GPIO_Input	
14	PB0	I/O	TIM1_CH2N	
15	PB1 *	I/O	GPIO_Output	
16	VSS	Power		
17	VDD	Power		
18	PA8 *	I/O	GPIO_Output	
19	PA9 *	I/O	GPIO_Output	
20	PA10 *	I/O	GPIO_Output	
21	PA11 *	I/O	GPIO_Output	
23	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	SWCLK
25	PA15 (JTDI)	I/O	USART2_RX	VCP_RX
26	PB3 (JTDO-TRACESWO) *	I/O	GPIO_Output	LD3 [Green]
27	PB4 (NJTRST) *	I/O	GPIO_Output	
28	PB5 *	I/O	GPIO_Output	
29	PB6	I/O	USART1_TX	
30	PB7	I/O	USART1_RX	
32	VSS	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	PI_Drop_Tower	
Project Folder	C:\Users\samue\STM32CubeIDE\workspace_1.12.1\PI_drop_tower_git\PI_Drop_	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART2_UART_Init	USART2
4	MX_TIM6_Init	TIM6
5	MX_USART1_UART_Init	USART1
6	MX_TIM1_Init	TIM1
7	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x2
мси	STM32L432KCUx
Datasheet	DS11451_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

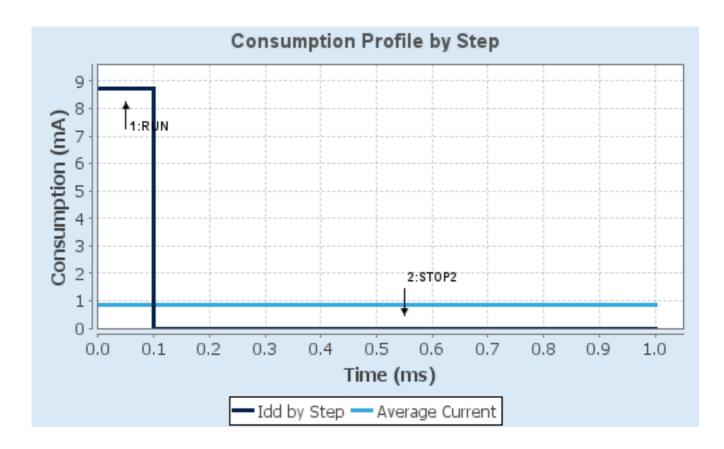
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.71 mA	1.06 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.98	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	871.95 μA
Battery Life	5 months, 9 days,	Average DMIPS	100.0 DMIPS
	16 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

mode: High Speed Clock (HSE)

Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

MSI Calibration Value 0

MSI Auto Calibration Enabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

LSE Drive Capability

LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.3. TIM1

Clock Source: Internal Clock
Channel2: PWM Generation CH2N

7.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 16-1 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 1000-1 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

BRK Sources Configuration

Digital InputCOMP1DisableCOMP2Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

BRK2 Sources Configuration

Digital InputCOMP1DisableCOMP2Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

Clear Input:

Clear Input Source Disable

PWM Generation Channel 2N:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CHN Polarity High
CHN Idle State Reset

7.4. TIM2

Clock Source: Internal Clock
Channel2: PWM Generation CH2

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 16-1 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 1000 *

Internal Clock Division (CKD) No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Disable

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

auto-reload preload

Clear Input Source Disable

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

7.5. TIM6

mode: Activated

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

auto-reload preload

Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx_EGR)

7.6. USART1

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 9 Bits (including Parity) *

Parity Even *

Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

7.7. USART2

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable

TX Pin Active Level Inversion Disable

RX Pin Active Level Inversion Disable

Data Inversion Disable

TX and RX Pins Swapping Disable

Overrun Enable
DMA on RX Error Enable
MSB First Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
	PA0	RCC_CK_IN	n/a	n/a	n/a	MCO [High speed clock in]
SYS	PA13 (JTMS- SWDIO)	SYS_JTMS- SWDIO	n/a	n/a	n/a	SWDIO
	PA14 (JTCK- SWCLK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	SWCLK
TIM1	PB0	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	VCP_TX
	PA15 (JTDI)	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	VCP_RX
GPIO	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO- TRACESWO	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Green]
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Prefetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	0	0		
USART1 global interrupt	true	0	0		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	true	0	0		
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused				
Flash global interrupt	unused				
RCC global interrupt	unused				
TIM1 break interrupt and TIM15 global interrupt	unused				
TIM1 update interrupt and TIM16 global interrupt	unused				
TIM1 trigger and commutation interrupts	unused				
TIM1 capture compare interrupt	unused				
TIM2 global interrupt	unused				
USART2 global interrupt	unused				
FPU global interrupt	unused				

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART1 global interrupt	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler	
	sequence ordering	handler		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	false	true	true	

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current

			Middleware			
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA		TIM1 ❷	USART1 ♥			
GРЮ ⊘		TIM2 ⊘	USART2 ♥			
NVIC ⊘		тім6 🤡				
RCC ♥						
sys 🗸						

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32l4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32l4_ibis.zip

System View https://www.st.com/resource/en/svd/stm32l4_svd.zip

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BSDL files https://www.st.com/resource/en/bsdl_model/stm32l4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32l4_ibis.zip

System View https://www.st.com/resource/en/svd/stm32l4_svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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tools_portfolio.pdf

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onal-safety-packages.pdf

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pres.pdf

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stm8_software_development_tools.pdf

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I462e-cell1_discovery_cellular_kit_product_overview.pdf

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discharge-sensitivity-measurement-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2606-stm32-

microcontroller-system-memory-boot-mode-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2639-soldering-

recommendations-and-package-information-for-leadfree-ecopack-mcus-

and-mpus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2834-how-to-get-the-

best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf

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design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf

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waveform-generation-using-the-dac-in-stm32-products-

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used-in-the-stm32-bootloader-stmicroelectronics.pdf

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used-in-the-stm32-bootloader-stmicroelectronics.pdf

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protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

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number-of-touchkeys-for-touch-sensing-applications-on-mcus-

stmicroelectronics.pdf

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- hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
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