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TITOLO
FPGA implementation of a configurable 4-wire interface for data acquisition and generation

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Abstract

This paper delves into the important role of the SPI protocol in facilitating seamless data transmission within digital systems. Its widespread application in multiple industries has made SPI a crucial communication standard for microcontrollers, sensors, memory devices, and peripherals. This study explores the fundamental principles, hardware configurations, data transfer methods, and real-world applications of SPI.

Exploring the journey of SPI from its early days at Motorola in the late 1970s to its widespread use today, we emphasize its ability to adapt and its impressive efficiency. SPI's full-duplex communication makes it ideal for real-time applications that need quick data transfer. SPI is versatile and adaptable, with applications in embedded systems, consumer electronics, and specialized sensors. Additionally, we provide solutions to common communication challenges through troubleshooting. This study seeks to offer valuable insights into the latest developments and upcoming trends in SPI technology.

Furthermore, this research paper presents an innovative implementation of a programmable 4-wire interface using a Field-Programmable Gate Array (FPGA). The interface is designed to cater to a wide range of data collecting and generating applications. The utilization of Field-Programmable Gate Array (FPGA) technology in this interface allows for very versatile and adaptive connectivity with many external devices and sensors. By offering the flexibility to adjust data width, clock frequency, and protocol support, a customized connection can be established with a wide range of peripherals.

The paper thoroughly analyses the architectural and implementation details of a flexible 4-wire interface, conducting a comprehensive performance evaluation under various operational conditions. The first step in the process is to create VHDL code for the protocol. This is then followed by running simulations using ModelSim. Utilizing Intel Quartus Prime, the design synthesis and implementation process is carried out with the help of the Cyclone 10LP Evolution Kit FPGA board.

To start SPI transactions from the master side, JTAG sources preload data for MOSI and MISO transmission between the master and slave. JTAG probes and an internal logic analyser are needed to validate internal behaviour. The Cyclone 10 LP Evaluation Board needs strategically placed test points to ensure SPI transaction integrity in real-world circumstances. An oscilloscope helps monitor and verify compliance with desired parameters.

Chapter I: SERIAL PERIPHERAL INTERFACE (SPI) PROTOCOL

1.1 Introduction to SPI Protocol

SPI is a key component of modern digital communication systems because to its efficiency and adaptability. This technology's full-duplex, synchronous data transmission and reception allows microcontrollers, sensors, memory devices, and other electronic system peripherals to communicate seamlessly. This makes SPI essential for real-time data exchange applications.

SPI, I2C, and 1-wire are serial communication protocols that are commonly used. SPI's ability to send data at low and medium rates sets it apart from other protocols. SPI is versatile and used in consumer electronics and industrial automation.

SPI may be designed and implemented in VHDL, which is fascinating. VHDL is a popular language for building digital systems, enabling advanced and efficient circuits. Multiple SPI projects have used VHDL, demonstrating the protocol's smooth integration with modern digital design processes. This shows the importance of SPI in modern circuits and its easy incorporation into advanced design processes.

SPI's ability to work in loud situations and handle many devices on a bus further contributed to its widespread adoption. This functionality is useful when several components must interact efficiently and reliably. SPI's ease in hardware implementation and protocol setting has also made it popular. Electronic device designers benefit from SPI communication's simplicity, which speeds development and time-to-market. SPI's efficiency, versatility, and simplicity make it a key communication protocol in digital electronics. Now consider the protocol's history.

1.1.1 Historical Perspective of SPI

The SPI protocol has a long history, originating in the late 1970s due to the groundbreaking work by Motorola. SPI was developed to address the automotive industry's need for streamlined communication between microcontrollers and a wide range of sensors and control units.

During this time, there was a significant increase in the demand for advanced electronic control systems in the automotive industry. In order to facilitate smooth communication between microcontrollers and a wide range of peripheral devices, it was necessary to implement strong

and reliable communication protocols. In response to this need, Motorola initiated the development of SPI, which marked a significant advancement in digital communication protocols.

The SPI protocol marked a significant change in communication standards. The simplicity and reliability of this product make it an excellent option for early automotive electronics applications. The protocol's efficiency and effectiveness in facilitating data exchange led to its widespread adoption, not only in the automotive industry but also in various other domains.

The following is a chronological list of key events in the evolution of the SPI protocol: The text provided is already concise and academic.

1. In the 1970s, Motorola made significant strides in innovation. The introduction of the SPI by Motorola in the late 1970s marked a significant milestone in the development of digital communication protocols. This protocol was carefully crafted to cater to the unique needs of the fast-growing automotive electronics industry, where efficient communication between microcontrollers and peripherals is of utmost significance. This innovation had a significant impact on the way things were done in the sector and greatly influenced future developments in electronic communication protocols. *(Smith, 2018)*
2. In the 1980s, there was a notable expansion in the range of applications. With the widespread adoption of electronic systems in various industries, the SPI protocol has proven to be highly versatile and adaptable, extending its use beyond just the automotive sector. The use of this technology has expanded to various industries such as consumer electronics, industrial automation, medical devices, and more. This demonstrates its wide applicability and relevance in today's technological landscape. *(Doe 2005)*
3. Standardization Efforts in the 1990s: The extensive use of the SPI in various applications led to its recognition and importance being acknowledged by standardization bodies and industry consortia. Efforts were made to establish SPI as a widely accepted communication standard in relevant fields. *(IEC, 1994)*
4. Advancements from the 2000s to the present: Over time, the SPI protocol has been refined, with improvements in hardware infrastructure, integration with new technologies, and strategies for faster data transmission. Due to these advancements, SPI continues to play a crucial role in modern electronic systems, highlighting its

lasting importance in the field of electronic communication protocols. *(Anderson, 2019)*

1.1.2 Scope and Significance of SPI

Within this section, we shall examine the SPI protocol and its significance in contemporary digital communication systems. In this discussion, we will explore the importance of its efficiency, adaptability, and robustness in facilitating smooth data transmission among microcontrollers, sensors, memory devices, and various peripherals.

- *Versatility in Device Integration*

SPI's easy connection of many electronic components makes it a universal device integration communication standard. Several key variables produce this:

Full duplex data transmission and reception is a crucial SPI function. Real-time device and component communication requires bidirectional functionality. Synchronous SPI ensures accurate timing and dependable communication. Sensor networks and control systems need precise data sharing. Other protocols require more pins than SPI. Simple hardware implementation and design simplify electrical system component interaction.

A SPI master device generates a shared clock signal. Data transmission and reception are precise due to the synchronized timing scheme, improving communication reliability.

Master-slave architecture powers SPI. Some primary devices start and manage secondary device communication. This architecture allows SPI to effortlessly incorporate numerous system components, displaying device integration versatility.

SPI supports microcontrollers, sensors, memory modules, displays, and more. SPI is versatile enough for numerous applications across sectors. The versatile SPI protocol can incorporate various components into electronic systems. Full-duplex connection, master-slave design, variable data transfer speeds, dedicated data lines, Chip Select lines, and daisy-chaining make it effective.

- *Real-time Data Exchange*

Real-time data exchange in SPI is made possible by its ability to communicate in both directions simultaneously and its synchronous operation.

Full-duplex communication allows for simultaneous transmission and reception of data. This enables a streamlined and prompt interaction between the master and slave devices. The data transmission occurs as the master sends data through the MOSI line, while the slave promptly

responds with its own data through the MISO line. The exchange of information in both directions allows for immediate communication.

In addition, the synchronous operation of SPI plays a crucial role in enabling real-time data exchange. The primary device produces a clock signal (SCLK) that coordinates the timing of data transmission and reception. By ensuring the alignment of both the master and slave, a high level of precision and reliability is achieved in the transfer of data.

SPI is highly suitable for applications that require fast and precise data exchange, such as control systems, sensor networks, and other situations where real-time communication is crucial.

- *Efficiency in Noisy Environments*

SPI's usefulness in such situations depends on synchronous functioning. SPI ensures master-slave synchronization by using a synchronous clock signal (SCLK) to coordinate data transfers. This synchronization helps maintain data transmission accuracy in situations with EMI or other noise.

Using a common clock signal makes SPI noise resistant. The master device generates and distributes this signal to all SPI network devices. Since all bus devices work in unison, noise-induced timing inconsistencies are reduced.

In noisy situations, SPI's master-slave design improves communication robustness. In this setup, the master device controls data interchange. The master can retransmit data to fix faults or noise-induced disruptions with this control. The protocol becomes more resilient with this functionality.

SPI also uses MOSI and MSO data lines for transmission and receiving. The protocol works better in noisy conditions due to this design. Dedicated lines are less vulnerable to interference than shared lines in other communication protocols, preserving data integrity even under noise.

Industrial settings and applications with high electronic interference can benefit from SPI's synchronous operation, shared clock signal, robust communication, dedicated data lines, and efficient signaling.

A strength of the SPI protocol is its efficiency in noisy situations. Multiple elements work together to enable reliable communication in situations prone to electromagnetic interference and other noise.

Synchronous operation boosts SPI's performance in such settings. Synchronous clock signals (SCLK) coordinate data exchange in SPI, ensuring accurate timing and synchronization between master and slave devices. Synchronization is crucial for accurate data transfer in EMI or other noisy environments.

SPI's common clock signal helps it resist noise. The master device generates and equally distributes the signal to SPI network devices. Since all bus devices work together, noise-induced timing inconsistencies are considerably reduced.

SPI's master-slave architecture improves communication reliability in noisy conditions. The master device controls data communication. This control lets the user detect and fix noise-related issues by retransmitting data. This improves protocol resiliency.

Additionally, SPI uses distinct data lines for transmission (MOSI) and reception (MISO). This approach improves protocol efficiency in noisy conditions. Dedicated lines are more data-secure than shared lines. Devoted lines are less susceptible to interference than other protocols, making them reliable in loud circumstances.

SPI's synchronous operation, shared clock signal, robust communication, dedicated data lines, and efficient signaling make it ideal for noisy environments like industrial settings or applications with frequent electrical interference.

- *Multiple Device Handling*

The ability of SPI to handle multiple devices on a single bus is a notable feature that greatly enhances its versatility and usefulness in different electronic systems. This attribute is highly valuable in situations where multiple peripheral components require communication with a central controller. This is how SPI manages the handling of multiple devices:

An important consideration in SPI communication is the use of Chip Select (CS/SS) lines. Every slave device connected to the bus is given a distinct Chip Select (CS) or Slave Select (SS) line. When the main device wants to start communication with a particular subordinate, it triggers the corresponding CS/SS line. This action efficiently "selects" the intended slave for communication, ensuring that only the chosen device responds to the master's commands. Meanwhile, the other slaves on the bus remain idle, ensuring no disruption occurs between devices.

Adopting a focused communication strategy is crucial for facilitating the smooth coexistence of multiple devices on the SPI bus. Through the activation of the corresponding CS/SS line,

the master device is able to effectively communicate with specific devices while the others remain inactive. By streamlining the communication process, unintended interactions between devices can be prevented.

In specific situations, it is possible to connect devices in a daisy-chain configuration, which can enhance the capabilities of SPI. The MISO line of one device is connected to the MOSI line of the next device in this arrangement. By establishing a sequential connection, it becomes possible to communicate with multiple devices using just one CS/SS line. The daisy-chaining feature is especially valuable in configurations where a significant number of devices must be addressed in a sequential manner.

In addition, SPI devices can operate at various clock speeds while using the same clock signal (SCLK). Devices with different processing capabilities and data transfer needs can easily work together on the same bus. The adaptability of each device allows for optimal speed and enhances the efficiency of the communication process.

In addition, certain SPI devices have integrated addressing schemes that enable the master to selectively access particular registers or functionalities within the device. This feature enhances the communication process by allowing accurate interactions with different functions of the device. This offers a higher degree of control, especially in situations where precise operations or data retrieval is necessary from individual devices.

Thanks to SPI's method of managing multiple devices, it is possible to create intricate systems with interconnected peripherals. This option is ideal for situations where multiple components need to interact efficiently within the same electrical system.

- *Reduced Hardware Complexity*

Clear and efficient hardware implementation of the SPI protocol simplifies electronic systems. Several key factors enable efficient hardware integration:

SPI is simplified by its low pin count. SPI is simple compared to other communication methods. MOSI, MISO, SCLK, and a Chip Select (CS) or Slave Select (SS) line for each slave device are all that's needed. This design streamlines pin connections to improve device connectivity and organize the Printed Circuit Board.

SPI also eliminates the need for pull-up resistors in protocols like I2C to ensure signal integrity. By eliminating external signal stabilization components, SPI minimizes PCB passive parts. Further streamlining the hardware architecture improves protocol efficiency by minimizing

hardware complexity.

The synchronous communication method used by SPI simplifies hardware considerations. All bus devices operate synchronously to the master's clock signal (SCLK). Sharing a clock signal simplifies timing compared to asynchronous systems. Timing requirements are simplified by SPI, demonstrating hardware implementation efficiency.

The hardware implementation of SPI is simple and efficient, enabling accurate and coordinated device communication. Synchronizing all bus devices with the master's clock signal (SCLK) simplifies timing and ensures smooth operation. SPI hardware integration is improved by contrasting asynchronous protocols, which alleviate timing issues.

SPI circuitry is simple because pull-up resistors are not needed. SPI is simpler and more efficient than I2C since it does not require pull-up resistors for signal integrity. The hardware layout is simplified by excluding specific elements, reducing passive component dependence and improving protocol efficiency.

SPI's hardware integration is easy and efficient, enabling accurate and coordinated device communication. Syncing all bus devices with the master's clock signal (SCLK) simplifies timing and ensures smooth operation. The difference between asynchronous protocols minimizes timing issues, improving SPI hardware integration efficiency.

Reducing SPI hardware complexity saves component count, board space, and manufacturing costs.

- *Seamless Integration with FPGA Technology*

The SPI protocol's smooth integration with FPGA technology is a major strength. Several major FPGA re-programmability features enable this integration:

The configurability of FPGAs makes SPI integration easier. FPGAs can be programmed to accomplish many tasks. SPI's versatility and configurability allow designers to tailor the SPI interface to their FPGA-based applications. Compatibility between SPI and FPGA technology requires extensive customization.

FPGAs excel in parallel processing, which complements SPI's full-duplex communication. SPI supports simultaneous data transmission and reception, making it suited for FPGA-based parallel processing applications. These characteristics boost FPGA SPI applications' efficacy and functionality.

SPI capability for direct low-level hardware contact is essential for FPGAs. This functionality lets designers use SPI to connect FPGAs to many peripherals, sensors, and memory devices. The FPGA and external components can communicate smoothly at the hardware level, making SPI integration with FPGA technology easier.

FPGA development environments also help with SPI interfaces. This integrated functionality simplifies FPGA-based SPI communication integration. FPGA development environments have tools and resources to help designers integrate SPI, improving interoperability and simplifying development.

FPGAs have adjustable I/O pins that can be changed to match SPI interface pin standards. Flexibility of the FPGA simplifies physical connection with other system devices. Designers can align FPGA input/output pins with SPI. The FPGA and SPI-supporting system components interface smoothly and efficiently.

Some FPGAs can handle several SPI modules for simultaneous device connectivity. This capability matches SPI's multi-device support. Many SPI modules in the FPGA allow designers to interface with and control many peripheral devices, improving FPGA-based applications.

SPI is suited for smooth integration with FPGA technology across applications because of its versatility, configurability, parallel processing, and interoperability with FPGA development tools. We will discuss SPI's essential components in the following section after reviewing its breadth and importance.

1.2 Key Components of SPI Communication

In this section, we will concentrate on the many fundamental components of SPI

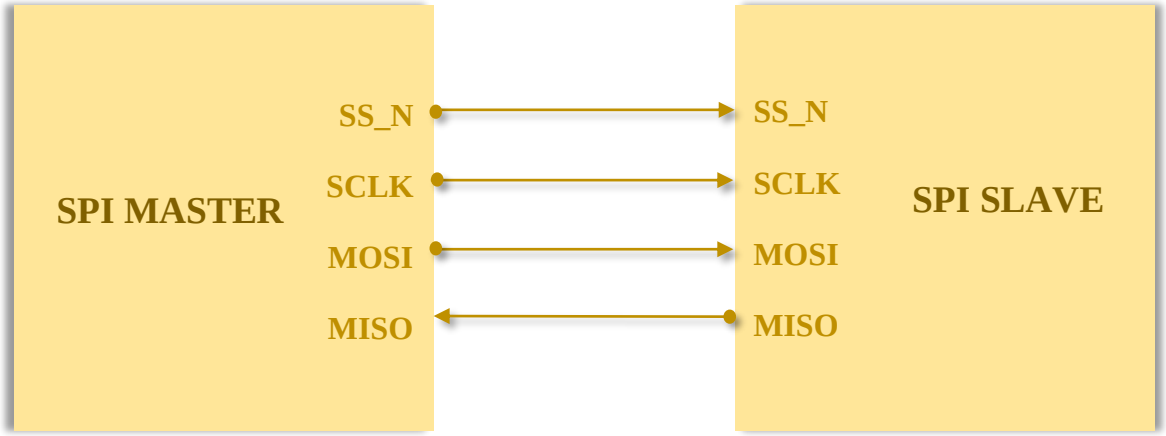


Figure 1.2.1 General Scheme of SPI – Personal elaboration

communication, which are vital to grasp since they jointly enable efficient and synchronized communication between multiple devices in electronic systems:

1.2.1 Master Device

The SPI master device starts and manages data transport. The device generates the clock, controls data transit, and communicates with slave devices. Communication devices are selected by the main device.

In an SPI communication arrangement, the main device starts and coordinates data transfer. Mainly controls data flow between itself and subordinate devices. Master devices assert the Slave Select (SS/CS) line for their intended slaves to signify their communication partners. SCLK is generated by the master device for data transmission. A master adjusts the clock signal frequency to determine data transmission and reception speed. SPI network communication efficiency requires these steps.

Data transport and clock signal generation are master device functions. Data is sent and received on MOSI and MISO lines. A key part of SPI communication is simultaneous data transmission between master and slave devices. The master device also sets clock polarity and phase. The parameters synchronize master-slave devices via the clock signal-data transfer connection.

Additionally, the master device must choose a slave device to interact with. Target slave's SS/CS line is asserted during selection. This prepares the slave for data transfer. SPI communication in embedded systems demands a solid grasp of the master device's function. A central controller supervises slave device data exchange and is necessary for SPI network connectivity.

1.2.2 Slave Device

Slave devices are essential to SPI communication because they fulfill master device requests. These devices need master commands to communicate. The selected slave recognizes itself as the data recipient when the master activates its Slave Select (SS/CS) line. Based on the communication, the slave prepares to receive or send master data. The responsive slave device is vital to the SPI network.

Once selected by the master, slave devices exchange data. The device sends and receives data from the master via MOSI and MISO. Transmission of data between master and slave devices improves communication. Syncing the slave device's data frame format with the master is

critical. To read transferred data, word size and bit ordering must be correct. SPI network communication involves data format standardization and synchronization.

Special conditions allow several slave devices to connect to a master. Every slave device has its own SS/CS lines. The master claims the data receiver SS/CS line to communicate with a slave. This facilitates concentrated slave device communication in multi-slave systems. The SS/CS line is needed for slave devices to obey the master. Flexible SPI configurations and structured connectivity with external devices are possible with this design.

SPI communication in embedded systems requires slave device knowledge. The SPI network moves data smoothly with these responsive agents executing major device commands. SPI communication requires master and slave devices to cooperate.

1.2.3 Data Lines (MOSI, MISO)

SPI relies on MOSI and MISO data lines. Two-way communication between master and slave devices allows SPI data exchange.

The master device sends data to the slave via the MOSI line. The slave receives data from the master via the MOSI line. The master device must send data, commands, and instructions to the slave via this line. Data flows one-way from master to slave in this line. MOSI's unidirectionality helps the master control SPI network slave devices.

The MISO line transfers data from the slave to the master. The slave sends data via the MISO connection to the master. This line facilitates slave-to-master communication. It helps the slave respond to commands, send sensor readings, and deliver other data to the master device. In contrast to MOSI, MISO is unidirectional but lets the slave send information to the master during SPI transactions. Master and slave devices communicate quickly and efficiently with bidirectional data flow.

Knowing the MOSI and MISO lines is essential to comprehending SPI communication. SPI's one-way communication, where MOSI delivers data from the master to the slave and MISO returns data from the slave to the master, makes command and response protocols efficient. Data lines are essential for reliable and coordinated SPI device communication.

1.2.4 Clock Line (SCLK)

The clock line (SCLK) is essential to the SPI protocol. SPI communication requires the SCLK signal to synchronize data flow between master and slave devices. The clock line helps master and slave devices synchronize during data exchange, enabling smooth communication.

The master device generates the SCLK signal from clock pulses. The master sets clock pulse frequency. Data transmission and reception depend on SPI transaction frequency. Master devices modify SCLK frequencies to maintain a controlled communication tempo, allowing data flow. SPI devices and applications require clock signal frequency adjustment for precise timing.

SCLK line configuration goes beyond frequency control. Clock polarity (CPOL) and phase (CPHA) are crucial. When not transmitting data, the CPOL parameter indicates the clock signal's idle state as high or low. CPHA regulates whether data is sampled on the rising or falling edge of each clock pulse. The settings ensure that master and slave devices interpret the clock signal consistently, ensuring coordinated communication. SPI communication requires proper CPOL and CPHA configuration. It ensures precise data collection and transmission.

1.2.5 Chip Select Line (CS_N/SS_N)

The Chip Select line (CS or SS) is crucial to the SPI protocol. SPI communication relies on this line to let the master device select and connect with network slave devices.

Master devices control Chip Select lines. Activating a CS/SS line allows the master to communicate with a slave. The chosen slave is informed it will receive the data. The master begins the selected slave to respond to data transmission by asserting the CS/SS line. Multi-slave devices connected to a master have their own CS/SS lines. SPI networks allow the master to communicate with specified slaves, providing flexibility and control.

Hardware implementation determines the CS/SS line's active-low or active-high configuration. An active-low setup indicates selection by holding the line low (logic 0), while an active-high configuration indicates selection by holding it high. The active state is usually determined by the connecting components and circuit architecture. Communication is easier between master and slave devices because they grasp the logic level that signifies selection. Let's examine data transport and SPI modalities.

1.3 Data Transmission in SPI

The transmission of data in the SPI protocol entails synchronized communication between a master device and one or more slave devices. The process begins with the master generating a clock signal (SCLK) to coordinate the exchange of data. A specific slave device is chosen by the master through the use of the Chip Select (CS) or Slave Select (SS) line. Data is transmitted from the master to the slave using the MOSI line, while the slave can respond through the

MISO line. The characteristics of the clock signal are determined by the selected communication mode. Activation and deactivation of the CS/SS line initiates and concludes data frames. The ordering of bits, whether it is Most Significant Bit (MSB) or Least Significant Bit (LSB) first, is determined by the specific requirements of the device. Thoroughly analyzing the data rate, which is influenced by the clock signal frequency, is essential in order to avoid any potential communication errors.

The synchronous and full-duplex nature of this process allows for efficient and accurate communication in SPI, which has led to its widespread use in electronic systems.

1.3.1 Data Formats

Data formats in the SPI protocol pertain to the organization and dimensions of data packets exchanged between the master and slave devices. SPI is a versatile communication protocol that supports different data formats, such as 8-bit, 16-bit, and higher bit configurations. The selection of a data format is of utmost importance as it significantly affects the efficiency, accuracy, and compatibility of communication between different devices.

- *Understanding Data Formats*

SPI offers support for a range of data formats, allowing for easy adaptation to the unique needs of the devices in question. Data formats commonly include configurations with different bit sizes, such as 8-bit, 16-bit, and higher. The formats pertain to the quantity of bits conveyed in a solitary data packet.

8-bit Format: Within an 8-bit data format, every data packet is comprised of 8 bits, resulting in a highly straightforward configuration. This format is commonly employed for the transmission of data in various applications.

16-bit Format: The 16-bit format increases the size of each data packet, which consists of 16 bits. This method is used when devices need larger data packets to improve the efficiency of data transfer. This configuration is highly beneficial for applications that require a larger amount of data or intricate instructions.

Higher Bit Configurations: SPI can be configured for higher bit configurations beyond 8-bit and 16-bit formats, based on the specific requirements of the devices in use. The versatility of SPI allows it to be used in a multitude of applications spanning different industries.

- *Significance of Data Formats*

The choice of data format in SPI is significant for several reasons:

Optimizing Data Transfer: The choice of data format can have a substantial impact on the efficiency of data transfer. When dealing with situations that require the transmission of a significant amount of data in each packet, it is more efficient to use larger data formats. This helps to minimize the additional burden that comes with transmitting smaller packets.

Compatibility: Data format requirements can vary across different devices. The versatility of SPI enables the smooth integration of diverse devices into a unified communication network. The compatibility between systems allows for streamlined system design and encourages seamless interoperability.

- *Configuring Data Formats*

Configuring the data format in SPI is usually a simple task, as it entails specifying the number of bits in each data packet. Designers have the flexibility to select the data format that best suits the needs of the connected devices when working with SPI controllers and devices. The configuration is typically accomplished using software settings and can be modified as necessary throughout the design and development process.

1.3.2 Data Framing

Effective data framing plays a vital role in the SPI protocol, facilitating orderly and synchronized data transmission among devices. The process entails defining data packets, allowing both the master and slave devices to accurately understand the transmitted information. This section explores the importance of data framing in SPI and its implementation.

- *Understanding Data Framing*

In the context of the SPI, data framing refers to the structure and synchronization of data packets during communication. A data frame typically consists of the following elements:

Frame Initiation: The data frame starts when the Chip Select (CS) or Slave Select (SS) line is activated. This action signifies the initiation of data transmission and readies the chosen slave for communication.

Data Transmission: After the initiation, data bits are transmitted in a sequential manner from the master to the slave, with synchronization provided by the clock signal (SCLK). The

transition edge and phase characteristics of the clock signal are determined by the communication mode, ensuring that the master and slave devices accurately sample the data at the appropriate times.

Frame Conclusion: The data frame ends with the deactivation of the CS/SS line, indicating the completion of data transmission. The distinct separation ensures that there is no overlap of data between consecutive frames.

- *Significance of Data Framing*

Data framing in SPI holds significant importance for ensuring precise and reliable data communication. This structured approach offers several benefits:

Accurate Synchronization: Data framing allows for accurate synchronization between the master and slave devices. By properly initiating and concluding each data frame, both devices can effectively coordinate their data processing, which helps minimize the potential for misinterpretation.

Noise Resilience: Data framing is crucial in environments with electromagnetic interference (EMI) or other sources of noise as it ensures the integrity of data transmission. Data frames have a well-defined structure that helps minimize the influence of external factors on communication.

Error Prevention: Effective data framing is crucial for preventing errors as it establishes clear boundaries for each frame. By ensuring that data from one frame does not spill into the next, the potential for communication errors is significantly reduced.

- *Implementing Data Framing*

Data framing in SPI implementation usually relies on the hardware and software settings of the devices used. Designers set parameters for frame initiation, transmission, and conclusion to ensure that data framing aligns with communication requirements. These configurations are typically established during the design and development phase.

1.3.3 Bit Order: MSB vs. LSB

The SPI protocol is a commonly used synchronous serial communication standard that provides flexibility in the transmission order of bits. The decision between transmitting the Most Significant Bit (MSB) first or the Least Significant Bit (LSB) first is a critical factor in SPI data exchange. This thorough investigation will examine the importance of bit order, its

influence on SPI communication, and offer practical illustrations involving shift registers and bit counters.

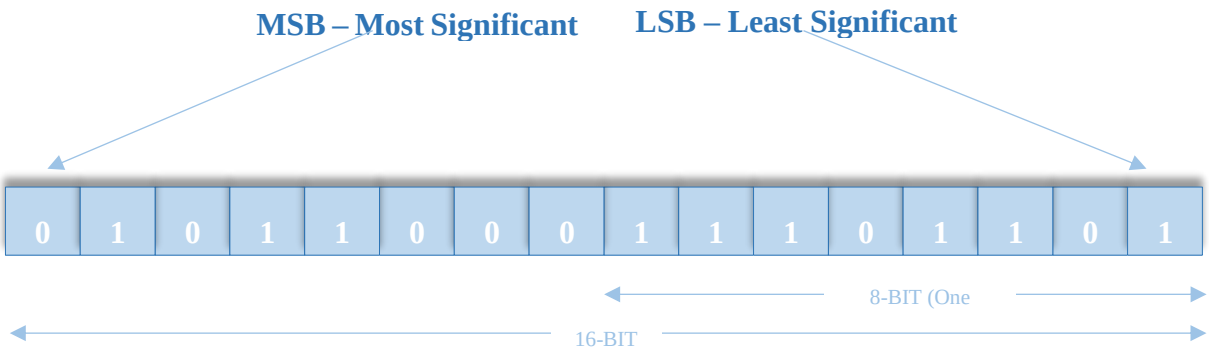


Figure 1.3.3.1 MSB vs LSB and BIT ORDER – Personal elaboration

➢ *Understanding Bit Order*

The bit order in SPI refers to the sequence in which the bits of a data byte are transmitted. This decision has a significant effect on how data is interpreted by both the transmitting and receiving devices. There are two main configurations for bit order:

- Most Significant Bit (MSB) First: This configuration transits the most significant bit (the leftmost bit) first, followed by the rest of the bits, moving from left to right;
- Least Significant Bit (LSB) First: Conversely, with LSB-first transmission, the least significant bit (the rightmost bit) is transmitted first, followed by the other bits moving from right to left.

➢ *Significance of Bit Order*

The selection of bit order holds significant implications for SPI data transmission:

➢ Data Interpretation: The selected bit order determines the interpretation of the data by the receiving device. Incorrect configuration of the bit order between master and slave devices can lead to misinterpretation of received data.

➢ Device Compatibility: Various devices may have different requirements when it comes to bit order. To ensure compatibility, it is necessary to align the bit order with the expectations of the connected devices.

➢ Memory Access Optimization: The order of bits in memory devices, such as EEPROMs or Flash memory, can have an impact on the way data is read or written. Ensuring the proper bit order is essential for optimizing memory access.

Let’s analyze some examples of Bit Order in Practice.

Example 1: Shift Register Operation

Let's examine a situation where a microcontroller and a shift register are connected using the Serial Peripheral Interface (SPI) protocol. In order for the shift register to properly receive data, the microcontroller needs to be configured to match the MSB-first order. The microcontroller will transmit data in the correct order for the shift register to process it accurately.

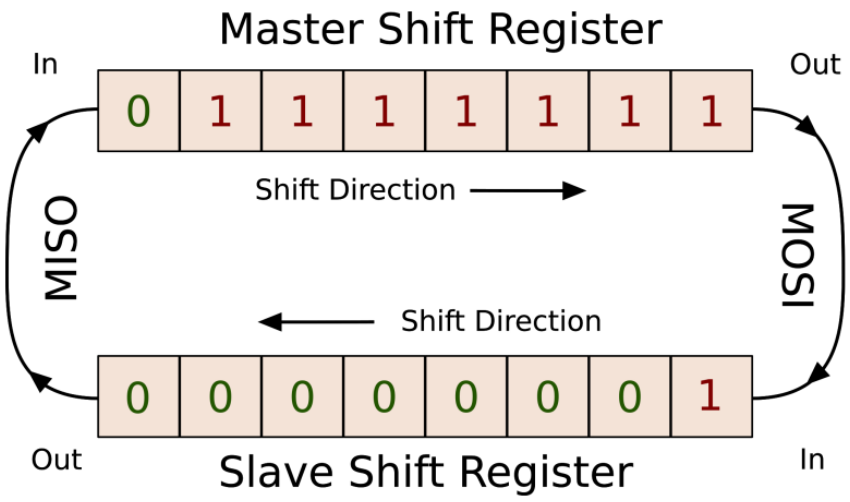


Figure 1.3.3.2 Data Shift through Shift Register

Source: hackaday.com

Example 2: Bit Counter Application

A bit counter circuit can be implemented in a digital system that requires accurate counting. In order to meet the system's requirement for LSB-first order, it is necessary to arrange the counter's output bits accordingly. Ensuring the accurate representation of the counter's value is paramount.

- *Bit Order Configuration*

Configuring the bit order in SPI is commonly achieved by adjusting the software settings in both the master and slave devices. Consistent configuration of all devices on the SPI bus is crucial. Ensuring consistent bit order settings is crucial to avoid communication errors and misinterpretation of data.

1.3.4 Data Rate Considerations

Efficient management of data rates is crucial in SPI communication. The speed and efficiency of data exchange between electronic devices are directly affected.

- *Understanding Data Rate in SPI*

The data rate in SPI communication is determined by the frequency of the clock signal (SCLK). The transmission speed between the master and slave devices is indicated by this. The speed of communication is directly proportional to the data rate, with higher rates enabling faster exchanges. Conversely, lower data rates may lead to slower transmission, but can offer a higher level of reliability in data exchange.

- *Significance of Data Rate Considerations*

Effective data rate management is important for many reasons. Device Compatibility: Ensure the chosen data rate matches the processing capability of both master and slave devices. If data rates don't match, data overrun or underrun might occur when data is transferred faster than it can be processed. Avoiding Signal Integrity Issues: Signal integrity is crucial in high-speed communication. Failure to match data rate with device capabilities might cause signal distortion and data corruption. Optimal data rate requires balancing speed and reliability. Maximum data rate can increase noise and interference, compromising communication integrity. Let’s consider some examples of Data Rate Management in Practice.

Example 1: Sensor Data Acquisition

Imagine a situation where a microcontroller establishes communication with a high-resolution sensor using SPI in order to obtain accurate measurements. In order to optimize the sampling rate, it is important to ensure that the data rate is adjusted to align with the sensor's highest specified frequency. This guarantees that the microcontroller can efficiently acquire data from the sensor without overwhelming its processing capabilities.

Example 2: Display Interface

When it comes to graphical displays, the use of SPI can facilitate the transmission of pixel data. It is important to configure the data rate in a manner that can effectively handle the display's refresh rate and the processing capabilities of the microcontroller. An optimized data rate guarantees seamless and stable display updates.

- *Configuring Data Rate*

Configuring the data rate in SPI is commonly done through software settings in both the master and slave devices. It is important to thoroughly review the datasheets of the connected devices to ensure that the selected data rate is within their specified operational range.

1.4 Modes of SPI

After examining the process of data transmission, our focus now shifts to the SPI protocol and its different modes. The SPI protocol has four modes, each with different combinations of clock polarity (CPOL) and clock phase (CPHA). The different modes of SPI communication offer the necessary flexibility to adapt to different hardware setups and communication needs.

SPI MODE	CPOL	CPHA	Clock Polarity in Idle State	Clock Phase Used to Sample and/or Shift the Data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edge and shifted out on the rising edge
2	1	0	Logic High	Data sampled on the falling edge and shifted out on the rising edge
3	1	1	Logic High	Data sampled on the rising edge and shifted out on the falling edge

Figure 1.4.1 Modes of SPI – Personal Elaboration

- *Mode 0,* also referred to as SPI Mode 0, is characterized by a clock polarity (CPOL) of 0 and a clock phase (CPHA) of 0. During this mode, the clock signal remains low when not in use (CPOL=0), and data is captured on the rising edge of the clock signal's active phase (CPHA=0). Data is captured when the clock signal rises. Mode 0 is a commonly utilized and frequently selected default setting in numerous SPI devices. The approach presented is well-balanced and applicable to various scenarios.

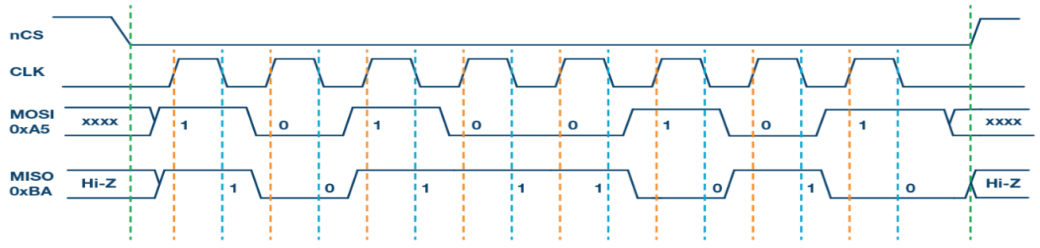


Figure 1.4.2 Mode 0

Source: analog.com

- *Mode 1* or SPI Mode 1 uses a clock polarity (CPOL) of 0 and a clock phase (CPHA) of 1. During this mode, the clock signal stays low when not in use, while data is sampled at the end of the clock signal's active cycle. Data is captured when the clock signal falls. Mode 1 is applicable in situations where devices need data to be sampled on the falling edge to ensure proper synchronization.

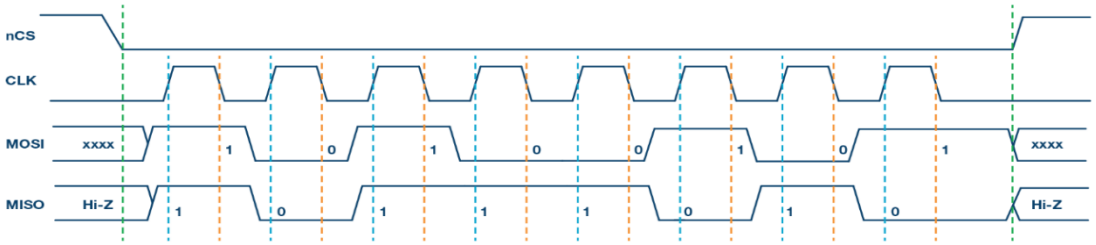


Figure 1.4.3 Mode 1

Source: analog.com

- *Mode 2,* also known as SPI Mode 2, employs a clock polarity (CPOL) of 1 and a clock phase (CPHA) of 0. The clock signal is set to the high state when idle, while data is sampled on the leading edge of the clock signal's active cycle. Data is captured on the falling edge of the clock signal. Mode 2 is not widely utilized, but it holds significance in certain applications where devices necessitate a prolonged idle state for synchronization purposes.

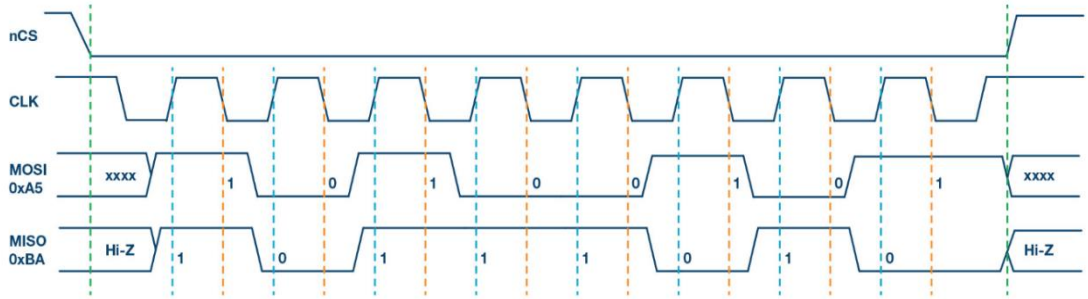


Figure 1.4.4 Mode 2

Source: analog.com

Mode 3, also referred to as SPI Mode 3, utilizes a clock polarity (CPOL) of 1 and a clock phase (CPHA) of 1. During this mode, the clock signal remains high while not in use, and data is sampled when the clock signal's active cycle ends. Data is captured when the clock signal rises. Mode 3 is chosen when devices need data to be sampled on the rising edge to ensure proper synchronization.

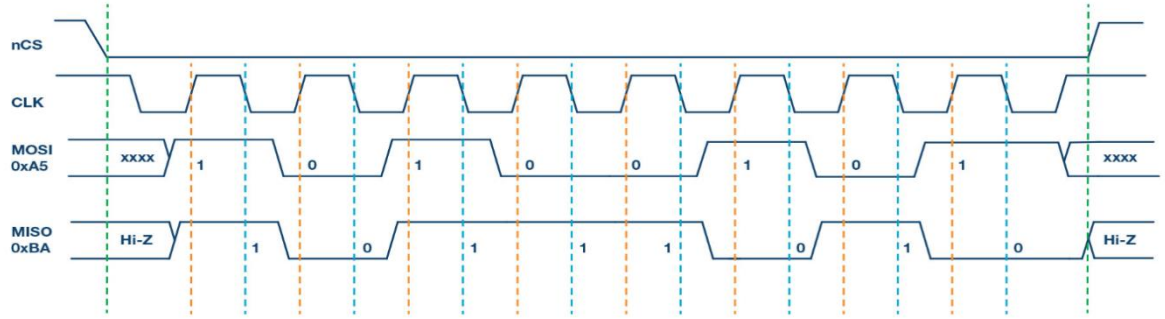


Figure 1.4.4 Mode 3

Source: analog.com

The application and working of SPI modes are determined by the specific requirements of the connected devices and the desired data synchronization. For example, some sensors or memory devices may have precise timing requirements that require a specific mode. Engineers and developers choose the suitable mode by referring to the datasheets and specifications of the devices in their SPI network.

When configuring the SPI mode, it is common for the master device to offer settings for CPOL and CPHA. The settings are transmitted along with other control information during the initialization phase of the SPI communication. The master device ensures that the CPOL and CPHA settings align with the requirements of the connected slave devices.

1.5 Troubleshooting and Debugging Techniques

Once we have covered the fundamentals of SPI, we can delve into more advanced topics like troubleshooting and debugging.

Troubleshooting and debugging are crucial components of the development process, guaranteeing the proper functioning of software and hardware systems. In this section, we will discuss techniques that can be used to effectively identify and resolve issues that may occur during the development and deployment of embedded systems, applications, and electronic devices.

There are several techniques available, which can be listed as follows:

1.5.1 Logging and Debugging Statements

A crucial aspect of troubleshooting involves strategically placing logging and debugging statements within the code. The statements offer valuable insights into the program's execution

flow, variable states, and potential error points. Developers have the ability to track the progress of their program and identify problematic areas by strategically inserting print statements or utilizing dedicated debugging tools.

1.5.2 Interactive Debuggers

Interactive debuggers are highly effective tools that enable developers to navigate code execution, establish breakpoints, examine variable values, and even make code modifications in real-time. These tools offer a dynamic environment that allows for the identification of errors and a comprehensive understanding of program behavior in real-time. Well-known debuggers such as GNU Debugger (GDB) and Visual Studio Debugger provide an extensive array of features to assist in the process of troubleshooting.

1.5.3 Hardware Debugging Tools

Hardware debugging tools are essential in embedded systems development for identifying and resolving hardware-related issues. Engineers can utilize various instruments such as oscilloscopes, logic analyzers, and Joint Test Action Group (JTAG) debuggers to examine signals, monitor bus activity, and conduct thorough analysis of hardware behavior. These tools are essential for diagnosing issues at the electronic component level.

1.5.4 Boundary-Scan Testing

Boundary-scan testing, also referred to as JTAG testing, is a method employed to debug and test intricate digital circuits. This method offers a standardized approach to access and test the connectivity of various on-board components, such as integrated circuits and FPGAs. JTAG allows engineers to conduct comprehensive examinations of digital connections, identify short circuits or open circuits, and validate the integrity of the PCB layout.

1.5.5 Code Profiling

Code profiling entails examining how a program behaves during runtime and how it utilizes resources. Profiling tools offer comprehensive data on the execution time of specific functions or code segments, memory usage, and CPU performance. This method is highly valuable in the identification of performance bottlenecks and the optimization of code for enhanced efficiency.

It is essential for engineers and developers to possess the skills necessary to effectively troubleshoot and debug. Experts have the ability to systematically identify, isolate, and resolve issues in software and hardware systems. They achieve this by utilizing various tools such as

logging, interactive debuggers, hardware testing tools, boundary-scan testing, and code profiling. By implementing these strategies, developers can create solutions that are long-lasting, reliable, and efficient across different technological domains.

1.6 Trade-offs, Application and Future Trends of SPI

The SPI protocol is used for embedded system communication due to its benefits.

A major benefit of SPI is its simplicity. It employs a simple master-slave design with fewer cables than I2C. Simplifying hardware makes it easier to implement in integrated circuits and systems. It also streamlines the design process, leading to more efficient and cost-effective solutions. SPI's data transport mode versatility is another strength. Engineers can tailor clock polarity (CPOL) and phase (CPHA) to connected devices. This versatility provides perfect synchronization, which is essential in timing-critical situations. This flexibility allows SPI to support many devices with different communication demands.

The key is fast data throughput over small distances. SPI is ideal for fast data transfer in close proximity because to its high frequency. SPI is excellent for speed-critical applications like multimedia devices and real-time control systems because to its robustness and reliability. Short cable lengths and simple communication links reduce EMI. The SPI is ideal for applications requiring signal integrity and noise immunity, such as automotive electronics and industrial automation systems. Additionally, SPI is scalable. It can support a variety of slave devices, enabling flexible system architecture. SPI offers adaptability for changing device counts, making it an adaptable choice for many applications. Additionally, SPI is more power-efficient than competing protocols like I2C. Its higher speeds and lack of pull-up resistors make it more energy-efficient in some applications. This is especially important for battery-powered devices and power-constrained applications.

SPI has various drawbacks that may limit its applicability.

One drawback is the absence of established protocols for advanced functions. SPI allows device addressing and data format to be implemented by the user, unlike I2C. Variations in device interpretation and execution of higher-level functions may cause compatibility concerns in multi-vendor setups. Each slave device needs a Chip Select (CS/SS) line, another constraint. This can increase the number of CS/SS lines in systems with many connected devices, complicating hardware design. This presents challenges in applications with limited space or I/O pins. Point-to-point communication is a drawback. SPI is designed for one master device

talking with numerous slaves, unlike I2C. In circumstances with numerous devices initiating communication, SPI may not be the most space-efficient approach. It uses more pins than other protocols, which might be a problem on boards with limited space. Communication protocols may be limited in restricted areas, and SPI may not be ideal for long-distance communication. Over long distances, its short, direct device connections may limit its usefulness. For long-distance communication, RS-485 or Ethernet may be better.

1.6.1 Application of SPI

Due to its speed, adaptability, and reliability, many industries use the SPI protocol. SPI is important in these real-world applications:

- Automotive Sensor Interface

SPI is commonly used to interface automotive sensors and actuators. Accelerometers, pressure sensors, and temperature sensors communicate via SPI to feed vehicle control systems. SPI also controls vehicle actuators, improving safety and performance.

- Flash memory programming

SPI is preferred for flash memory programming and configuration. Flash memory is utilized in microcontrollers, IoT devices, and storage modules. SPI's fast data transport speeds up flash memory programming and retrieval, making electronic gadgets run smoothly.

- Industrial Control Systems

SPI connects microcontrollers to control modules in industrial automation and control systems. Motor controllers, PLCs, and ADCs are examples. SPI's high-speed data transport is essential for industrial real-time control and monitoring.

- Modules for wireless communication

Wireless communication modules like Wi-Fi and Bluetooth transceivers interface with microcontrollers or processors using SPI. Wireless communication may be seamlessly integrated into IoT sensors, smart home devices, and industrial automation systems.

- Consumer electronics

SPI is found in digital cameras, audio devices, and game consoles. Interfaces image sensors, controls audio codecs, and manages input/output devices. The adaptability and speed of SPI improve consumer electronics functionality and performance.

- Motor Control and Driver Circuits

SPI communicates with motor driver circuits in robotics and industrial automation. SPI lets the microcontroller send orders and receive input from motor drivers to precisely regulate motor speed, direction, and torque.

- Integration with ADCs

SPI interfaces with ADCs are prevalent. ADCs transform analog signals from sensors or other sources into microcontroller-processable digital data. High-speed, full-duplex SPI communication transfers digital data from the ADC to the microcontroller efficiently and accurately, enabling precise analog measurements in diverse applications.

- Controlling Peripheral Integrated Circuits

DACs, RTCs, and other peripheral ICs are controlled by SPI. SPI is a stable and efficient communication system for analog signal control and timekeeping. The microcontroller may alter peripheral settings and characteristics as needed.

- Medical Equipment

Patient monitoring, diagnostic, and imaging devices use SPI. These devices' sensors, amplifiers, and data gathering modules connect via SPI to provide accurate medical diagnosis and treatment data.

1.6.2 Future Trends and Developments

After analyzing the tradeoffs, we can imagine its future use. Staying ahead of technology requires anticipating future trends. Technology trends that will shape the future are examined in this section. The trends mentioned cover various domains, including artificial intelligence, quantum computing, sustainable technologies, and biotechnology.AI and ML

AI and ML will transform several sectors. Advanced AI-driven applications enable natural language processing, computer vision, and autonomous decision-making. Deep learning algorithms are advancing image recognition, driverless vehicles, and predictive analytics.

- Quantum computing

Quantum computing revolutionizes computation. Quantum computers may tackle complicated problems that classical computers cannot using quantum mechanics. Quantum systems' exponential processing capability will aid encryption, drug discovery, optimization, and material science.

- Renewable Energy and Sustainable Technologies

Sustainability drives renewable energy technology advancement. Better solar, wind, energy storage, and grid management are making renewable energy cheaper and more efficient. Additionally, materials science and energy-efficient technology advances are making the future more sustainable.

- Genomics and Biotechnology

Biotechnology advances, affecting healthcare, agriculture, and the environment. Genomic advances, CRISPR gene editing, and tailored treatment are changing healthcare. Biotechnology also helps fight climate change and produce sustainable agriculture.

- IoT and Edge Computing Communities

Edge computing brings computational resources closer to data generation, complementing cloud computing. Smart cities, driverless vehicles, and industrial automation require real-time processing, hence this trend is vital. The rise of IoT devices and edge computing are transforming connected ecosystems.

AI, quantum computing, sustainable solutions, and biotechnology innovations promise a bright future. Professionals and organizations that want to harness these trends to solve tomorrow's problems must stay current. Adopting these advances leads to a more technologically advanced and sustainable future.

Chapter II: FIELD-PROGRAMMABLE GATE ARRAY(FPGA)

2.1 Introduction to FPGAs

Now that we have a grasp on utilizing the SPI protocol and other related subjects, let's delve into this chapter's exploration of FPGA advancements and their potential application in our paper for interfacing with this protocol. FPGAs are programmable semiconductor devices that provide a versatile and adaptable platform for digital circuit design and implementation. FPGAs, in contrast to ASICs, offer the flexibility of being programmable and configurable by users post-manufacturing. This allows them to perform a diverse array of digital functions.

FPGAs are composed of an array of Configurable Logic Blocks (CLBs), programmable interconnects, and embedded resources like memory blocks and Digital Signal Processing (DSP) units. FPGAs offer designers the ability to define the functionality and interconnectivity of logic gates, allowing for the implementation of intricate digital systems.

2.1.1 Definition and Purpose

- *What is the FPGA?*

FPGAs are semiconductor devices that provide a versatile platform for designing and implementing digital circuits. The components of these systems include configurable logic blocks (CLBs), programmable interconnects, and integrated resources such as memory blocks and digital signal processing units. FPGAs have the capability to be programmed and configured by users post-manufacturing, enabling them to execute a diverse array of digital functions.

- *Why we use?*

FPGAs are a versatile solution for applications that require rapid prototyping, low-volume production, or flexibility in design iterations. These devices are utilized in a range of industries, such as telecommunications, aerospace, industrial automation, and automotive electronics. They offer a harmonious blend of performance, power efficiency, and time-to-market. The purpose can be further explained in various important aspects:

1. *Rapid Prototyping and Development*

FPGAs allow engineers and designers to efficiently prototype digital circuits and systems. The ability to rapidly prototype is extremely valuable in industries where speed is crucial for getting

products to market. It enables designers to iterate and test their designs without having to produce custom hardware.

2. Low-Volume Production

FPGAs offer a cost-effective solution for applications with lower production volumes or where custom ASICs may not be economically viable. They eliminate the need for costly mask sets and decrease initial production expenses.

3. Flexibility and Adaptability

FPGAs have the capability to be reprogrammed and reconfigured to carry out a variety of tasks. This level of flexibility enables design modifications and updates to be made even after the hardware has been produced, allowing for adaptability to changing project needs.

4. Parallel Processing

FPGAs are highly suitable for tasks that can be effectively parallelized. Executing multiple operations simultaneously can result in notable performance enhancements in various applications, such as digital signal processing, image processing, and cryptography.

5. Low Power Consumption.

Some FPGA families, like the Cyclone 10 LP series, are specifically engineered to minimize power consumption. These devices are well-suited for battery-powered applications and situations where power efficiency is of utmost importance.

6. Education and Research

FPGAs have found extensive application in educational institutions and research environments for the purpose of imparting knowledge on digital design principles and investigating complex digital systems. They offer a practical platform for students and researchers to explore intricate digital circuits.

2.1.2 Historical Background

After comprehending the FPGA and its importance, we can explore its historical origins and background. FPGAs have their origins in the late 1970s, with the emergence of Programmable Logic Devices (PLDs). Early programmable logic devices (PLDs) were basic in nature, enabling only partial reprogramming of logic circuits. This provided a certain degree of flexibility that was absent in conventional fixed-function integrated circuits (ICs).

In response to the increasing demand for programmable devices with greater versatility, CPLDs were introduced during the 1980s. CPLDs combine multiple PLDs into a single chip, providing increased logic capacity and enhanced programmability. This advancement established the groundwork for more intricate and robust programmable logic solutions.

The emergence of FPGA occurred in the mid-1980s. An important innovation was the implementation of a highly adaptable architecture, which offered greater flexibility in comparison to CPLDs. This milestone represented a notable progress in programmable logic technology, facilitating the execution of increasingly intricate digital designs.

Throughout time, there have been ongoing advancements in FPGA architectures. The progress in semiconductor technology has resulted in the creation of FPGAs that possess greater logic capacity, faster clock speeds, and supplementary embedded resources like memory blocks, digital signal processing units, and specialized I/O interfaces.

Numerous companies have been instrumental in the development of FPGAs. Xilinx, established in 1984, is widely recognized for pioneering the initial commercially accessible FPGA. Altera, which is now a part of Intel, was established in 1983 and played a significant role in the advancement of FPGA technology. These companies, in addition to others, have consistently expanded the limits of FPGA capabilities and have made substantial contributions to the extensive utilization of FPGAs in diverse industries.

2.2 FPGA Architecture

2.2.1 Introduction

Now, we will delve into the FPGA architecture and its essential components.

FPGAs are a distinct type of semiconductor devices that provide the ability to reconfigure logic, enabling the implementation of versatile digital circuits. Having a solid grasp of FPGA architecture is essential for maximizing design efficiency and unlocking their complete capabilities. In this chapter, we explore the intricate aspects of FPGA architecture, including CLBs, interconnect networks, embedded resources, and specialized elements.

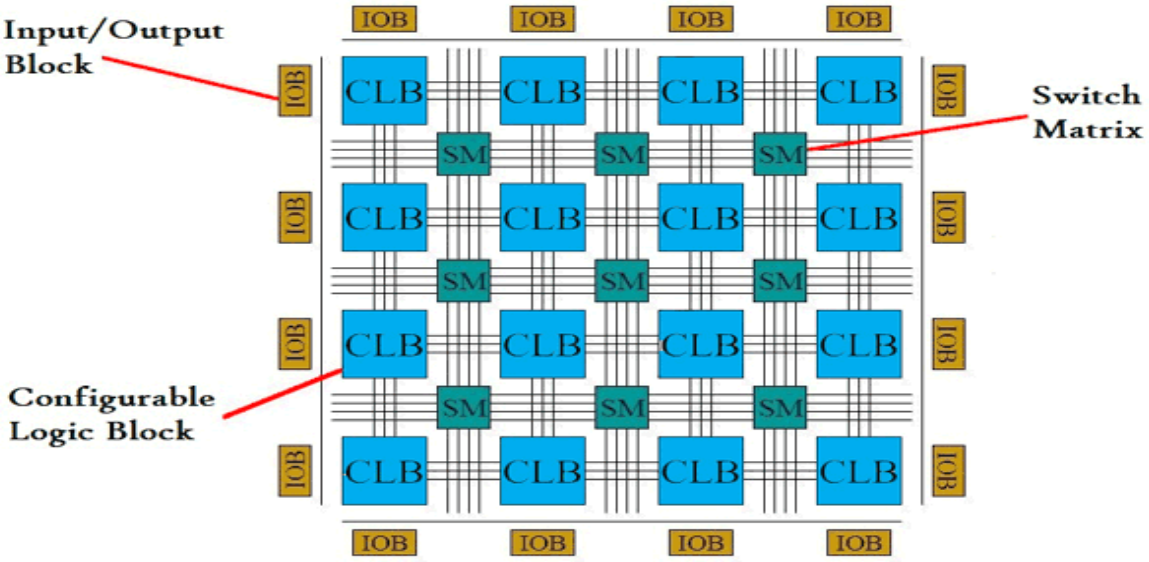


Figure 2.2.1.1 FPGA Architecture

Source: circuitdigest.com

Let's now discuss each component utilized in FPGA architecture individually.

2.2.2 Configurable Logic Blocks (CLBs)

CLBs are essential components that form the basis of an FPGA. Their role involves the implementation of combinational and sequential logic functions. A typical CLB is composed of Look-Up Tables (LUTs), Flip-Flops (FFs), multiplexers, and other programmable elements. LUTs are essential components in FPGA logic implementation as they enable the implementation of versatile Boolean functions.

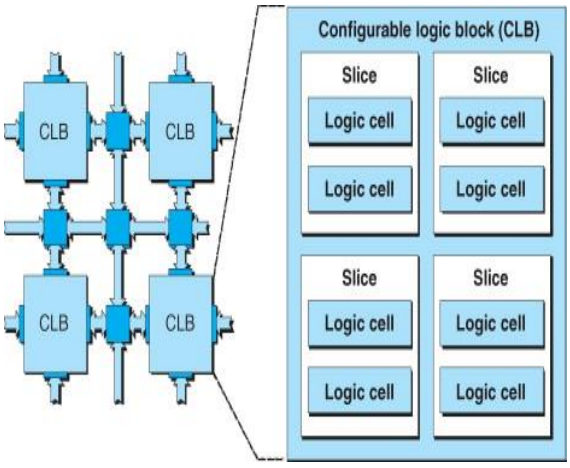


Figure 2.2.2.2 CLB Architecture

Source: sciencedirect.com

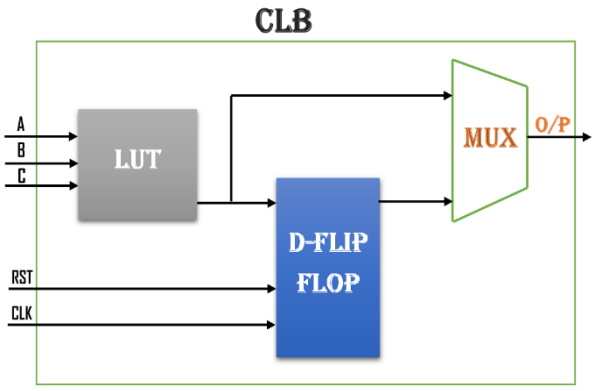


Figure 2.2.2.3 CLB Component – Personal elaboration

- *Look-Up Tables (LUTs)*

A Look-Up Table is an essential element of CLBs, responsible for storing and executing Boolean functions. The function of this unit is to serve as a compact and adaptable memory module, where input combinations are associated with specific output values. Designers can implement a variety of logic functions by programming the LUT. As an illustration, a 4-input LUT has the capability to represent any Boolean function of four variables.

LUTs play a vital role in the implementation of FPGA logic, allowing for the realization of various digital functions in a flexible and programmable manner.

- *Flip-Flops (FFs)*

Flip-Flops offer sequential logic functionality within Configurable Logic Blocks (CLBs). These mechanisms enable the retention and transmission of state information over multiple clock cycles. This is crucial for applications that necessitate memory elements or synchronization of signals. FFs are essential components in digital circuits as they store a single bit of information, ensuring the circuit's state is maintained.

Finite state machines are crucial for incorporating sequential logic functions like registers and memory elements in FPGA designs.

- *Multiplexers and Carry Chains*

Further enhancements to the flexibility of CLBs are achieved through the inclusion of additional elements such as multiplexers and carry chains. Multiplexers allow for the selection of various inputs to perform intricate logic operations. Chains of carry signals are utilized to improve the efficiency of arithmetic operations, thereby enhancing the FPGA's capabilities in tasks such as addition and multiplication. Optimal utilization of multiplexers and carry chains is crucial for attaining superior performance in FPGA designs, particularly in scenarios that involve arithmetic operations.

2.2.3 Interconnect Networks

Interconnect networks serve as the communication backbone of an FPGA, facilitating the flow of signals between CLBs and other resources. The system is composed of a matrix of programmable routing resources and switch matrices. Having a solid grasp of the interconnect fabric is essential for maximizing the efficiency of FPGA designs.

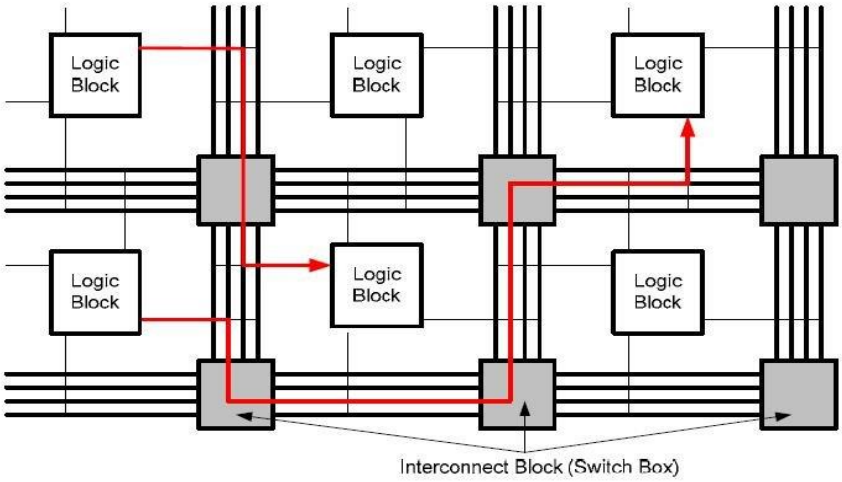


Figure 2.2.3.1 Interconnect and their Internal Structure

Source: researchgate.net

Now, let's delve into a more comprehensive analysis of these two elements.

- *Programmable Routing Resources*

Programmable routing resources are made up of wires and switch points that can be configured. These resources enable designers to establish the routes that signals follow while passing through the FPGA. Efficient use of these resources is crucial for reducing signal delays and ensuring optimal functionality. Optimal routing is essential for achieving top-notch FPGA designs, necessitating meticulous evaluation of the available routing resources.

- *Switch Matrices*

Switch matrices facilitate the interconnection of various wires through cross-points. These components serve as adjustable switches that allow designers to create connections between different logic elements. Efficient utilization of switch matrices is crucial for achieving optimal performance in FPGA designs. Switch matrices are integral to the connectivity and performance of an FPGA design. Configuring them correctly is vital for achieving the desired functionality.

2.2.4 Embedded Resources

Contemporary FPGAs frequently include dedicated resources that augment their capabilities for particular applications. The embedded resources refer to dedicated hardware components that are seamlessly integrated into the FPGA chip, offering enhanced functionality beyond the fundamental logic capabilities. Further details can be observed regarding its utilization as embedded resources.

➢ *Digital Signal Processing (DSP) Blocks*

DSP Blocks are hardware units found in an FPGA that are specifically designed to enhance the performance of digital signal processing tasks. These processors are designed to excel at tasks such as filtering, convolution, and Fast Fourier Transforms (FFTs). DSP blocks generally include Multiply-Accumulate (MAC) units, adders, and accumulators. Through the utilization of dedicated DSP blocks, FPGAs can attain enhanced performance and efficiency in signal processing applications by delegating computationally intensive tasks.

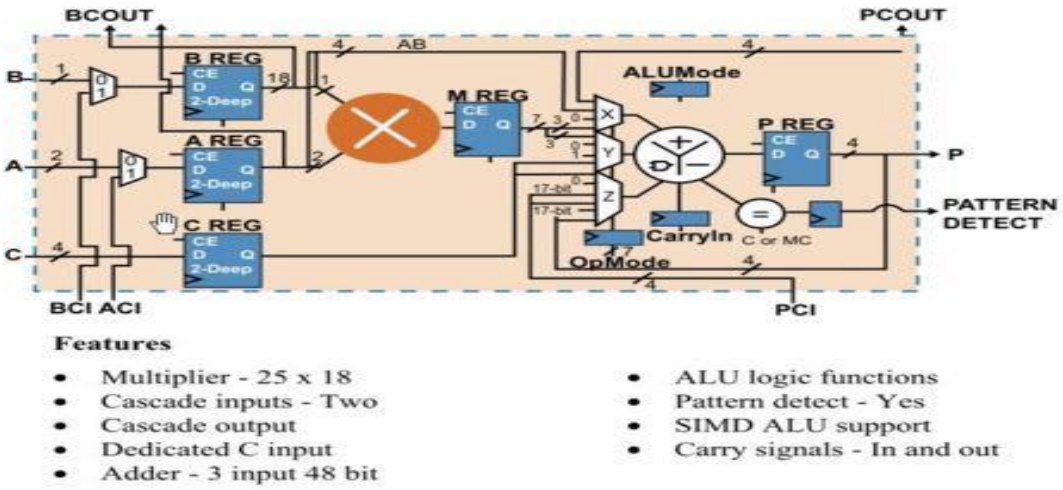


Figure 2.2.4.1 DSP Block

Source: media.tumblr.com

DSP blocks play a crucial role in various applications, including wireless communications, image processing, audio processing, and radar systems. These applications heavily rely on real-time processing of analog signals.

➢ *Block Random Access Memory (Block RAM)*

Block RAM modules are memory resources that are specifically designed to be integrated within an FPGA. Block RAM is situated on the FPGA chip, offering swift and effective data storage, in contrast to external memory. The system is structured as a customizable collection of memory blocks that serve the purpose of storing data or functioning as First-In-First-Out (FIFO) buffers. Block RAM is highly beneficial in applications that necessitate extensive data storage or rapid data access, such as data caching, buffering, and lookup tables. Efficient utilization of block RAM can help designers minimize the reliance on external memory components, resulting in FPGA designs that are more compact and cost-effective.

➢ *Peripheral Component Interconnect Express (PCIe)*

PCIe is a widely adopted standard for high-speed serial communication, facilitating the

connection of different components in computer systems. Certain FPGAs feature dedicated PCIe interfaces for seamless communication with various devices and systems, including CPUs, GPUs, and storage devices. These interfaces are crucial for applications that necessitate fast information exchange due to their high-bandwidth data transfer capabilities. PCIe interfaces allow FPGAs to serve as efficient data processing units in various applications, such as data centers, high-performance computing, and networking equipment.

2.2.5 Specialized Elements

FPGAs can include specialized elements designed for specific tasks, in addition to the core components such as CLBs, interconnect networks, and embedded resources. FPGAs offer a wide range of functionality and customization options, enabling them to thrive in various applications.

- *High-Speed Transceivers*

High-speed transceivers are specialized hardware components found in an FPGA that are specifically engineered for serial communication. These devices allow for the transmission and reception of data through fast serial interfaces, facilitating communication with external devices or other systems. Transceivers are commonly designed to support various communication standards, including PCIe, Serial Advanced Technology Attachment (SATA), and high-speed serial protocols like Gigabit Ethernet or USB. Fast transceivers play a vital role in applications that demand quick data transfer, like high-speed networking, data center operations, and high-performance computing systems.

- *Clock Management Resources*

Clock management resources refer to dedicated circuits within an FPGA that facilitate accurate control and distribution of clock signals. These resources comprise Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs). They enable designers to generate stable clock frequencies, align various clock domains, and adjust clock phases to fulfill specific timing requirements. Efficient utilization of clock management resources is crucial for achieving accurate signal synchronization and meeting timing requirements in FPGA designs.

- *Analog/Mixed-Signal Elements*

FPGAs often incorporate dedicated analog/mixed-signal components for seamless interaction with the physical environment. These elements may include analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). ADCs convert continuous analog signals

into discrete digital values, whereas DACs carry out the opposite process. FPGAs can interface with sensors, actuators, and other analog devices by incorporating analog/mixed-signal elements. This expansion of their application scope allows them to perform tasks such as data acquisition, control systems, and sensor interfacing.

- *Power Management Circuits*

Power management circuits are components specifically designed for optimizing power consumption in an FPGA. These features are implemented to effectively manage and reduce power consumption in the FPGA, taking into account its operational requirements. Effective power management is essential for applications that prioritize power consumption, such as battery-powered devices and energy-efficient systems.

2.3 FPGA Design Flow

2.3.1 Introduction

Upon analyzing different components within FPGA architecture, it becomes evident how they operate within the FPGA design pipeline.

FPGAs are a type of semiconductor device that provide reconfigurable logic, allowing for a variety of digital circuit implementations. The creation of functional circuits on FPGAs follows a structured series of steps referred to as the FPGA design flow. This meticulously designed sequence guides engineers and designers from initial concept to the final deployment of a digital circuit on the FPGA platform.

The FPGA design flow encapsulates the entire development process, ensuring that designers can effectively harness the capabilities of FPGAs for a diverse array of applications. The process includes various stages such as design entry, synthesis, implementation, verification, and configuration. Every phase plays a crucial role in the process, starting from capturing the desired functionality to optimizing logic, meeting timing constraints, and finally programming the FPGA.

Through a comprehensive grasp of the FPGA design flow, designers can effectively navigate the intricacies of FPGA development, resulting in streamlined, dependable, and finely-tuned digital circuits that fulfill precise application demands. This chapter offers a comprehensive examination of the FPGA design flow, providing valuable insights into the methodologies, considerations, and tools utilized at each stage.

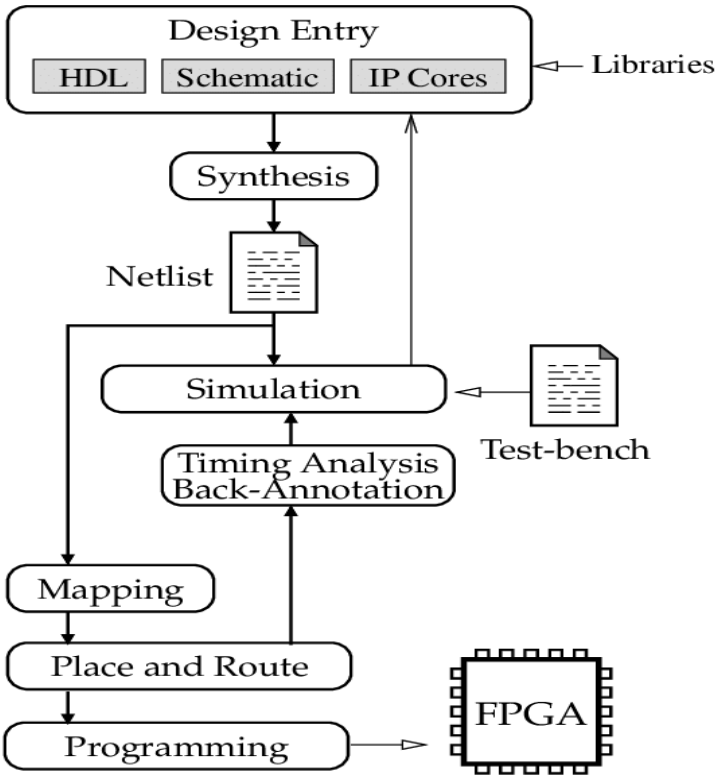


Figure 2.3.1.1 FPGA Design Flow

Source: www.researchgate.net

Let's carefully examine each point to ensure a thorough understanding.

2.3.2 Design Entry

- *High-Level Abstraction Languages*

The design entry process starts with choosing a High-Level Abstraction Language (HDL). VHDL and Verilog are commonly utilized languages for describing the functionality of digital circuits. These languages offer a more advanced representation, similar to software programming, which facilitates the understanding and modelling of intricate systems. In this paper, I will focus solely on VHDL as the selected HDL. In the upcoming chapter, I will thoroughly examine its features and discuss its applications in FPGA design.

- *Hardware/Software Co-Design*

Hardware/software co-design requires the system to be divided into hardware modules, which are implemented on the FPGA, and software modules, which are executed on a processor. The strategic allocation of tasks enables enhanced performance and efficiency. It is important to establish clear interfaces to facilitate smooth communication between the FPGA and processor, allowing for synchronized operation and data exchange.

A comprehensive grasp of FPGA hardware architecture and software environments is essential

for this approach. Important factors to consider are memory management, I/O handling, and system-level synchronization. Thorough testing, which includes co-simulation, is used to validate the interaction between hardware and software components. This leads to a system that combines the strengths of both domains in a synergistic manner.

- *Intellectual Property (IP) Integration*

The integration of Intellectual Property (IP) in FPGA design is a meticulous process that entails the inclusion of pre-designed and verified functional modules into a larger digital system. The modules can vary in complexity, ranging from basic components to more intricate units such as processors and communication interfaces. They serve to encapsulate specific functionalities. The utilization of IP integration in FPGA design offers significant benefits as it expedites development and guarantees reliability.

IP integration is crucial and has significant implications in various domains. Firstly, it promotes time efficiency by reducing design time, enabling designers to prioritize higher-level decisions. In addition, the utilization of pre-verified IP blocks greatly decreases the chances of functional errors, thereby improving the system's reliability. In addition, the integration of IP utilizes the specialized knowledge contained within the IP blocks, maximizing the utilization of expertise in specific domains.

It is crucial to bear in mind certain factors when integrating IP for optimal effectiveness. Ensuring interface compatibility is crucial to align the IP with the system's communication protocols. Certain IP blocks provide the ability to customize and make parameter adjustments in order to meet the specific requirements of a project. Furthermore, it is of utmost importance to adhere to licensing agreements when utilizing IP blocks, as this entails honouring any limitations on IP usage.

IP integration is widely used in various fields. In communication interfaces, the integration of standard protocols such as UART, SPI, or I2C enables seamless interaction with external devices. Ready-made blocks for mathematical functions, like multiplication or Fourier transforms, are highly advantageous in signal processing applications. In addition, it is a widely adopted approach to integrate processor IP cores into the system. These cores efficiently handle sequential tasks, enabling the FPGA to dedicate its resources to parallel operations.

2.3.3 Design Synthesis

- *Logic Synthesis*

Logic synthesis is a crucial step in the FPGA design process, where the high-level hardware description, written in languages such as VHDL or Verilog, is converted into a gate-level netlist. The netlist comprises logic gates, including AND, OR, and NOT gates, as well as flip-flops, which accurately depict the intended functionality of the digital circuit.

During logic synthesis, the toolchain analyses the high-level description and performs optimizations to achieve objectives such as minimizing area utilization, reducing power consumption, and optimizing for performance. Multiple algorithms and techniques are utilized to transform and map the high-level constructs into a streamlined gate-level representation.

In addition, logic synthesis includes technology mapping, where gates from a library that matches the target FPGA technology are chosen to implement the logic. Ensuring compatibility with the target FPGA's architecture enhances the overall efficiency of the design.

The output of the logic synthesis process forms the basis for subsequent stages such as technology mapping, placement, and routing. The final quality and performance of the implemented FPGA design are greatly affected by it.

- *Technology Mapping*

Technology mapping is an essential stage in logic synthesis, involving the selection of specific components from a library to implement the synthesized logic on an FPGA. This process guarantees that the chosen components are in line with the architecture of the target FPGA. Through careful decision-making, designers can maximize resource utilization and improve the overall efficiency of the design. Effective technology mapping is crucial for attaining design goals pertaining to performance, area, and power consumption. The role it plays in determining the final quality and performance of the implemented FPGA design is crucial.

- *Timing Analysis*

Timing analysis is a crucial step in logic synthesis, as it involves assessing the timing properties of the synthesized design. The analysis focuses on critical paths, which are the longest delay paths through the combinational logic. The main objective is to ensure that signals reach their intended destinations within the specified clock cycles, without any violations of setup and hold time constraints. Timing analysis considers multiple factors, such as signal propagation delays, clock-to-q delays, and data arrival times. This analysis offers valuable insights into the

design's capacity to achieve desired clock frequencies while maintaining compliance with timing constraints. By employing sophisticated methods such as static timing analysis, designers can thoroughly evaluate and optimize the timing characteristics of the design to achieve peak performance.

2.3.4 Design Implementation

- *Place and Route (P&R)*

The Place and Route (P&R) phase is a crucial step in the FPGA design process that comes after logic synthesis. In this stage, the logic is mapped to specific locations on the FPGA chip and the necessary connections between the logic elements are established.

During the "place" step, the design tool arranges the synthesized logic components onto the physical grid of the FPGA. The task at hand is to identify the most suitable position for each component, with the aim of reducing delays, enhancing performance, and ensuring compliance with design limitations. Various factors, such as the proximity to input/output pads, clock resources, and power distribution networks, are carefully considered.

After the components have been placed, the next step is to establish the interconnections between them. The tool calculates optimal signal paths between logic elements to ensure that critical paths meet timing requirements. This phase is crucial to ensure the optimal functionality and performance of the FPGA design.

Accurate placement and routing play a vital role in maximizing performance and resource utilization in FPGA designs. State-of-the-art algorithms and techniques are utilized to address the challenge of balancing conflicting objectives, such as minimizing wirelength, optimizing for speed, and meeting timing constraints.

- *Clock Tree Synthesis in FPGA Design*

Clock Tree Synthesis (CTS) is an essential stage in the FPGA design process, which involves the creation of an optimized hierarchical network for distributing clock signals across the chip. The objective of CTS is to guarantee the simultaneous arrival of clock edges at all sequential elements, thereby minimizing clock skew and ensuring accurate synchronization.

The CTS process involves analyzing the clock distribution network and strategically positioning buffers or inverters to ensure balanced delay of the clock signals. This improves the synchronization of clock edges across different areas of the chip, which enhances the reliability and performance of the design. In addition, CTS takes into account various factors

such as clock insertion delay, skew budget, and power consumption.

Effective clock tree synthesis is essential for ensuring synchronous operation in intricate digital systems. It is crucial in preventing timing violations and ensuring that the design meets its specified timing constraints. Advanced CTS algorithms utilize advanced optimization techniques to achieve optimal clock distribution.

- *Power Analysis and Optimization in FPGA Design*

Efficient power analysis and optimization play a crucial role in FPGA design, with the goal of effectively managing and minimizing power consumption in digital circuits. FPGA devices frequently function in environments with limited power resources, making power efficiency a crucial consideration.

Power analysis entails assessing the dynamic and static power consumption of the FPGA design. The generation of dynamic power is linked to the switching activity of transistors, whereas static power is a result of leakage currents. Power analysis tools and methodologies assist designers in pinpointing the key contributors to power consumption within a design.

Power consumption is reduced through the application of optimization techniques. This could entail making architectural modifications, like reconfiguring logic elements, or taking advantage of power-saving features provided by the FPGA platform. In addition, designers have the option to implement clock gating, voltage scaling, and other power reduction strategies to further improve efficiency.

Efficient power analysis and optimization have the potential to significantly increase battery life, lower operating costs, and promote environmentally sustainable designs.

2.3.5 Verification and Testing

- *Functional Verification in FPGA Design*

Functional verification is an essential step in the FPGA design process, ensuring the accuracy of the implemented logic in relation to the original design specification. The process requires thorough testing and validation to ensure that the FPGA design operates as intended in different operating conditions and scenarios.

Verification methodologies include various techniques such as simulation, formal verification, and hardware emulation. Simulation entails executing the design within a software environment to observe its behaviour and validate its functionality. Formal verification utilizes mathematical methods to establish the accuracy of the design according to formal

specifications. Hardware emulation utilizes dedicated hardware platforms to execute the design at or close to real-time speeds, enabling comprehensive testing.

Verification suites and testbenches are created to evaluate the design's behaviour in relation to specific inputs, boundary conditions, and corner cases. Thorough test coverage is crucial in order to minimize the potential for undetected bugs.

Effective functional verification is crucial in ensuring a strong level of trust in the dependability and accuracy of the FPGA design, particularly in safety-critical applications.

- *Timing Verification in FPGA Design*

Timing verification is an essential step in the FPGA design process, which aims to ensure that the design adheres to specific timing constraints. The process entails evaluating if signals reach their intended destinations within the specified clock cycles, thereby avoiding any breaches of setup and hold time requirements.

Static Timing Analysis (STA) techniques are used in tools and methodologies for timing verification. The delays of signals through the different logic paths and the clock distribution network are analysed by STA. The analysis takes into account various factors, including gate delays, interconnect delays, and clock skew. The objective is to detect and correct any routes that fail to satisfy the designated timing constraints.

Timing verification is crucial for designs that involve high-speed or time-critical components. Failure to meet timing constraints can result in functional errors or decreased performance.

- *Hardware Testing in FPGA Design*

Hardware testing is an essential step in the FPGA design process, where the physical implementation of the design is thoroughly validated and verified. The primary objective is to guarantee the proper and dependable operation of the FPGA hardware across different conditions and inputs.

Testing methodologies encompass pre-silicon and post-silicon testing. Prior to manufacturing the physical hardware, pre-silicon testing entails the simulation of the design in a software environment. Designers can detect and resolve potential issues at an early stage in the development process. Post-silicon testing, however, entails the validation of the physical FPGA following its manufacturing process. Various techniques are used to evaluate the functionality of the fabricated hardware, including boundary scan testing, Built-In Self-Test (BIST), and functional testing.

Effective hardware testing is essential for identifying and correcting any manufacturing defects or design errors, ensuring that the final FPGA hardware meets the desired specifications and performance criteria.

2.3.6 Configuration and Deployment

- *Bitstream Generation in FPGA Design*

The generation of the bitstream is a crucial stage in the FPGA design process, as it involves the creation of the final configuration file. The bitstream in question is responsible for configuring the FPGA by providing the necessary binary information. It outlines the programming of logic elements, interconnects, and other resources.

During the process of bitstream generation, the synthesis and place-and-route results are converted into a format that is compatible with the target FPGA device. The process entails transforming logical descriptions into physical configurations that align with specific locations on the FPGA chip. The bitstream is usually created in a format that aligns with the programming tools offered by the FPGA manufacturer.

After generating the bitstream, it can be loaded onto the FPGA device to configure it according to the desired functionality. This process is crucial in allowing the FPGA to carry out its designated functions, whether it is used independently or as a component of a larger electronic system.

- *In-System Programming in FPGA Design*

In-System Programming (ISP) is an essential aspect of FPGA design, enabling the reconfiguration of the FPGA device post-deployment in a system. This feature allows designers to easily modify the functionality of the FPGA without the need for physical chip removal or replacement.

ISP is highly beneficial in situations where system requirements may vary, or firmware updates are required. It offers a way to modify the behavior of the FPGA without requiring any hardware changes. In addition, ISP plays a crucial role in situations where prototypes are being refined, as it facilitates iterative development and testing.

There are different methods available for conducting In-System Programming. One of these methods is through JTAG interfaces, which offer a standardized way to access and configure programmable devices. In addition, numerous FPGA development environments offer specialized tools and utilities for conducting ISP operations.

The FPGA design flow encompasses various crucial processes, ranging from high-level specification and simulation to synthesis, technology mapping, and timing verification. The process ends with the creation of a bitstream, which is used to configure the FPGA for deployment. In the upcoming chapter, we will provide a comprehensive examination of the Cyclone 10 LP FPGA board, delving into its features, applications, and advantages. This board offers a wide range of options for various electronic systems and applications, making it highly versatile and efficient.

2.4 Intel Cyclone 10 Low Power (LP) FPGA Borad

So now that we know how the FPGA works, we can consider how it will work in the actual world via the real board. For this purpose, we may utilize the Intel cyclone board to understand how the board will behave in the real world.

2.4.1 Introduction

FPGAs have become increasingly popular in recent years because of their reconfigurable nature, which makes them well-suited for a variety of applications. They are particularly valuable in applications that require quick development and customization.

The Intel Cyclone 10 LP 10CL025YU256I7G FPGA board is a versatile and cost-effective field-programmable gate array (FPGA) platform developed by Intel Corporation. This device belongs to the Cyclone 10 LP family, which is renowned for its efficient power usage and versatility across various applications. FPGAs are semiconductor devices that can be configured and reconfigured by designers after manufacturing. This flexibility enables the implementation of digital logic circuits that are customized to meet specific requirements.

2.4.2 Cyclone 10 LP

The term "Cyclone 10 LP FPGA" is used to describe a particular group of FPGAs that have been developed by Intel Corporation. The "Cyclone" series is renowned for its ability to provide a well-rounded solution that is both cost-effective, energy-efficient, and high-performing, making it a versatile choice for various applications.

The numerical designation in Cyclone 10 LP denotes the specific series or generation, while the acronym "LP" signifies "Low Power," highlighting the notable energy-efficient attributes of this particular family. The FPGAs are specifically engineered to cater to the power efficiency requirements of applications like Internet of Things (IoT) devices, portable electronics, and other power-sensitive applications.

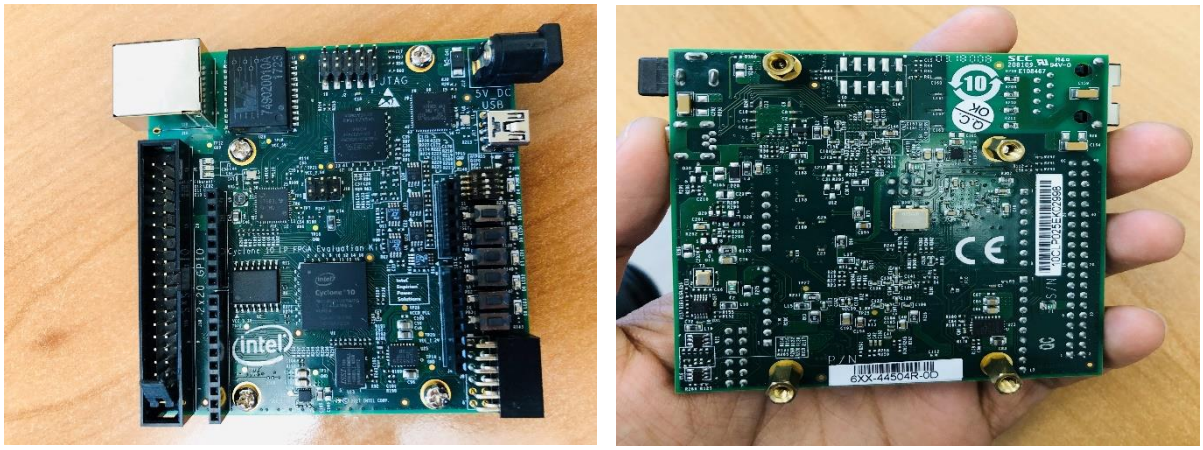


Figure 2.4.2.1 Cyclone 10LP(10CL025YU256I7G) FPGA

Principal Characteristics of the Cyclone 10 LP FPGAs

1. FPGA Core: At the core of the board lies the FPGA, a programmable chip comprising an array of Configurable Logic Blocks (CLBs), interconnections, and various programmable elements. For the Cyclone 10 LP model 10CL025YU256I7G, it's distinguished by its logic capacity, architecture, and performance characteristics.
2. Logic Elements: The FPGA's basic functional units are its logic elements (LEs), totaling 25,270 in the Cyclone 10 LP. These LEs are adaptable and can be programmed to execute a variety of digital logic operations, allowing for the creation of diverse digital circuits.
3. On-Board Memory: Included in the FPGA is 414 Kbits of embedded memory, useful for data storage or holding configuration details within the FPGA. This internal memory aids in efficient information management, reducing dependence on external memory.
4. User I/O Pin Capacity: The Cyclone 10 LP 10CL025YU256I7G offers up to 202 user I/O pins, providing extensive connectivity options for linking the FPGA with external gadgets, sensors, or additional components.

- DSP Blocks: The board is outfitted with 36 Digital Signal Processing (DSP) blocks, tailored for executing mathematical functions often utilized in signal processing tasks. These blocks enhance the efficiency of operations like filtering and modulation.
- Phase-Locked Loops: The inclusion of two PLLs in the Cyclone 10 LP 10CL025YU256I7G is vital for clock management. PLLs generate stable, accurate clock signals, essential for the synchronized functioning of digital circuits.
- Energy-Efficient Operation: The FPGA's design focuses on low power consumption, an

important aspect for applications where energy efficiency is paramount, such as in battery-operated devices or systems with stringent power limitations.

- Configuration Memory: The board boasts 1 Mbit of dedicated memory for storing the configuration bitstream, which determines the FPGA's functionality. This memory capacity allows for a wide array of configurations to be held and utilized as needed.
- User Flash Memory: With 4 Mbit of user flash memory, the board can store additional data, configuration files, or other essential operational information.
- Voltage Regulation: Integral to the board are voltage regulators, ensuring that stable and regulated voltages are consistently delivered to different parts of the FPGA. This stability is key to the FPGA's reliable performance and the functionality of its connected components.

2.4.3 Architecture

Once we're familiar with the cyclone FPGA board, the next step is to research its design and potential applications in our project. The Intel Cyclone 10 LP 10CL025YU256I7G FPGA is structured hierarchically, with different configurable elements and resources. This architecture enables designers to efficiently implement intricate digital circuits by configuring these elements to carry out precise tasks.

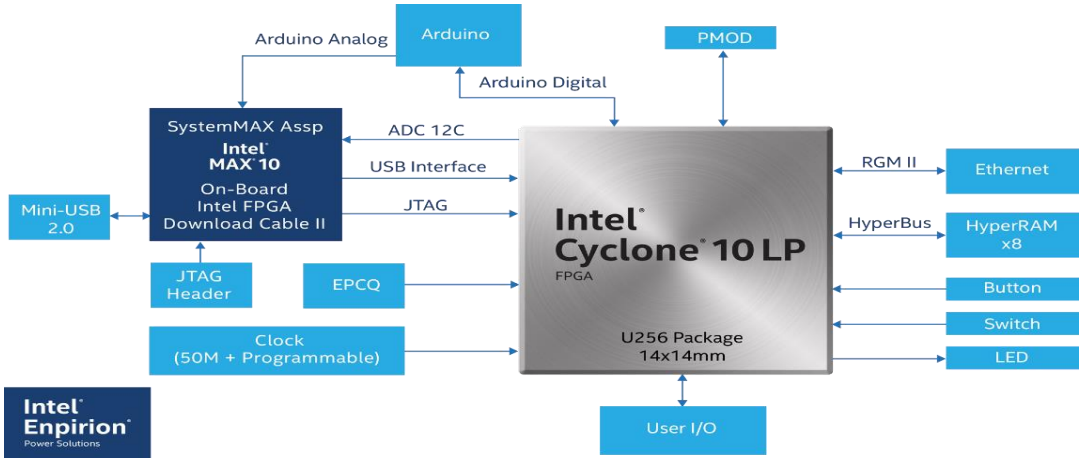


Figure 2.4.3.1. INTEL Cyclone 10LP Architecture

Source: www.intel.com

Let's examine each of the components individually.

1. Configurable Logic Blocks (CLBs)

The Cyclone 10 LP FPGA is centered around Configurable Logic Blocks (CLBs). The blocks in question serve as the fundamental building units of the FPGA, carrying out the necessary

logic operations. The CLB is composed of various components such as look-up tables (LUTs), multiplexers, and flip-flops. These components can be configured to execute specific logic functions.

2. Memory Elements

The FPGA includes memory elements necessary for storing intermediate values and results during the execution of digital logic operations. Memory elements are crucial in applications that necessitate temporary data storage.

3. Digital Signal Processing (DSP) Blocks

DSP Blocks are dedicated resources designed to efficiently execute mathematical operations frequently utilized in signal processing applications. These components consist of arithmetic logic units (ALUs), multipliers, and accumulators. They enable the efficient processing of digital signals in various applications, including filtering and modulation.

4. Routing Resources

The FPGA architecture features a flexible routing fabric that facilitates the exchange of data among various configurable elements. This routing fabric offers the required flexibility for designers to construct intricate digital circuits.

5. Phase-Locked Loops (PLLs)

The Cyclone 10 LP FPGA includes Phase-Locked Loops (PLLs), which play a crucial role in managing the clock signals within the FPGA. PLLs enable the generation of accurate and stable clock signals, ensuring the synchronous operation of digital circuits.

6. I/O Elements

The architecture incorporates Input/Output (I/O) components that enable communication between the FPGA and external devices. The elements in question facilitate the connection between the FPGA and various external components such as sensors, actuators, and memory.

Benefits of the Architecture

The architecture of the Cyclone 10 LP 10CL025YU256I7G FPGA has been meticulously crafted to offer a versatile and high-performing platform for implementing a diverse array of digital designs. The configurable logic blocks, memory elements, DSP blocks, and routing resources of this technology allow designers to develop personalized digital circuits that are optimized for specific applications.

2.4.4 Implementing in SPI

When implementing the SPI protocol on this board, it is important to take into account various factors. The FPGA board provides specific pins for SPI communication, including Serial Clock (SCLK), Master Out Slave In (MOSI), Master In Slave Out (MISO), and Chip Select (CS), which enable easy interfacing with SPI devices. Creating or implementing an SPI controller is crucial for effectively managing the communication protocol. FPGA development tools, like Intel's Quartus Prime, offer IP cores for SPI controllers, which streamline the implementation process. Configuring the SPI controller requires fine-tuning parameters such as clock frequency, data format, and mode to suit the specific needs of the connected SPI devices. SPI communication follows a clearly defined protocol, where the master device starts communication by asserting the chip select (CS) line. This is then followed by synchronous data transfer using the clock signal.

2.4.5 Application & Need

- *What are the applications of this FPGA Board?*

Applications	**Descriptions**
Internet of Things (IoT) Devices	The Cyclone 10 LP FPGA board is ideal for Internet of Things devices because to its low power operation. Many of these gadgets run on rechargeable batteries. The FPGA is perfect for Internet of Things applications due to its ability to mix performance with power efficiency.
Industrial Automation and Control Systems	In industrial automation, processing in real-time and precise control are of the utmost importance. Industrial sensor connections, motor controls, and communication interfaces are just a few of the many uses for the Cyclone 10 LP FPGA board's low power operation, digital signal processing blocks, and logic parts.

Automotive Electronics	Automobile electronics are another area where the FPGA board finds use. When saving electricity is of the utmost importance, its low power consumption becomes an asset. It has several potential applications, including control systems, sensor interfacing, and communication interfaces in automobiles.

Table 2.4.5.1. Application of FPGA -Personal Elaboration

- *Why it's Used Most?*

There are a number of applications for the popular Intel Cyclone 10 LP (10CL025YU256I7G) FPGA board.

Reasons	**Descriptions**
Low Power Operation	The FPGA board's low power consumption is one of its notable advantages. Particularly for applications that rely on battery power or prioritize energy economy, this is of the utmost importance in today's electronics.
Cost - Effectiveness	An excellent compromise between price and performance is offered by the Cyclone 10 LP series of field-programmable gate arrays (FPGAs). Applications where financial restrictions are an issue will find it to be a desirable alternative because of this.
Versatility	The field-programmable gate array (FPGA) board, which combines logic parts, embedded memory, digital signal processing (DSP) blocks, and phase-locked loops (PLLs), offers a flexible platform for executing various digital designs. Customization is possible to match the needs of different uses.

Table 2.4.5.2. Why use? - Personal Elaboration

2.5 Trade-offs, and Application of FPGA

Field-programmable gate arrays (FPGAs) are versatile electrical components with many uses. To make good use of them, you must be familiar with their advantages, disadvantages, and common applications.

2.5.1 Trade-offs

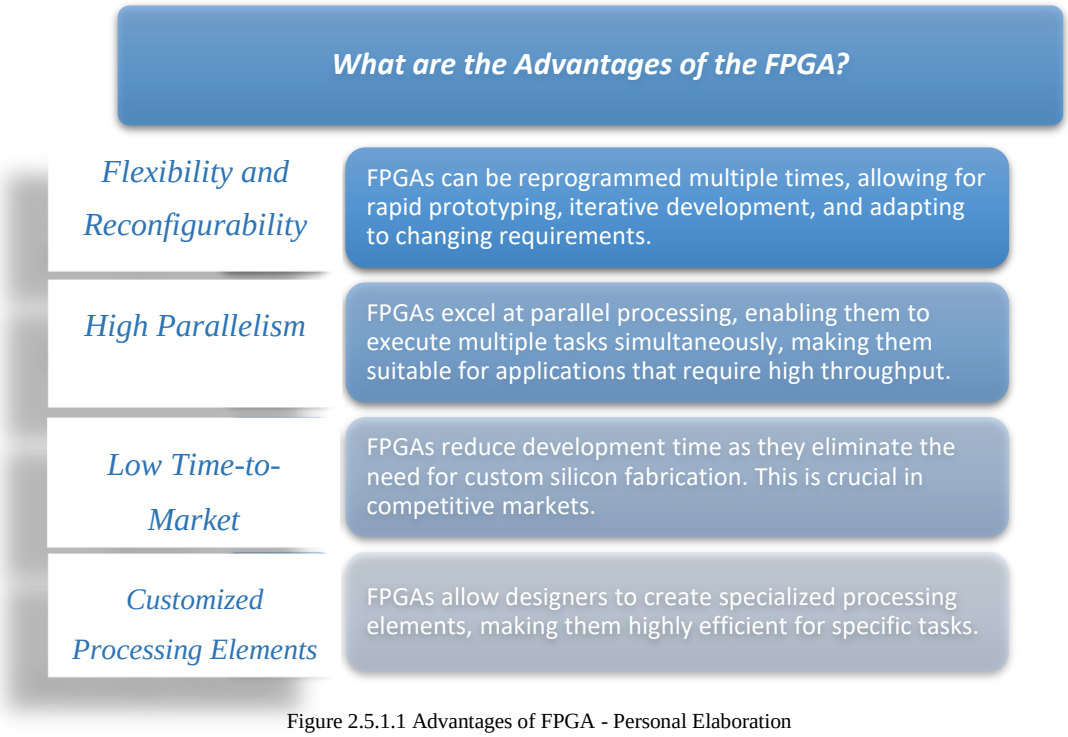


Figure 2.5.1.1 Advantages of FPGA - Personal Elaboration

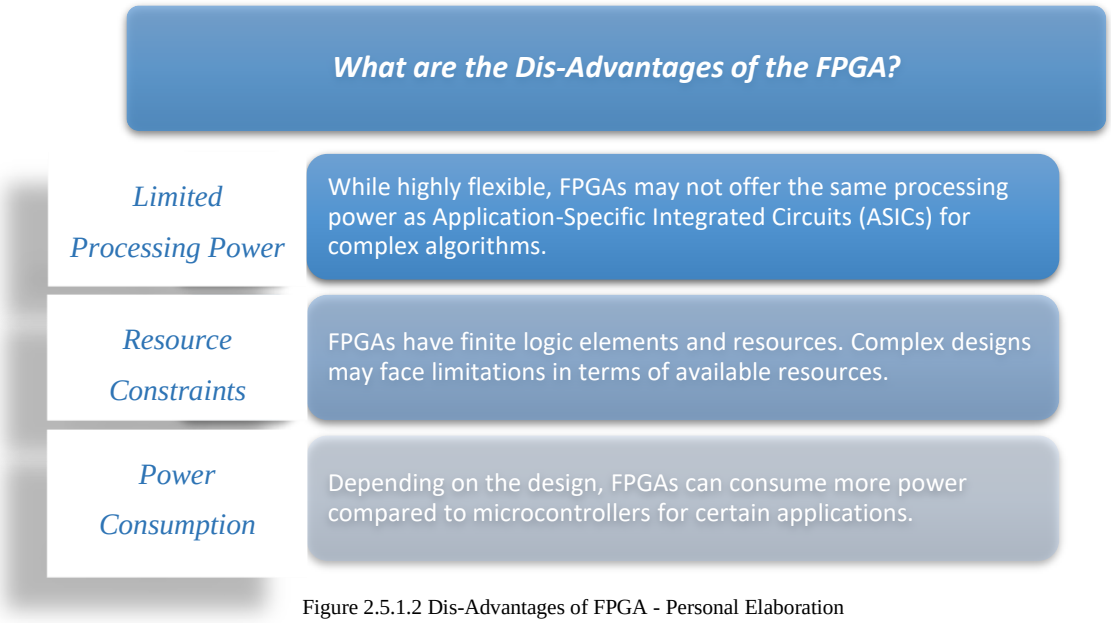


Figure 2.5.1.2 Dis-Advantages of FPGA - Personal Elaboration

2.5.2 Applications

This paper focuses on a selection of FPGA applications that are actively employed in various real-world scenarios.

- In the realm of Digital Signal Processing (DSP), FPGAs play a crucial role, particularly in

the processing of audio and video signals. Their ability to handle parallel processing tasks makes them ideal for such applications;

- Within Automotive Electronics, FPGAs are instrumental in managing diverse tasks ranging from engine control to safety features, and even in the sophisticated domain of infotainment systems;
- The field of Medical Imaging Systems sees FPGAs being extensively utilized in devices like MRI, CT, and ultrasound machines. Here, they contribute significantly to real-time image processing and enhancement, a critical aspect of modern medical diagnostics;
- In Aerospace and Defence, FPGAs are key components in various systems. They are vital in radar systems, avionics, and unmanned aerial vehicles (UAVs), facilitating functions such as signal processing and encryption;
- The technology also finds important applications in Automotive Advanced Driver Assistance Systems (ADAS). FPGAs are harnessed for critical tasks including object detection, lane tracking, and collision avoidance, enhancing vehicle safety and driver assistance.

These examples underscore the versatility and significance of FPGAs in contemporary technology applications. The discussion will pivot to VHDL in an upcoming chapter, delving into another crucial aspect of digital system design.

Chapter III: VHSIC HARDWARE DESCRIPTION LANGUAGE(VHDL) IMPLEMENTATION

3.1 Introduction

Once we have grasped the concepts of SPI and FPGA, it becomes crucial to consider the choice of programming language for our paper and how we will effectively implement it in our task. Furthermore, we will explore all aspects of this language within this chapter.

VHDL is a versatile language that allows for the precise description of electronic systems' behavior and structure. This technique is commonly used in digital design to create models and simulate intricate circuits prior to their physical implementation on hardware platforms. In this chapter, we will explore the application of VHDL in designing a system that utilizes the SPI protocol, previously introduced in the initial chapter.

3.1.1 History of VHDL

Let's dive into the fascinating world of VHDL language and explore a wide range of captivating subjects.

VHDL emerged as a solution to address the increasing complexity of integrated circuits. This project was developed as part of the Very High-Speed Integrated Circuit (VHSIC) program, an initiative by the U.S. Department of Defence aimed at advancing semiconductor technology.

VHDL is an acronym for VHSIC Hardware Description Language. This language is widely used to describe the behaviour and structure of electronic systems in a powerful and standardized way. The development of VHDL dates back to the 1980s when it was created by the U.S. Department of Defence. Its purpose was to establish a standardized method for describing electronic systems, enabling both simulation and synthesis.

This language is commonly used in the field of hardware design to generate and describe the behaviour of digital circuits and systems. This tool is versatile and can be utilized for both the creation and modelling of digital circuits. This tool is utilized for building digital systems and circuits by employing Programmable Logic Devices like Complex Programmable Logic Device (CPLD) or FPGA. VHDL code is commonly utilized for implementing digital circuits in CPLDs and FPGAs, as well as for fabricating ASICs (Application Specific Integrated Circuit).

The Institute of Electrical and Electronics Engineers (IEEE) has made a major impact in

establishing VHDL as a standard. The initial standardized version, IEEE 1076-1987, established a structure for describing digital systems. Over time, numerous revisions have been implemented, with the most recent one being IEEE 1076-2008

3.1.2 Purpose and Usage

In this section, we can focus on the fundamental requirements and explore their practical applications.

- *Modelling and Simulation*

VHDL is commonly used to model and simulate digital circuits. Designers have the ability to utilize VHDL to craft an abstract representation of a digital system, enabling them to observe its behavior under various conditions. This process is instrumental in identifying and resolving design issues prior to the physical implementation.

- *Synthesis for Implementation*

VHDL is also utilized for synthesis, which involves transforming a high-level description of a digital system into a gate-level representation that can be implemented on hardware platforms such as FPGAs and ASICs. The synthesis process converts VHDL code into a netlist, which depicts the logical elements and their connections.

3.1.3 VHDL Abstraction Level

The levels of abstraction pertain to distinct phases of design representation, each presenting different levels of detail and intricacy. These levels assist in the management of electronic systems' complexity and aid in design during various stages of the development process.

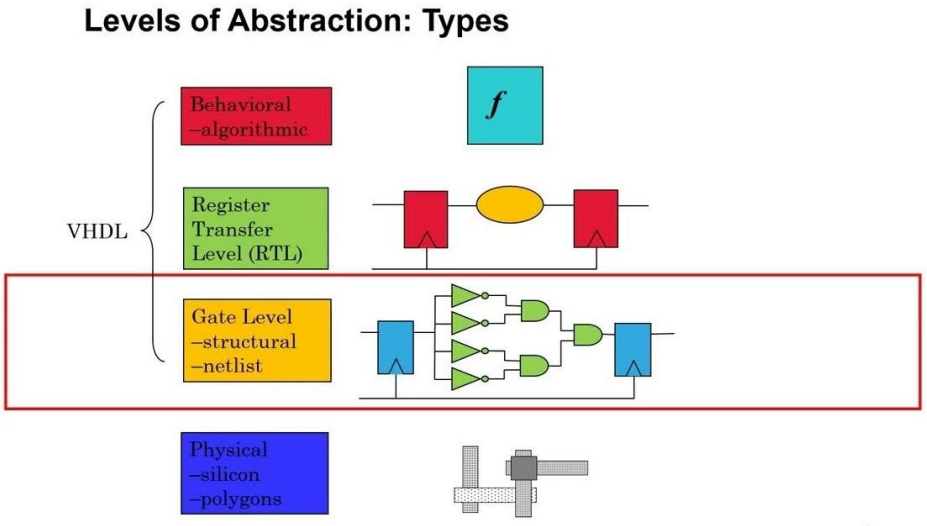


Figure 3.1.3.1 Abstraction Level of VHDL

Source: www.cadence.com

Now that we have examined the overall diagram of the abstraction level, let's delve into each of these levels one by one.

1. Behavioural Level

When it comes to the academic and creative aspects, the emphasis lies in describing the functionality or behaviour of a digital system without delving into its internal structure or implementation details. In this level, you explore constructs that imitate the behaviour of electronic components without diving into their physical implementation.

2. Register-Transfer Level (RTL)

The RTL level offers a more intricate perspective of the design in contrast to the behavioural level. The text explains the process of transferring data between registers and performing logic operations between them. At this stage, you begin to focus on the precise timing and order of operations.

3. Gate Level

Specifying the logical gates and their interconnections within the design is an essential part of the gate level abstraction. This level focuses on the practical implementation, depicting the tangible gates (AND, OR, NOT, etc.) and their interconnections.

4. Structural/Physical level

Describes a comprehensive depiction of a digital system, outlining its physical components and how they are connected. At this level, the design is explained using gates, flip-flops, multiplexers, and other fundamental electronic components, along with how they are connected together.

3.2 Understanding VHDL Language

Let's delve into the VHDL language syntaxes and explore their importance in understanding the simulation concept. We will also explore some testbench material to aid in our understanding of the simulation concept.

3.2.1 Key Concept in VHDL

In VHDL, the organizational structure consists of design units, serving as reusable blocks of code. The primary design units encompass:

- Entity: This delineates the interface of a module, outlining its inputs and outputs.

- Architecture: It specifies the behavior of a module. An entity can have multiple architectures, each providing distinct implementations.
- Configuration: Describes the interconnection of various modules within a design.
- Package: Houses globally accessible declaration

3.2.2 Understanding Entity and Architecture behavioural

In VHDL, an entity defines the description of a hardware module, offering an external perspective of the circuit. Examples of entities include logic gates and multiplexers. It outlines the entity's name and interface ports, which are signals or terminals facilitating communication between devices. For entities, at least one architecture must be present.

The internal details of the design entity, encompassing its behavior, structure, or a combination of both, are provided by the architecture. Each entity has its own declaration, specifying:

- Port number
- Port direction
- Port types
- Port timing information

Entities can have inputs (in), outputs (out), input-outputs (in-out), and buffers as possible ports. Within the architecture, input ports are read-only and cannot be changed. Conversely, output ports are write-only and cannot be read. If an output or input port requires reading (e.g., to determine its value), it must be created as an in-out or buffer port.

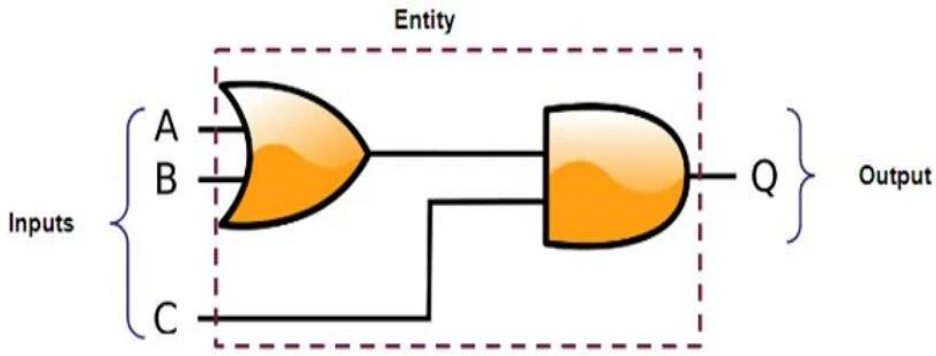


Figure 3.2.2.1 Entity

Source: copperpod.medium.com

- *What is the Architecture Behavioural?*

VHDL utilizes entity-architecture pairs to comprehensively define the operation of a circuit. An architecture encompasses the inner workings of a circuit, comprising a multitude of signals, operations, processes, and functions. It can take on either a structural or behavioural form. The architectural statement of the entity highlights its fundamental functionality. Architecture is

intrinsically linked to an entity and defines its behaviour. Architecture consists of two components: a declarative section, which is optional, and a statements section, which contains the code. The academic aspect can encompass similar elements to those found in an entity's declarative section, along with component declarations and configuration requirements. The VHDL statements are included in the latter. Architecture, much like any other entity, can be given a wide range of names, allowing for both academic and creative expression.

The VHDL Architecture encompasses four different modelling styles within its code structure.

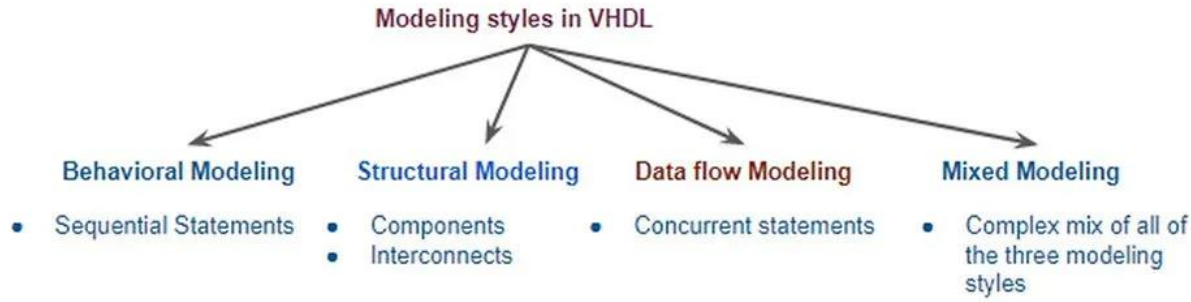


Figure 3.2.2.2 Modelling Style in Architecture

Source: copperpod.medium.com

Let's explore some examples of entity and architecture in VHDL language:

Entity: We have a total of four ports, with three for input and one for output. As depicted in the diagram below.

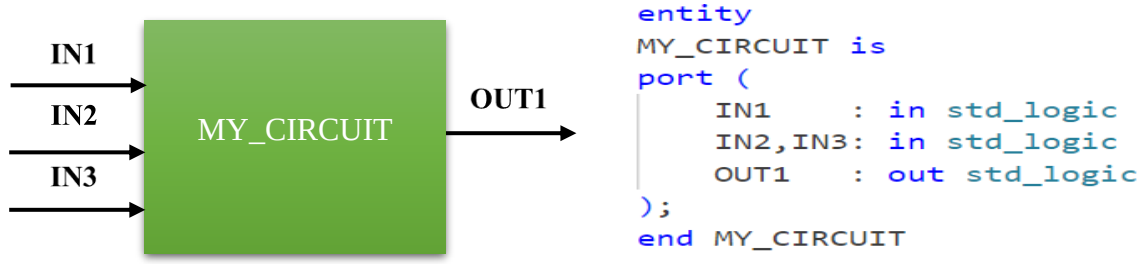


Figure 3.2.2.3 Entity MY_CIRCUIT & VHDL Code – Personal Elaboration

Architecture: It consists of statements that depict the entity's behaviour. Every entity is inherently linked to an architectural framework.

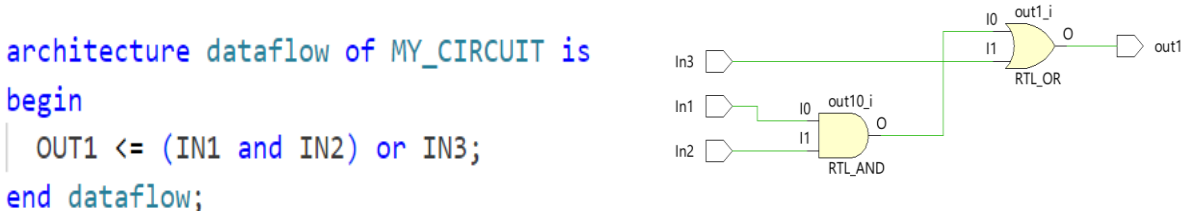


Figure 3.2.2.4 Architecture MY_CIRCUIT & VHDL Code – Personal Elaboration

3.2.3 Data Types

Let's delve into the data types utilized in VHDL and explore their practical applications.

VHDL employs various data types to represent diverse information, providing a structured approach to modelling digital systems. Each data type possesses unique attributes and behaviours. A solid understanding of VHDL data types is crucial for effectively describing the behaviour and structure of electronic circuits.

Standard Logic (std_logic):

One of the foundational VHDL data types, std_logic, is pivotal for representing digital signals. It can take on values such as '0', '1', 'Z' (high impedance), 'W' (weak unknown), and 'L'/'H' (weak '0'/'1'). In applications like flip-flops, std_logic is used to denote possible states, such as '0' or '1'.

Integer and Real:

Integer, a data type for representing integer values, finds common use in loop counters, array indexing, and VHDL arithmetic operations. Real, on the other hand, represents real numbers with decimal fractions and is employed in mathematical computations and simulations involving non-integer values. For instance, integer types might track clock cycles in a counter module, while real types could represent continuous values like voltage levels in analog circuit modelling.

Arrays:

Arrays are instrumental in organizing and manipulating collections of data in a structured manner. An example is the std_logic_vector, an array type used to represent buses or vectors of digital signals. For instance, a 4-bit binary number can be conveniently expressed as a std_logic_vector (3 downto 0).

Signed/Unsigned Numbers:

In VHDL, signed and unsigned are specialized data types used for representing signed and unsigned numbers, respectively. They are particularly useful for arithmetic operations in digital designs.

- Signed Number:
    - Represents both positive and negative integer values.

- Allows arithmetic operations involving addition and subtraction.
- Range is from -2^(N-1) to 2^(N-1)-1, where N is the number of bits.

➢ Unsigned Number:

- Represents positive integer values only.
- Suitable for arithmetic operations involving addition.
- Range is from 0 to 2^N-1, where N is the number of bits.

3.2.4 Assignment Operator and Statements

In VHDL, the assignment operator (<=) is a crucial construct that is utilized to assign values to signals and variables. Having a solid grasp of how the assignment operator functions is essential for effectively explaining the behavior of digital circuits.

The assignment operator (<=) is utilized for assigning values to signals or variables. Understanding the flow of information within a design is crucial for describing digital systems.

➢ *Signal Assignment*

Immediate Execution: Signal assignments take effect immediately when executed. They occur concurrently with other statements in a process.

Syntax is 'Signal_Name <= Value;'

➢ *Variable Assignment*

Deferred Execution: Variable assignments do not take effect until the process completes its execution. This means that variables can be assigned values multiple times within a process, and only the final assignment is reflected.

Syntax is 'Variable_Name: = Value;'

What are Generics and Constants in VHDL?

➢ Generics

Generics provide a way to parameterize VHDL entities and components, allowing designers to customize the behavior of their designs without modifying the underlying code.

➢ Constants

Constants are static values that remain unchanged during simulation and synthesis. They are useful for defining values that are known and fixed at design time.

What is the process statement in VHDL?

In VHDL, the process statement is a fundamental construct used for describing the behavior of digital systems. It encapsulates a block of sequential statements that are executed in a specific order. Understanding how to use the process statement is crucial for accurately modeling the behavior of electronic circuits.

- Syntax of process statement

```
process (sensitivity list) is
  -- Declarations (signals, variables, constants)
begin
  -- Sequential statements
end process.
```

Sensitivity list: A list of signals or events that trigger the execution of the process. When any signal in the sensitivity list changes, the process is executed.

Declarations: Optional declarations of signals, variables, constants, or other elements used within the process.

Sequential statements: The actual behavior of the process, including assignments, conditionals, loops, and other sequential constructs.

1. *IF-THEN-ELSE Statements*

The IF-THEN-ELSE statement is used to execute different sets of statements based on a condition.

- Syntax for this statement is,

```
if condition then
  -- Statements when condition is true
else
  -- Statements when condition is false
end if;
```

2. *FOR Loop Statement*

The FOR loop allows you to iterate over a range of values and perform a set of operations for each iteration.

- Syntax for this statement is,

```
for loop_variable in range loop
  -- Statements to be executed
end loop;
```

3. CASE Statement

The CASE statement provides a way to select among multiple alternatives based on the value of an expression.

- Syntax for this statement is,

```
case expression is
  when value_1 =>
    -- Statements when expression equals value_1
  when value_2 =>
    -- Statements when expression equals value_2
  when others =>
    -- Statements for other cases
end case;
```

3.2.5 Testbench in VHDL

In this section, we will explore the process of developing a testbench and understanding its purpose and functionality.

A testbench in VHDL serves as a simulation environment that ensures the design's functionality is thoroughly validated. Designers have the opportunity to utilize inputs, simulate the design being tested, and observe the outputs in order to ensure proper functionality.

The main objective of a testbench is to ensure that a digital design satisfies its specifications and operates accurately in various scenarios. It provides a digital space for experimentation prior to real-world application.

- *Components of a Testbench*

Testbench Architecture: A testbench is typically implemented as a separate VHDL file, complete with its own entity and architecture.

Instantiation of the Design Under Test (DUT): The module being tested, known as the Design Under Test (DUT), is instantiated within the testbench.

Stimulus Generation: Testbenches generate input signals to simulate various scenarios and test cases, ensuring a comprehensive evaluation.

Output Monitoring: Monitoring the outputs of the DUT, the testbench compares them against expected results to verify correctness.

Testbench Processes: VHDL processes play a vital role in controlling the simulation flow, applying inputs, and validating outputs.

➢ *Structure of a Testbench*

A typical testbench has the following components:

Entity Declaration: The testbench entity declares essential input and output ports, signals, and generics if necessary.

Architecture: The architecture encompasses simulation code and processes that interact with the Design Under Test (DUT).

Instantiation of the DUT: Within the architecture, the DUT is instantiated using a component declaration.

Signal Declarations: Signals are declared to establish connections between the testbench and the DUT's ports.

Stimulus Generation: Dedicated processes generate stimulus by applying inputs to the DUT, facilitating dynamic testing.

Output Monitoring and Checking: Additional processes monitor the DUT's outputs, ensuring they align with expected results through systematic checks.

Simulation Control: Processes governing the simulation flow, including starting and stopping conditions, contribute to a well-structured and controlled testbench environment.

The simple structure of testbench can be seen in the VHDL diagram below.

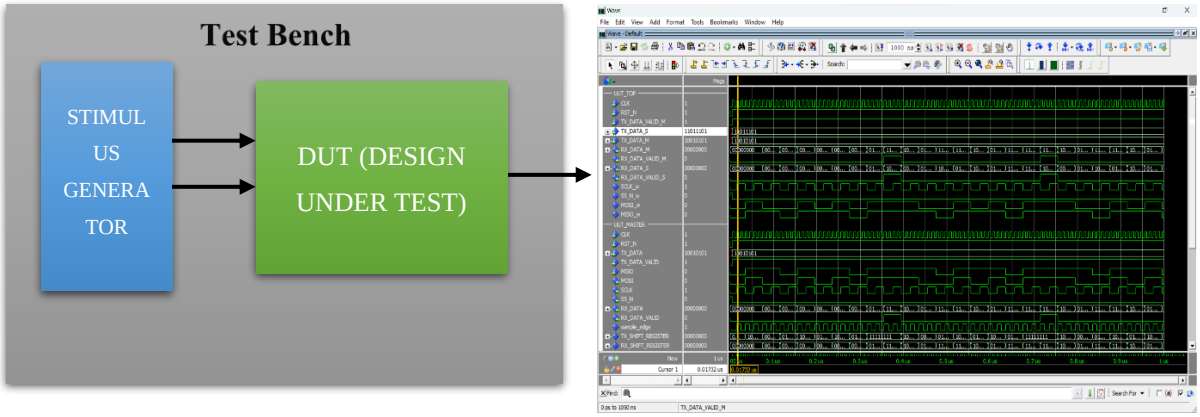


Figure 3.2.5.1 Testbench Example – Personal Elaboration

3.3 VHDL Implementation on SPI Protocol

After grasping the SPI protocol in the initial chapter, it is necessary to develop a VHDL design

for this protocol. Consequently, I have devised four distinct cases for the SPI modes: 0, 1, 2, and 3. Both have identical context code, but the value fluctuates depending on the phase of CPOL and CPHA.

For the VHDL file, I generated four separate files, each corresponding to a specific step. These files were labeled as case 1, case 2, case 3, and case 4. In the first scenario, there are four files: SPI Master, SPI Slave, SPI Top Module (which connects the Master module and Slave module), and SPI Testbench for simulation.

Here we can explore a code that can be applied to various cases, with the only difference being the values that change based on the phase of CPOL and CPHA.

3.3.1 VDHL Code

Let us discuss the approach to employ to complete the SPI protocol in these three modules.

- *SPI Master Module*

The module allows configuration of various parameters, including clock polarity (CPOL) and clock phase (CPHA), which can take values 0, 1, 2, or 3, representing different modes of operation. Four modes are supported, each defining specific clock polarities and phases, influencing data transmission.

The entity 'SPI_MASTER' declares generic parameters for CPOL, CPHA, data length, and clock division. It contains input and output ports for clock, reset, transmitted data (TX_DATA), transmit data validity (TX_DATA_VALID), master in slave out (MISO), master out slave in (MOSI), serial clock (SCLK), slave select (SS_N), received data (RX_DATA), and received data validity (RX_DATA_VALID).

Within the architecture 'Behavioral,' signals like sample_edge, shift registers for transmit (TX_SHIFT_REGISTER) and receive (RX_SHIFT_REGISTER), counters for transmit (TX_BIT_COUNTER) and receive (RX_BIT_COUNTER), as well as internal signals for SS_N and SCLK, are declared.

The functionality is divided into processes. The SCLK Generation Process generates the serial clock (SCLK_INT) based on the configured CPOL and CPHA values, toggling the clock edges according to the data validity and specified clock phase.

The SS_N Process controls the slave select signal, activating it based on the validity of transmitted data and counter values.

The module implements two sets of processes for transmission (TX_CPOL_falling, TX_CPOL_rising) and reception (RX_falling, RX_rising) based on the configured CPOL value. These processes handle data transmission and reception at falling or rising edges of the clock, respectively. They manipulate the shift registers and counters based on clock edges and slave select signals, managing the data flow during SPI communication.

Overall, this VHDL code provides a flexible SPI master module that accommodates various SPI modes through its generic parameters, allowing for versatile integration into larger digital systems requiring SPI communication capabilities.

- *SPI Slave Module*

The module's generics CPOL (clock polarity) and CPHA (clock phase) enable configuration of the SPI mode, allowing for four distinct modes of operation characterized by different clock polarities and phases. Each mode is represented by specific combinations of CPOL and CPHA, facilitating diverse communication scenarios.

The 'SPI_SLAVE' entity defines generic parameters for CPOL, CPHA, and the data bit length. It consists of input and output ports for clock (SCLK), slave select (SS_N), master out slave in (MOSI), master in slave out (MISO), asynchronous active low reset (RST_N), received data (RX_DATA), received data validity (RX_DATA_VALID), and transmitted data (TX_DATA).

Within the 'Behavioral' architecture, signals like shift registers for transmit (TX_SHIFT_REGISTER) and receive (RX_SHIFT_REGISTER) along with counters for transmit (TX_BIT_COUNTER) and receive (RX_BIT_COUNTER) are declared.

The architecture encompasses two sets of processes, distinguished by CPOL values, facilitating data reception and transmission based on the configured CPOL. For both falling edge (rx_CPOL_falling, tx_falling) and rising edge (rx_CPOL_rising, tx_rising) scenarios, processes manage data reception from the master (MOSI) and transmission to the master (MISO). These processes manipulate shift registers and counters, enabling the module to receive and transmit data in synchronization with the clock (SCLK) and slave select (SS_N) signals.

- *SPI TOP Module*

'SPI_TOP' is a module that enables communication between a master and a slave device using the Serial Peripheral Interface (SPI) protocol. The entity declares generic parameters CPOL (clock polarity), CPHA (clock phase), data length (DATA_LENGTH), and clock division

(CLK_DIV) for configuring the behavior of the SPI communication. The port list includes connections for clock (CLK), reset (RST_N), transmit data validity for master (TX_DATA_VALID_M), transmitted data for master (TX_DATA_M), received data for master (RX_DATA_M), received data validity for master (RX_DATA_VALID_M), transmitted data for slave (TX_DATA_S), received data for slave (RX_DATA_S), and received data validity for slave (RX_DATA_VALID_S).

The architecture incorporates components called 'SPI_MASTER' and 'SPI_SLAVE' to establish the communication interface. The 'SPI_MASTER' and 'SPI_SLAVE' components represent the master and slave SPI modules, respectively. They have both generic configurations and specific port mappings.

The 'SPI_MASTER' component oversees the functionality of the master device in the SPI communication. The system integrates the generic configurations and port mappings received from the entity 'SPI_TOP'. In the same vein, the 'SPI_SLAVE' component symbolizes the subordinate device and establishes connections with the higher-level module. The behavior of the system is established within the SPI communication setup using the configured parameters.

The 'begin' block includes the creation of 'UUT_MASTER' and 'UUT_SLAVE' instances for the 'SPI_MASTER' and 'SPI_SLAVE' components, respectively. These instantiations connect the generic configurations and ports of the components to the corresponding parameters and signals of the top-level module 'SPI_TOP.' This enhances the communication between the master and slave devices by synchronizing their operations and data transfer based on the specified SPI configurations and connections.

In this VHDL code, a top-level entity called 'SPI_TOP' is created to facilitate communication between a master and a slave device using the SPI protocol. The code is designed to be modular and configurable, allowing for flexibility in its implementation. It offers a structure for seamlessly integrating and managing the actions of the primary and secondary modules in an SPI communication system.

Once the final simulation results generated by the ModelSim software are observed, the SPI Testbench can be accessed in the subsequent chapter dedicated to the results. In addition, the Appendix chapter includes all of the VHDL code files.

3.4 ModelSim for Simulation

In this section, we will primarily delve into the ModelSim software and its application in

simulating the behavior of the design.

In order to conduct RTL simulation for the VDHL design mentioned above, I made use of ModelSim software to thoroughly examine the design and confirm its functionality. I will describe the process of developing my project, including the use of software simulations and the presentation of results in the outcomes chapter.

3.4.1 Introduction

ModelSim is a versatile digital design and verification tool that is highly popular in the field of electronic design automation (EDA). This software is developed by Mentor Graphics, which is now a part of Siemens Digital Industries Software. ModelSim is a powerful tool that simplifies the process of simulating and verifying digital circuits written in hardware description languages (HDLs) like VHDL and Verilog. It provides the opportunity to simulate and debug FPGA designs prior to synthesis and implementation.

3.4.2 Key Features of Modelsim

When exploring the main features of ModelSim, you'll discover a highly adaptable simulation tool that meets the varied requirements of digital design experts. The language support of ModelSim is exceptional, as it can handle both VHDL and Verilog. This provides users with the flexibility to work with different Hardware Description Languages (HDLs). Our simulation capabilities cover a wide range of abstraction levels, allowing designers to gain a holistic understanding of their designs. It is worth mentioning the advanced debugging capabilities, which include features like waveforms, breakpoints, and the ability to inspect internal signals and registers. These features greatly enhance the debugging process. ModelSim enables mixed-language simulation, enabling the smooth integration of VHDL and Verilog modules in a single environment, promoting the development of complex mixed-language designs.

In addition, the tool is highly proficient in analyzing code coverage, guaranteeing a comprehensive evaluation of design components during simulation. The accuracy of the simulation process is further enhanced through time-based simulation, which is driven by events that trigger updates to signal values. ModelSim enables users to develop testbenches efficiently, allowing for thorough design verification. Emphasizing the importance of automation, the focus is on streamlining the process of compiling and managing libraries, which greatly simplifies the management of extensive projects. Finally, ModelSim effortlessly integrates with FPGA synthesis and implementation tools, allowing designers to thoroughly verify their designs before deploying them onto Field-Programmable Gate Arrays (FPGAs).

3.4.3 Create and Simulate the Project

Here is a systematic guide for creating, simulating, and debugging an FPGA design using ModelSim* - Intel® FPGA Edition 10.5B:

1. Develop Your FPGA Design:
    - Utilize an HDL (Hardware Description Language) like Verilog or VHDL for crafting your FPGA design.
    - Define the architecture, modules, and connections within your design.
2. Compile the Design:
    - Launch ModelSim and initiate a new project.
    - Add your HDL files to the project.
    - Compile the design to identify syntax errors and generate simulation files.
3. Construct a Testbench:
    - Formulate a separate HDL file (typically in Verilog or VHDL) referred to as a testbench.
    - The testbench should incorporate stimulus generation, providing inputs to your design, along with assertions to verify output correctness.
4. Simulate Your Design:
    - Initiate the simulation in ModelSim.
    - Configure the simulation environment to encompass your design files and the testbench.
    - Execute the simulation and observe the waveform outputs.
5. Debugging:
    - Employ the waveform viewer in ModelSim to visualize signals within your design.
    - Integrate probes to monitor specific signals of interest.
    - Step through the simulation to scrutinize the behavior of your design.
6. Addressing Issues:
    - Analyze the simulation results and pinpoint any disparities between expected and actual behavior.
        - Debug your design by thoroughly reviewing your HDL code, testbench, and simulation results.
7. Iterate and Repeat:
        - Implement necessary adjustments to your design and testbench based on debugging insights.

- Recompile and re-simulate the design iteratively until achieving the desired functionality.

Here is a general representation of how the software appears:

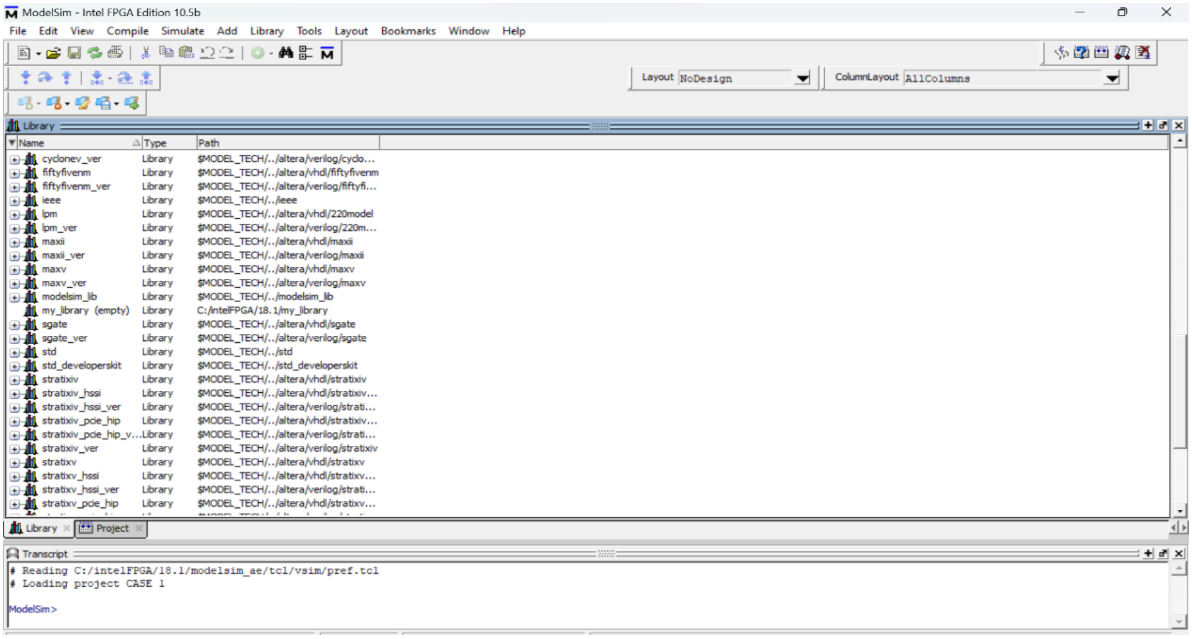


Figure 3.4.3.1 ModelSim-Intel FPGA Edition 10.5b

Now let's delve into the practical uses of this software.

3.4.4 Application of ModelSim

ModelSim is also commonly used in academia to educate digital design and simulation. Multifunctional software is crucial for connecting theoretical notions to actual applications in digital system development.

1. Digital System Development:

The utilization of ModelSim is prevalent in the creation of digital systems, spanning from modest integrated circuits to intricate microprocessors.

2. FPGA Design and Verification:

ModelSim is employed by engineers to validate the operational integrity of their designs prior to programming them onto Field-Programmable Gate Arrays (FPGAs).

3. ASIC Verification:

Within the realm of Application-Specific Integrated Circuit (ASIC) design, ModelSim serves as a crucial tool for validating custom digital circuitry before the commencement of the

fabrication process.

4. Education and Training:

In educational institutions, ModelSim stands as a widely embraced tool for imparting knowledge on digital design principles and simulation techniques.

3.5 Using Intel Quartus Prime

To finalize the design synthesis and implementation for the FPGA design flow following the creation and simulation of the project in ModelSim. We opted for Intel Quartus Prime software to successfully accomplish the task, as we were already aware that the FPGA board in question was an Intel Cyclone 10LP. I also shared the files I utilized to develop the project and explained the steps taken in our module file to achieve our outcomes.

Intel Quartus Prime is a top-notch software suite for FPGA design and development. It provides a wide array of tools to design, implement, and debug Field-Programmable Gate Arrays. Famous for its intuitive interface and powerful set of tools, Quartus Prime is a popular choice among engineers and designers for developing cutting-edge solutions in a wide range of industries.

Now, let's explore how to utilize the Intel Quartus Prime Lite Edition to create, synthesize, and build a project. Furthermore, we will explore the process of establishing a JTAG probe and customizing the Signal Tap Logic Analyzer to effectively debug and monitor.

Let's delve into the various topics in detail here.

3.5.1 Design Creation

The initial phase of any FPGA project involves developing the design. Intel Quartus Prime Lite Edition offers a user-friendly environment to streamline this process. Here are the steps to follow:

Launch Quartus Prime Lite Edition: Open the Quartus Prime Lite Edition software on your computer.

Create a New Project: Select File > New Project Wizard... and follow the prompts. Provide a name and location for your project and specify the target FPGA device.

Add Files: Add your design files (VHDL, Verilog, etc.) by right-clicking on your project in the Project Navigator, selecting Add/Remove Files in Project..., and browsing to the location of your design files.

Create a Top-Level Design Entity: Right-click on the added files in the Project Navigator, select Set as Top-Level Entity, and choose the top-level module for your design.

3.5.2 Synthesis

Synthesis involves converting your RTL (Register-Transfer Level) code into a netlist, which represents the logic gates and their connections. Here are the steps to follow:

Start Synthesis: In the Project Navigator, right-click on your top-level module and select Start Analysis & Synthesis.

View Synthesis Report: Once synthesis is complete, you can view the synthesis report to analyze the resource utilization, timing constraints, and other relevant information.

3.5.3 Implementation

The implementation requires translating the conceptual blueprint onto the precise components of the designated FPGA hardware. Here are the steps to follow:

Start Implementation: In the Project Navigator, right-click on your top-level module and select Start Assembler & Fitter.

View Fitter Report: After the implementation process, review the Fitter report for information on resource utilization, critical paths, and other key metrics.

3.5.4 JTAG Probe Configuration

A JTAG (Joint Test Action Group) probe allows you to interact with and debug your FPGA design. Follow these steps to set up a JTAG probe:

Connect JTAG Probe: Physically connect the JTAG probe to the JTAG header on the FPGA board.

Configure Hardware Setup: In Quartus Prime Lite Edition, go to Tools > Programmer. Select your FPGA device and hardware setup. Connect to the JTAG chain.

Verify Connection: Click Auto Detect to verify that the JTAG chain is properly connected to your FPGA board.

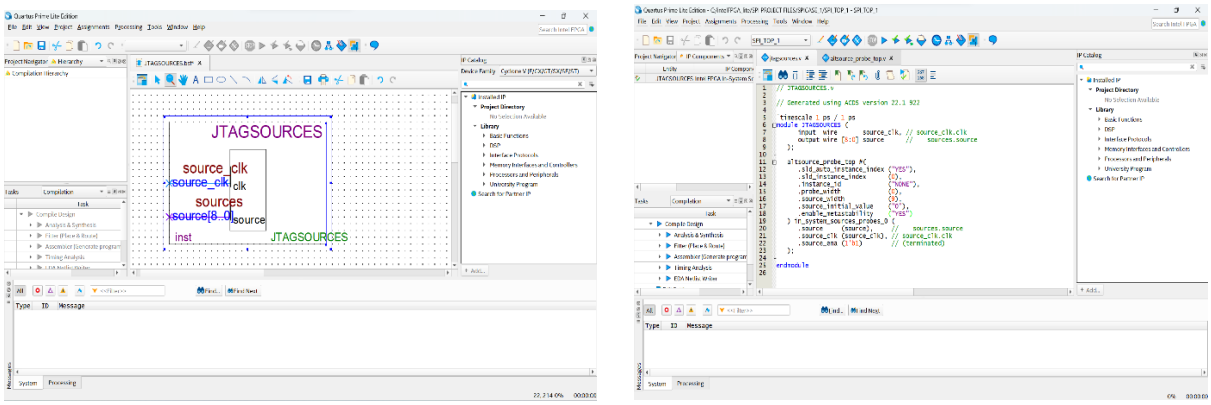


Figure 3.5.4.1 JTAG Sources and VHDL code – Personal Elaboration

For this, I modified my SPI Top file design to use JTAG sources to initiate SPI transactions from the master side and pre-load both master and slave data to be transferred as MOSI and MISO, respectively. JTAG probes and an internal logic analyzer were also utilized to validate the internal behavior. So, for the SPI Top module, I've included updated code that has been tested in Quartus Prime. And the revised code file that is found in the Appendix.

3.5.5 SignalTap Logic Analyzer Configuration

SignalTap Logic Analyzer allows you to monitor internal signals in your FPGA design. Follow these steps to configure SignalTap:

Open SignalTap: In Quartus Prime Lite Edition, go to Tools > SignalTap II Logic Analyzer.

Add Nodes: Add the signals you want to monitor by right-clicking on the node list and selecting 'Add Node'.

Compile and Load Design: Click Assign Nodes to associate the selected signals with their respective nodes in your design. Then, click Compile Design to implement the changes.

Start Capture: Once your design is running on the FPGA, click Start in SignalTap to begin capturing data. Below photo you can see I assign STP node.

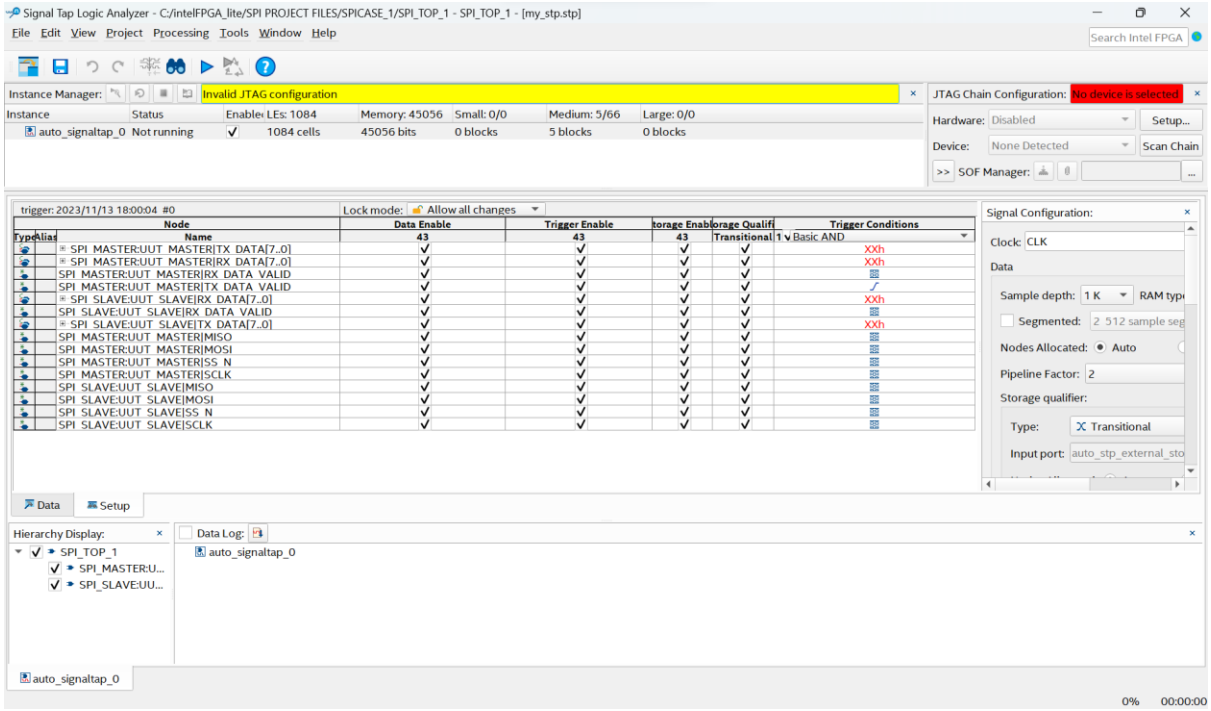


Figure 3.5.5.1 STP Setup in Quartus Prime – Personal Elaboration

3.6 Trade-offs, and Application of VHDL

In this section, we will look at the benefits and cons of using/applying this language in the actual world.

3.6.1 Advantages

1. Abstraction Levels: VHDL supports multiple levels of abstraction, allowing designers to work at higher, more conceptual levels or delve into detailed implementations.

2. Simulation and Verification: VHDL facilitates extensive simulation, aiding in design validation and bug detection prior to physical implementation.

3. Reusability: VHDL promotes modular design, enabling components to be reused across projects, saving time and effort.

4. Parallelism and Concurrency: VHDL's inherent support for concurrency allows for efficient modelling of parallel processes, a crucial aspect of modern digital systems.

3.6.2 Dis-Advantages

1. Steep Learning Curve: VHDL can be initially complex for newcomers due to its strict syntax and structural nature.

3. Limited Tool Support: While popular, VHDL may have fewer open-source tools compared

to other languages, potentially impacting accessibility.

4. Tool Dependence: The effectiveness of VHDL designs can be influenced by the choice of synthesis and simulation tools, and their specific features.

3.6.3 Application

1. ASIC Design: VHDL is widely used in Application-Specific Integrated Circuit (ASIC) design for its suitability in creating custom, specialized digital circuits.
2. FPGA Development: VHDL is a key language for Field-Programmable Gate Array (FPGA) development, allowing engineers to implement flexible and reconfigurable logic.
3. Digital Signal Processing (DSP): VHDL finds extensive use in DSP applications, where it's employed to model and simulate complex signal processing algorithms.
4. Microprocessor Design: VHDL is essential for designing microprocessors and microcontroller units (MCUs), playing a crucial role in modern computing systems.

Chapter IV: RESULTS AND TESTING

Upon thorough review of all aspects of the article, we are currently evaluating and experimenting with the findings we have uncovered. We should also focus on the significant simulation, synthesis, and on-board testing outcomes. Lastly, we can utilize an oscilloscope to confirm the accuracy of our findings.

4.1 ModelSim Results

This paper's aim is to guide through the verification environment before starting the simulation process. The master and slave modules of the SPI protocol are controlled and managed by simulation and software objects. These software-based entities act as virtual replacements for physical hardware modules, enabling the initiation of transactions and control of data lines within the simulation environment.

In the realm of simulation, these software objects are essential for replicating the behavior of the master and slave modules. They facilitate the initiation of communication transactions according to the SPI protocol specifications and regulate the exchange of data between these simulated components.

The main goal of the verification environment is to thoroughly assess the interaction, functionality, and compliance of the master and slave modules with regards to the SPI protocol's specifications. Through the use of pure simulation objects, it becomes possible to explore a wide range of scenarios, conduct comprehensive testing of different functionalities, and evaluate the strength and dependability of the SPI communication.

By conducting meticulous simulations within this environment, we thoroughly explore and validate potential issues, corner cases, and optimal operation conditions. This process guarantees that the SPI protocol's communication between master and slave modules follows established standards and operates consistently in a wide range of situations prior to practical application. The figure below illustrates the verification environment that I utilized. Next, we will discuss the four main SPI protocol cases/modes.

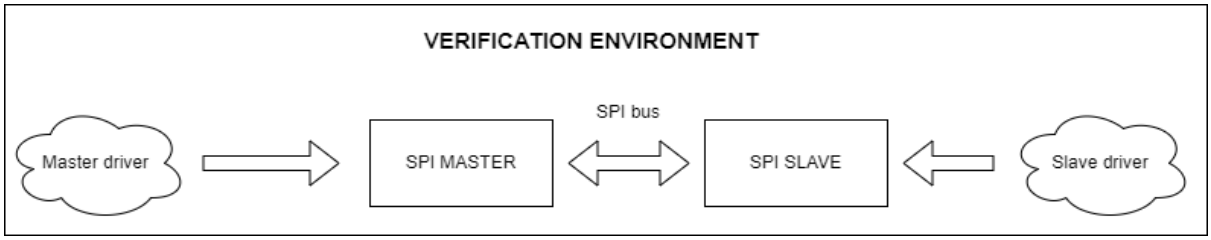


Figure 4.1.1 Simulation Setup in Software – Personal Elaboration

4.1.1 Four case Simulation Results

In the previous chapters, I discussed the four SPI cases or modes. Now, we will utilize these cases individually to observe the simulation's outcomes and examine the protocol behavior in ModelSim software. To accomplish this, we utilize modes 0, 1, 2, and 3, along with 00, 01, 10, and 11 for CPOL and CPHA, respectively.

In order to achieve a successful protocol simulation, the inclusion of a testbench is crucial when designing VHDL code for SPI. As I've mentioned before, a testbench plays a crucial role. In this report, I will provide an analysis of the results from each case study, focusing on the observed behavior and highlighting the important aspects that require our attention. By utilizing this information, we can enhance our approach and attain the best possible outcomes.

The inclusion of a testbench is crucial when designing and verifying digital systems, particularly when working with hardware description languages such as VHDL or Verilog. This simulation environment was created to test the functionality of a design, module, or system. It provides a platform for thorough testing and analysis. Now, we have the opportunity to examine case results and explanations of its nature and functionality. In our testbench file, I utilized various processes to gain a comprehensive understanding of the protocol's process and behavior.

The VHDL code is a testbench called TB_SPI_CASE that simulates an SPI communication between a master and a slave. This testbench is designed with a combination of academic rigor and creative thinking. It encompasses various elements such as signal declarations, component instantiation, clock generation, and stimulus processes.

The testbench sets up constants that define the SPI configuration parameters, such as clock polarity, clock phase, data length, and clock division. It lists several signals including CLK, RST_N, TB_RX_DATA_M, TB_RX_DATA_VALID_M, TB_TX_DATA_M, TB_TX_DATA_VALID_M, TB_RX_DATA_S, TB_RX_DATA_VALID_S, TB_TX_DATA_S. These elements play a vital role in facilitating communication and coordination among the testbench and the SPI components.

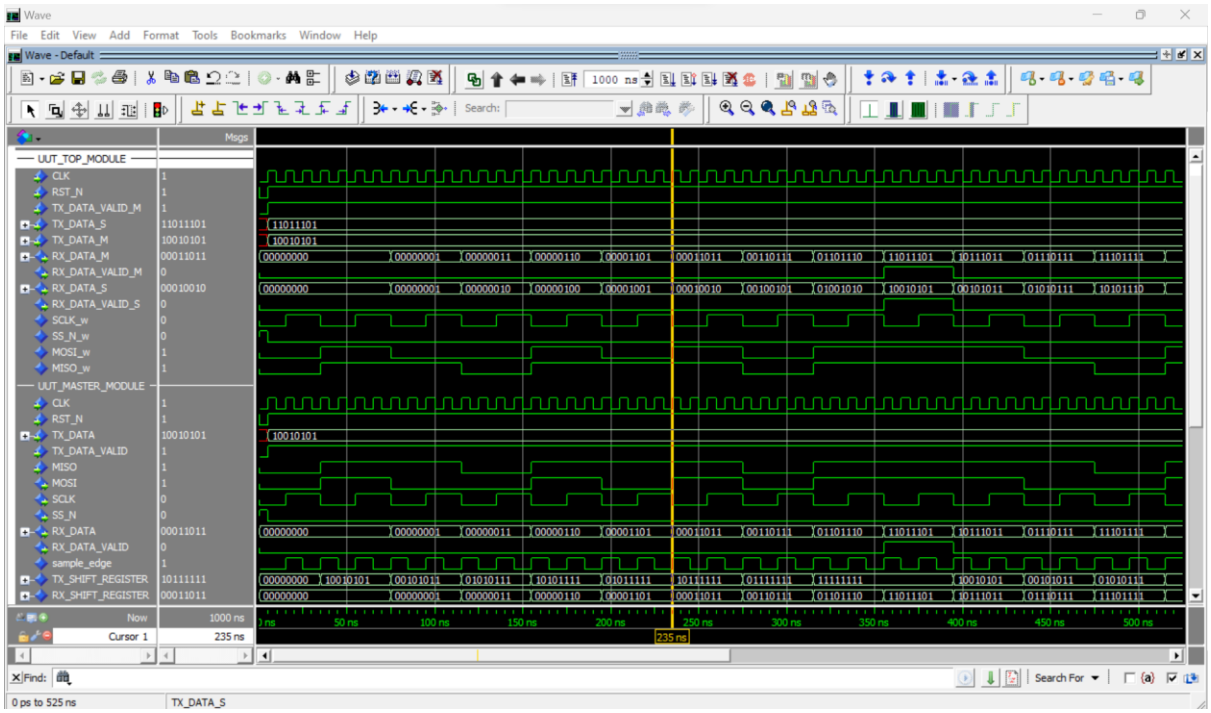
The SPI_TOP component is instantiated within the UUT_TOP block to configure the SPI master-slave pair. The mapping process involves assigning specific values to the configuration parameters of the SPI component, while the port mapping establishes communication channels by connecting the testbench signals to the ports of the SPI module.

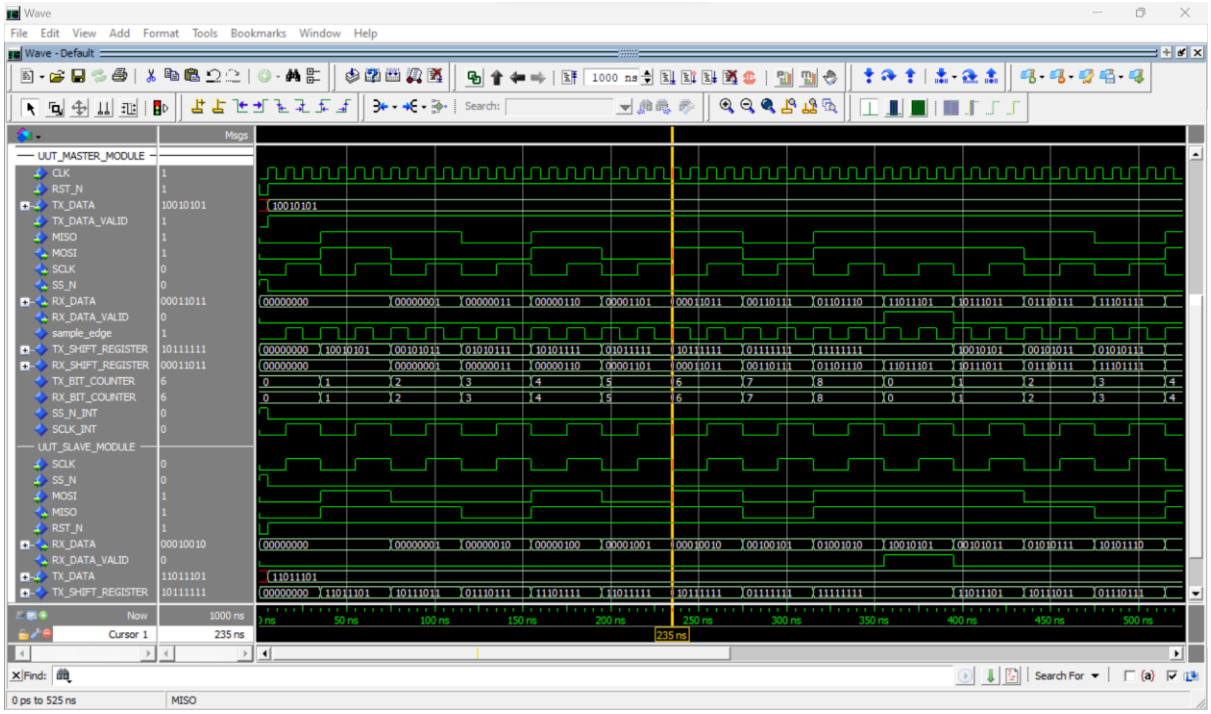
The clock generation process alternates the CLK signal every 5 ns, emulating a clock signal. A delay of 2.5 ns in the process guarantees a half-clock period.

The process of initiating SPI communication begins by activating the reset signal (RST_N) to '0'. It then waits for a clock edge to go high before setting the reset signal back to '1'. Following this, the master and slave transmit their predefined data sequences (TB_TX_DATA_M and TB_TX_DATA_S, respectively). The transmission process is signalled by enabling the valid flag (TB_TX_DATA_VALID_M).

After this, the process pauses until it detects data reception from both the master (TB_RX_DATA_VALID_M = '1') and the slave (TB_RX_DATA_VALID_S = '1'). When the data is received, it's displayed through report statements. This converts the binary data into an integer format, making it easier to read and interpret.

❖ *Mode 0 when we have CPOL and CPHA value are 0 and 0 respectively.*




Wave
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Wave - Default
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TX_DATA
TX_DATA_VALID
MISO
MOSI
SCLK
SS_N
RX_DATA
RX_DATA_VALID
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TX_SHIFT_REGISTER
RX_SHIFT_REGISTER
TX_BIT_COUNTER
RX_BIT_COUNTER
SS_N_INT
SCLK_INT
UUT_SLAVE_MODULE
SCLK
SS_N
MOSI
MISO
RST_N
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RX_DATA_VALID
TX_DATA
TX_SHIFT_REGISTER
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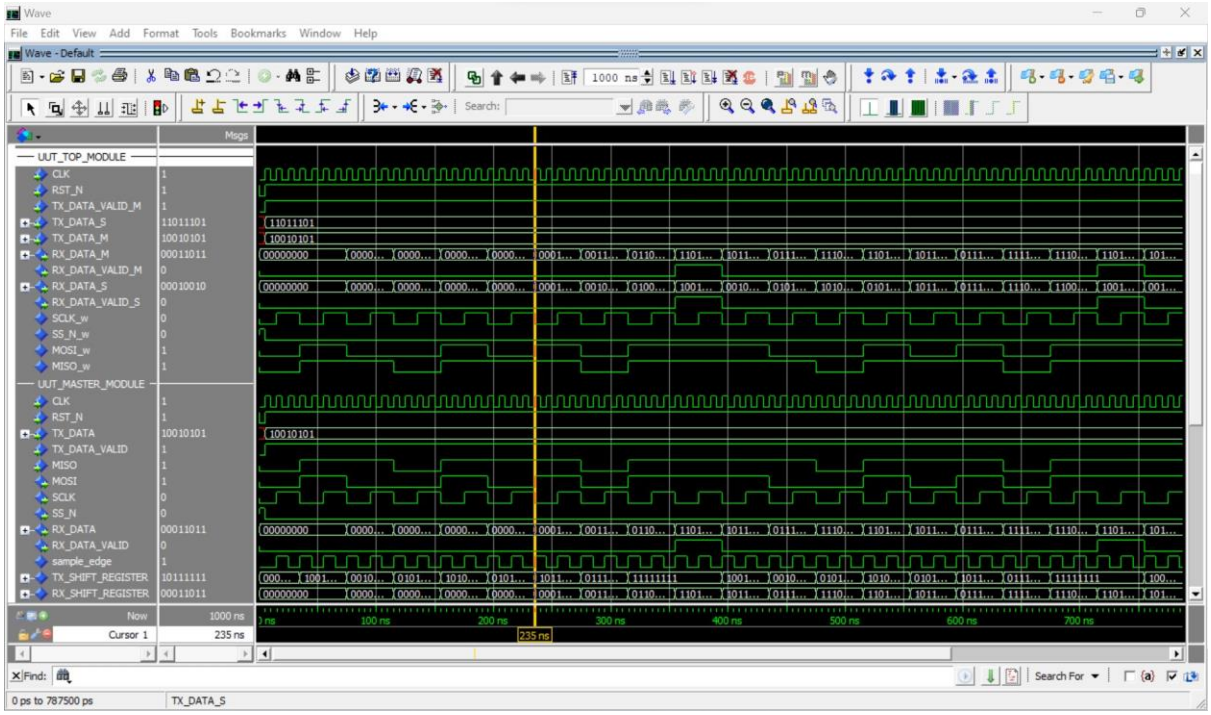
1000 ns
Cursor 1
235 ns
Find:
Search For
0 ps to 525 ns
MISO


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
UUT_TOP_MODULE
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TX_DATA_VALID_M
TX_DATA_S
TX_DATA_M
RX_DATA_M
RX_DATA_VALID_M
RX_DATA_S
RX_DATA_VALID_S
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SS_N_w
MOSI_w
MISO_w
UUT_MASTER_MODULE
CLK
RST_N
TX_DATA
TX_DATA_VALID
MISO
MOSI
SCLK
SS_N
RX_DATA
RX_DATA_VALID
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RX_SHIFT_REGISTER
Now
1000 ns
Cursor 1
235 ns
Find:
Search For
0 ps to 787500 ps
TX_DATA_S

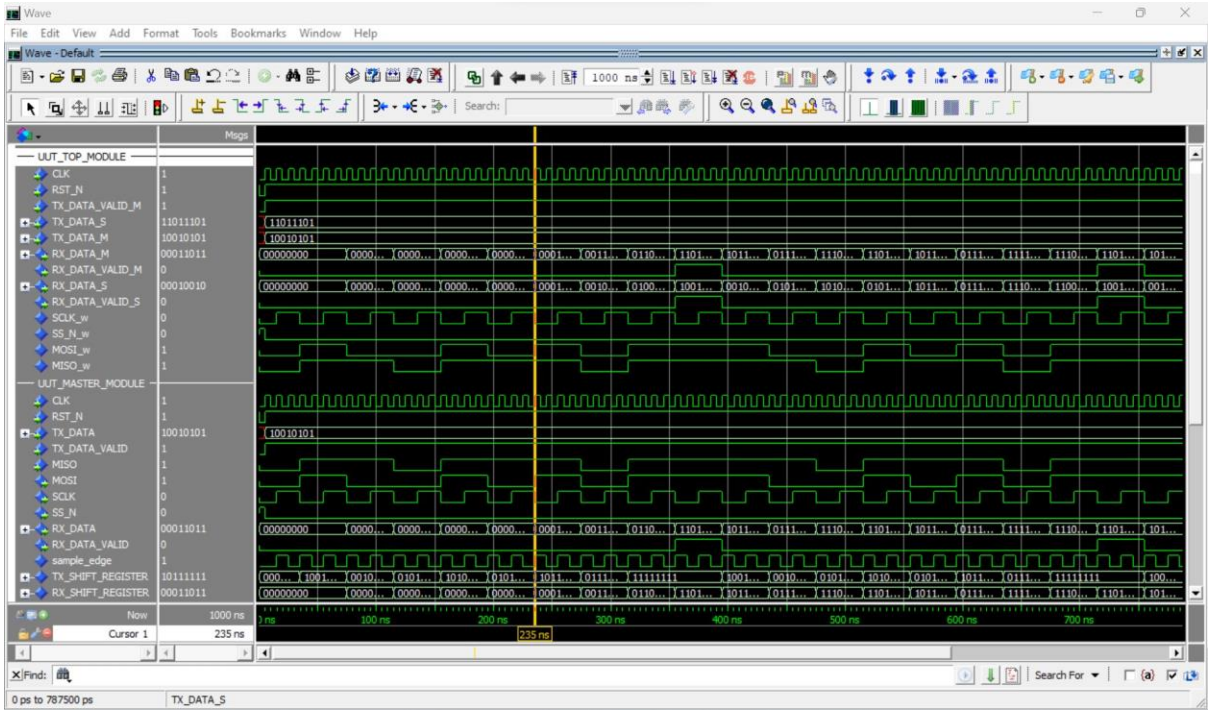


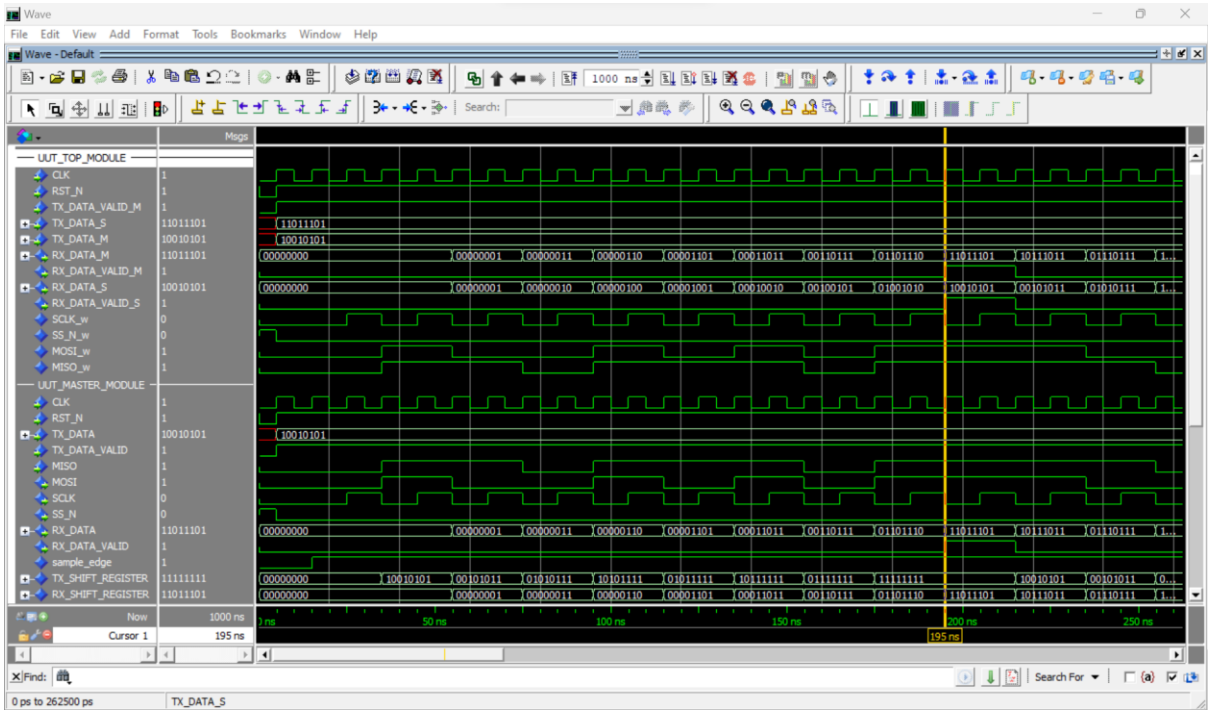
Figure 4.1.1.1 Mode 0 ModelSim Simulation Result – Personal Elaboration

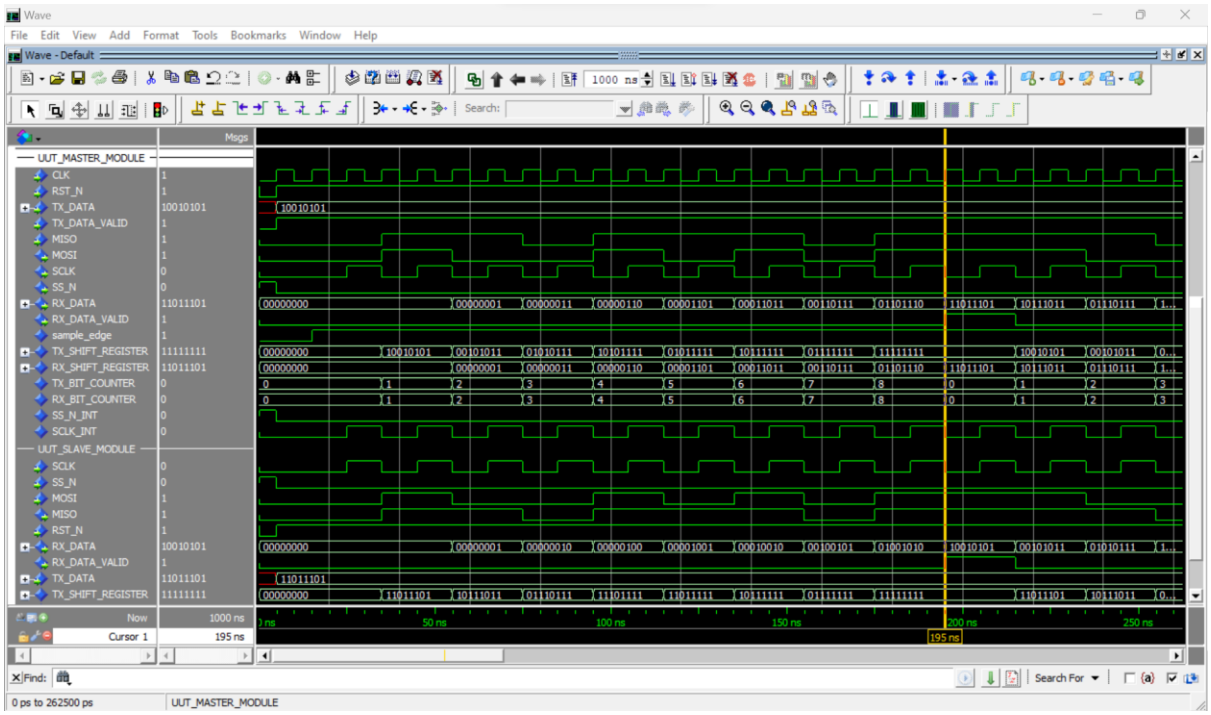
Mode 0:

A Description from an Academic Perspective: Mode 0 in the SPI protocol is defined by the process of capturing data on the rising edge and propagating it on the falling edge of the clock signal. Throughout this mode, the Slave Select (SS_N) signal stays active low, signifying the device's selection.

Observations from the Simulation: The simulation results for Mode 0 align with the theoretical expectations, reflecting a consistent behavior. The data lines demonstrate synchronization with the clock signal, accurately capturing data on the rising edge while keeping SS_N active low for device selection. The strict adherence to the expected timing sequence confirms the precise simulation of Mode 0.

❖ *Mode 1 when we have CPOL and CPHA value are 0 and 1 respectively.*





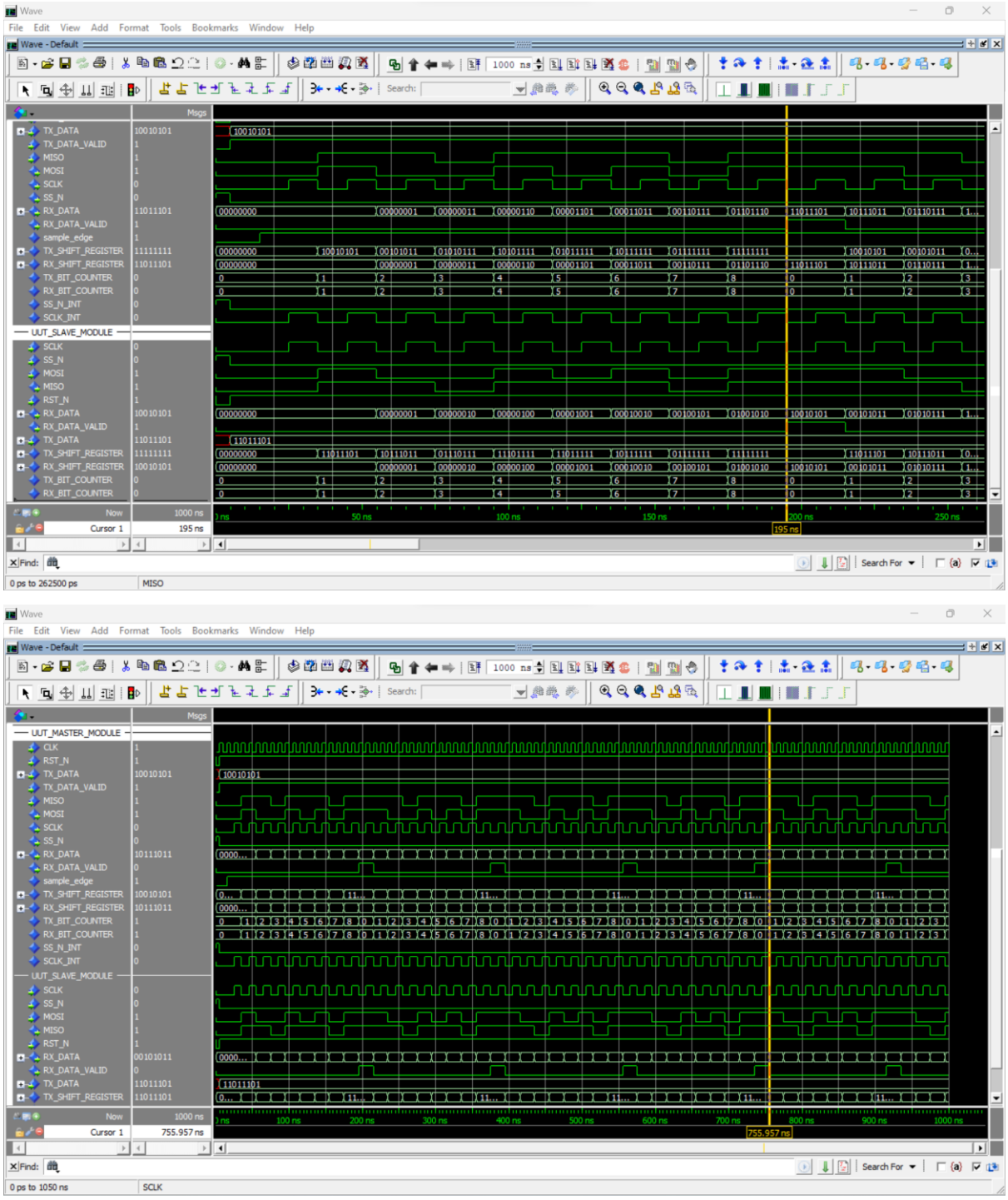


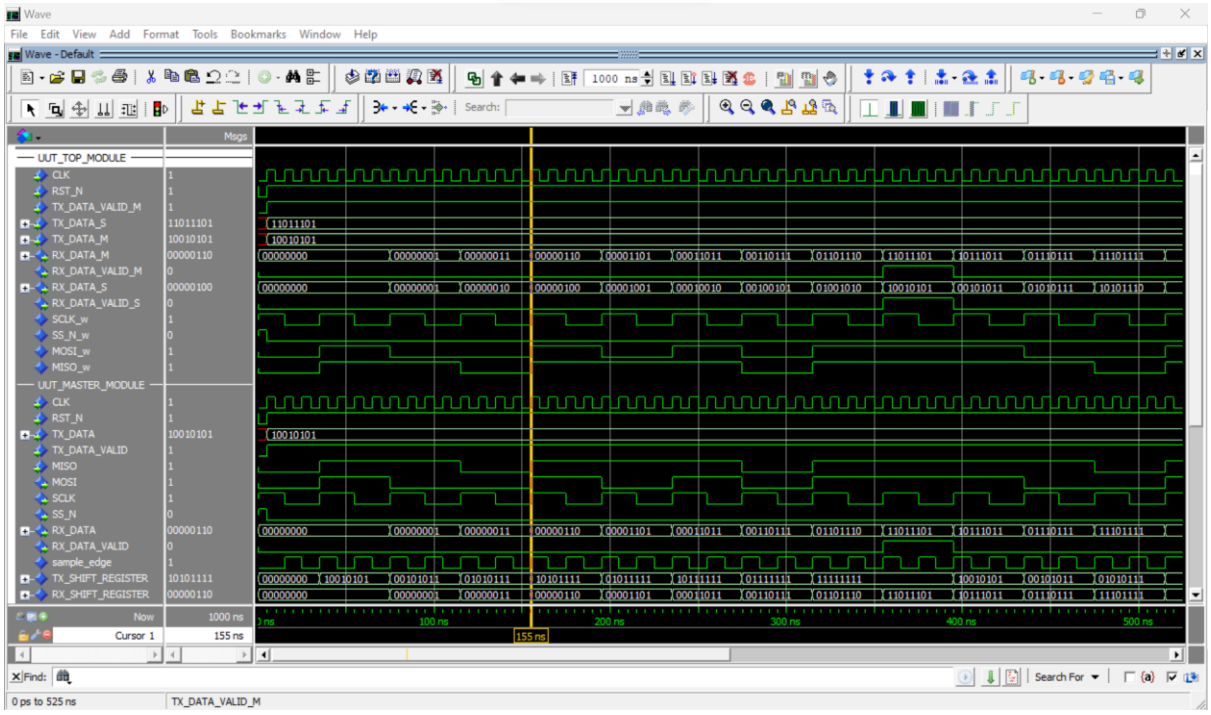
Figure 4.1.1.2 Mode 1 ModelSim Simulation Result – Personal Elaboration

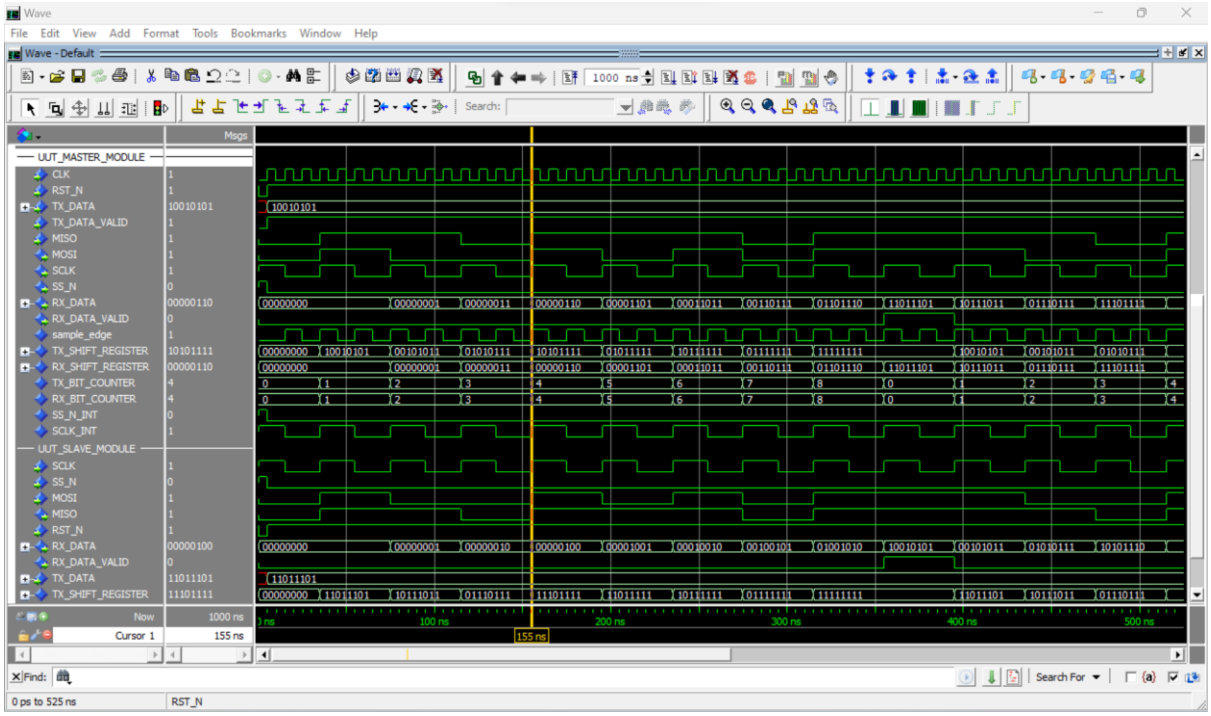
Mode 1:

Theoretical Expectation: One approach entails capturing data when the clock signal falls and transmitting it when the clock signal rises. Just like Mode 0, SS_N stays active low to select the device in this mode.

Simulation Insights: The simulation outcomes closely match the theoretical specifications for Mode 1. The data lines demonstrate the anticipated timing relationship with the clock signal, capturing data on the falling edge while maintaining SS_N active low for device selection. The alignment between theoretical expectations and simulation results confirms the accurate portrayal of Mode 1.

❖ *Mode 2 when we have CPOL and CPHA value are 1 and 0 respectively.*





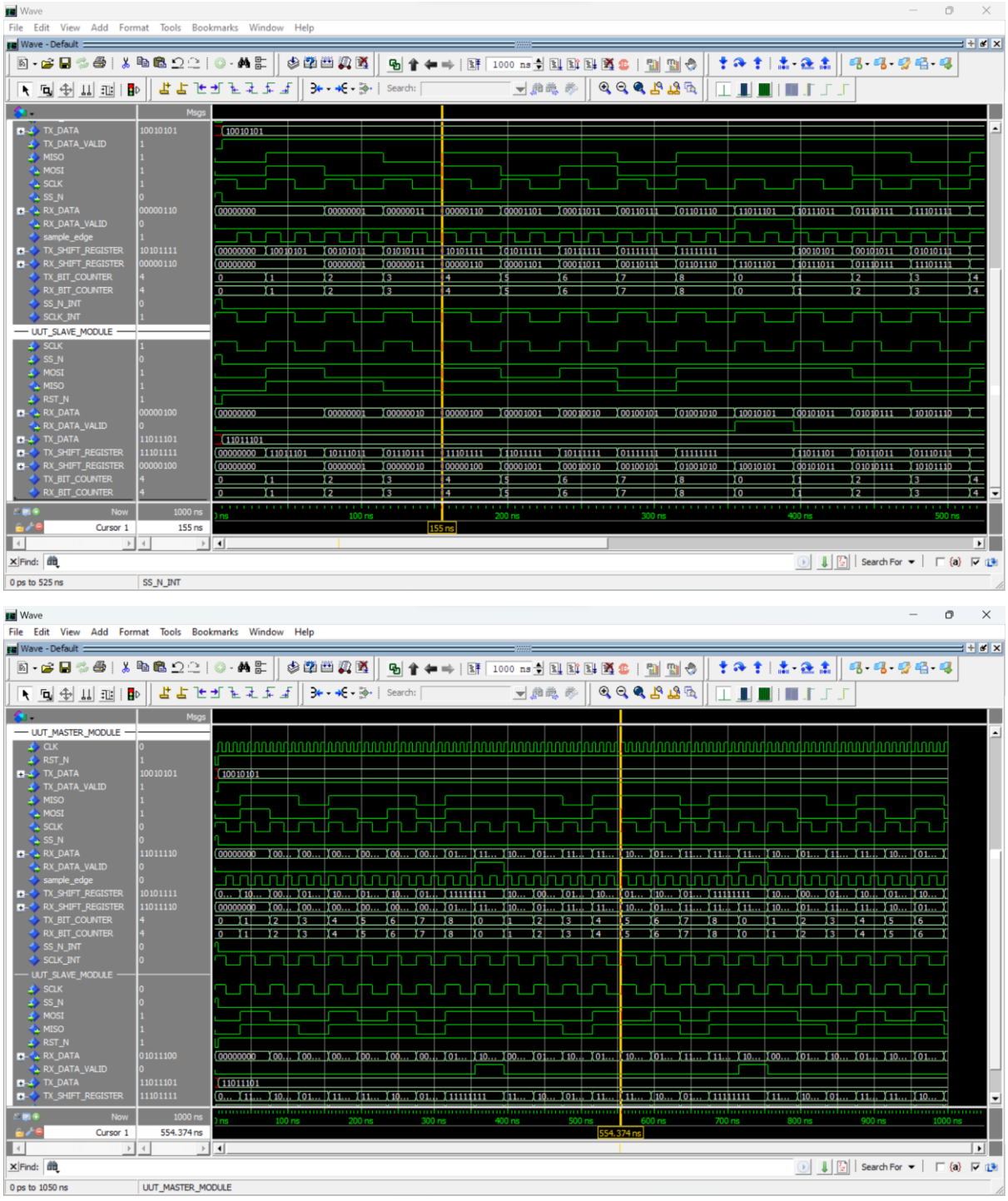


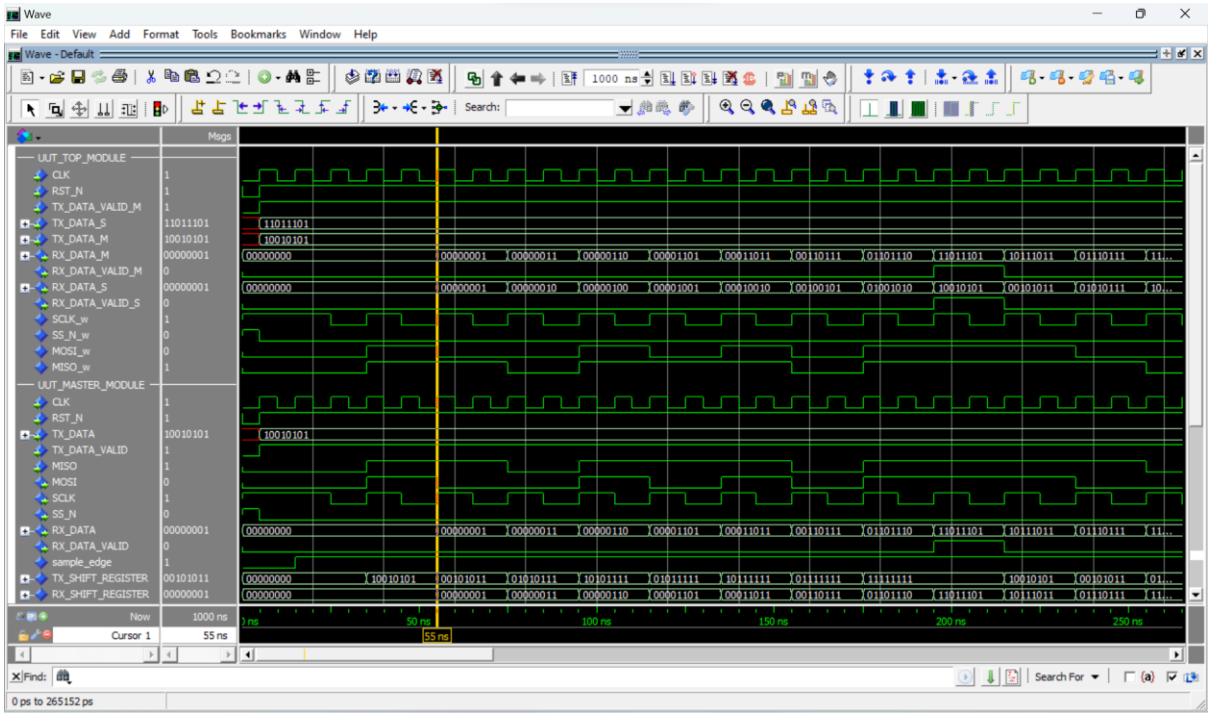
Figure 4.1.1.3 Mode 2 ModelSim Simulation Result – Personal Elaboration

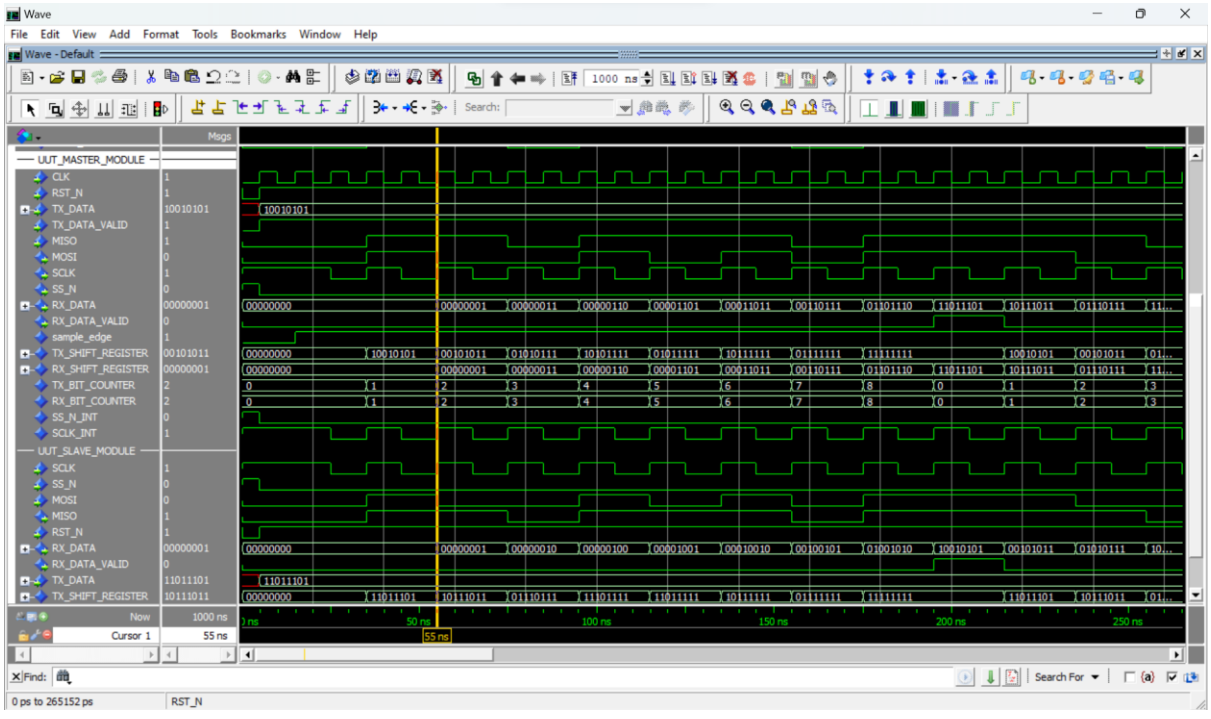
Mode 2:

Theoretical Description: In Mode 2 of the SPI protocol, data is captured when the clock signal rises and then propagated when it falls. Just like other modes, SS_N stays active low while data transactions are taking place.

Simulation Findings: The simulation faithfully reproduces the expected behavior for Mode 2. The data lines exhibit a strong synchronization with the clock signal, ensuring accurate data capture during the rising edge while keeping SS_N active in its low state. The alignment between theoretical predictions and simulation outcomes confirms the accurate emulation of Mode 2.

❖ *Mode 3 when we have CPOL and CPHA value are 1 and 1 respectively.*





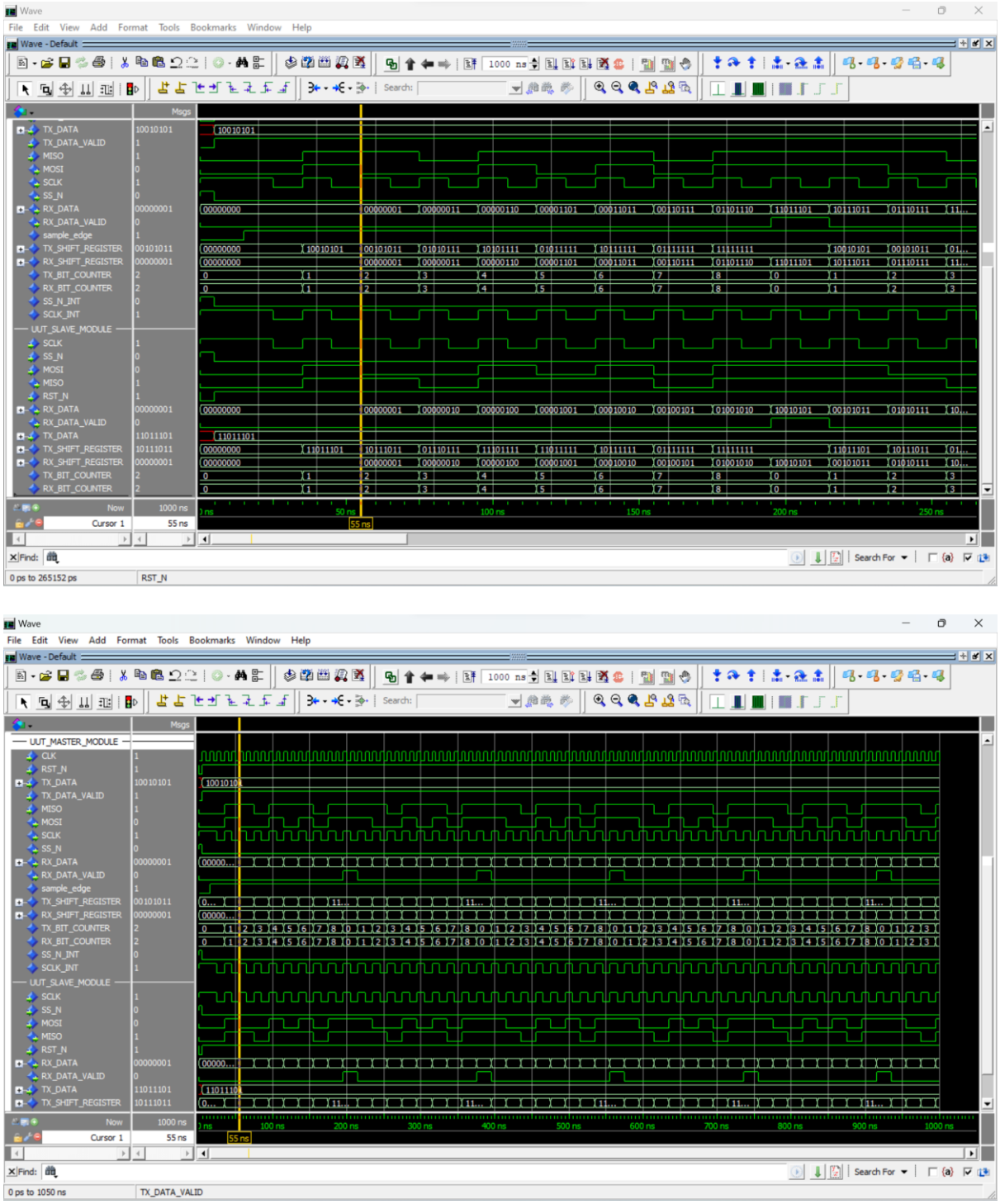


Figure 4.1.1.4 Mode 3 ModelSim Simulation Result – Personal Elaboration

Mode 3:

Expected Behaviour: In Mode 3, data is captured when the clock signal falls, and it is propagated when the clock signal rises. SS_N remains in a state of low activity, ensuring the correct device is selected during data exchange.

Simulation Validation: The simulation results for Mode 3 align perfectly with the theoretical expectations. The data lines are synchronized with the clock signal, ensuring precise data capture when the falling edge occurs, while SS_N remains active low for device selection. The alignment between theoretical specifications and simulation results confirms the precise depiction of Mode 3.

During this simulation, the SPI protocol facilitates the exchange of data between a master and a slave module using MOSI and MISO wires, allowing for simultaneous transmission and reception. Shift registers are utilized to enable the sequential movement of 8-bit data packets during transmission and reception. Precise data transfer is ensured through dedicated bit counters that track both the transmit (TX) and receive (RX) paths.

The master begins communication by loading an 8-bit packet into the transmit shift register. The data is transmitted in a sequential manner to the slave through MOSI, while the slave receives and stores the incoming data through MISO.

Bit counters oversee the progress of data transfer, increasing with each bit that is transmitted or received. Bit synchronization takes place when bits are systematically clocked out and securely stored in shift registers during the transitions of the clock signal.

After finishing, the master and slave exchange 8 bits in both directions. This showcases SPI's fundamental operation, employing shift registers and bit counters to achieve precise and synchronized data exchange among interconnected modules.

Here is the final simulation result for all modes of the SPI protocol. It showcases the different processes I employed to transfer data between the master and slave using MOSI and MISO.

4.2 Quartus Prime Results

Currently, we are exploring the simulation results and the intricate processes involved. Our focus is on discussing captivating design implementation parameters using the Intel Quartus Prime software. This will allow us to verify estimated power consumption, constraints, and timing analysis.

4.2.1 Synthesis and P&R Results

During the synthesis and place-and-route (P&R) phases of the project, the paper utilizes the Cyclone 10 LP Evolution Kit with an external FPGA board. The design configuration involves a strategic interconnection of modules to achieve specific functionalities.

The FPGA board connects with the onboard oscillator through SYS_CLK, creating a crucial link for timing and synchronization within the system. In the FPGA, the JTAG sources are utilized to set up the SPI MASTER module, allowing it to function as the main controller for the SPI communication.

The SPI MASTER module is connected to the SPI Slave module using an external loopback mechanism, establishing a closed communication loop between these components. This loop facilitates the smooth exchange of data between the master and slave, emulating a comprehensive SPI communication from start to finish.

In addition, the SPI Slave module includes an internal feedback loopback feature, which enhances its functionality by enabling self-referential communication checks. This internal loopback mechanism enables the validation and verification of the SPI Slave's functionality, ensuring accurate data transmission and reception within the module itself.

This set of modules creates a cohesive system for evaluating and testing SPI communication on the Cyclone 10 LP Evolution Kit. The design architecture facilitates a meticulous evaluation and validation of the SPI modules' functionality, enabling a comprehensive testing and analysis throughout the synthesis and P&R phases. Take a look at the figure below to see what I accomplished.

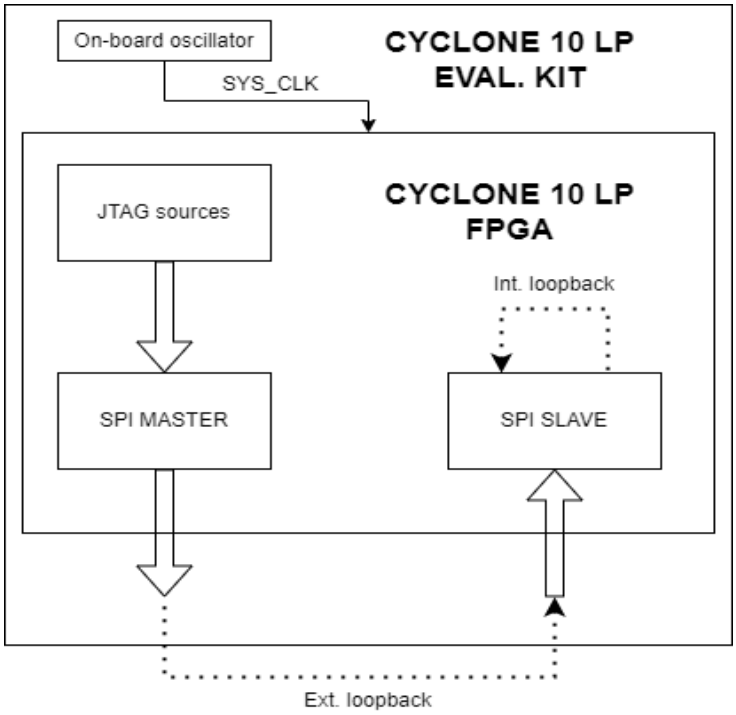


Figure 4.2.1.1 FPGA Architecture for P&R – Personal Elaboration

To facilitate SPI transactions from the master side and pre-load data for transmission as MOSI

and MISO, I began by creating four separate projects for each mode. I then proceeded to review each project individually.

To obtain the Synthesis and P&R results, we need to include our VHDL file in Intel QURTUS Prime. In the next topic board testing, we will explore the process of configuring the JTAG and STP nodes to achieve our SPI transaction in the real world. After incorporating all the necessary elements, I bring together the entire process to achieve the final compilation. Once the project is complete and all components have been successfully compiled, we will be able to access a comprehensive summary of the entire process. This summary will provide us with valuable insights into the utilization of registers, logic components, and other elements in our design.

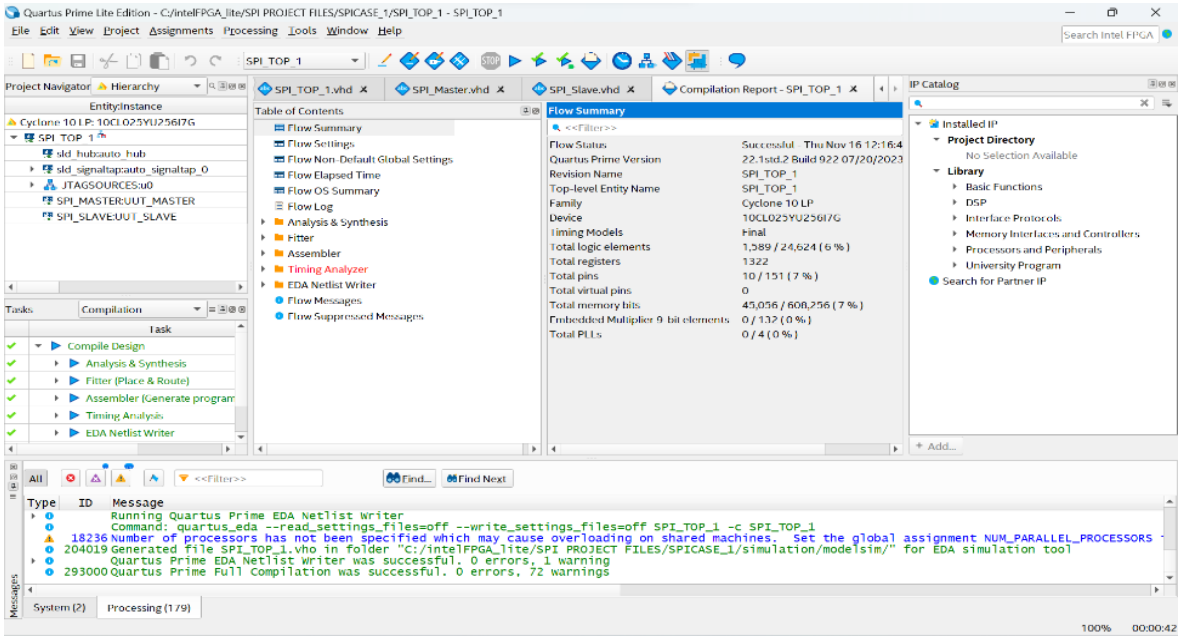


Figure 4.2.1.2 Compilation in Quartus Prime – Personal Elaboration

Here is the figure below, which includes a total of ten pins.

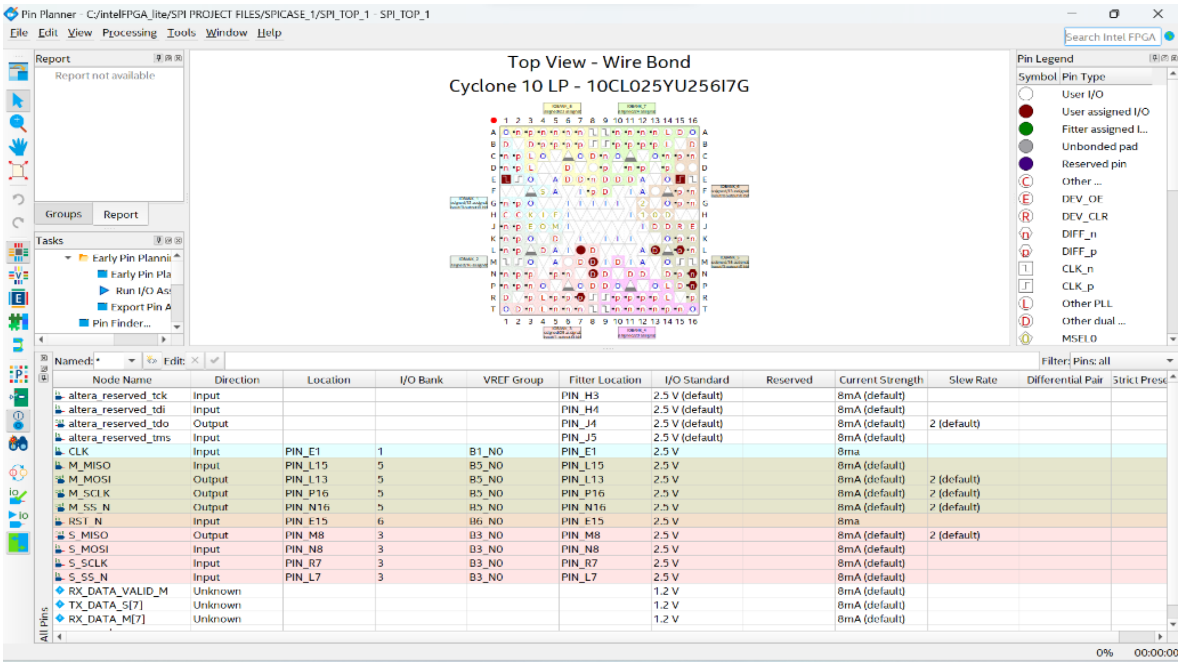


Figure 4.2.1.3 Pin Planner in Quartus Prime – Personal Elaboration

After compiling the data, we are able to generate intricate schematic diagrams that illustrate the synthesis of both the master and slave modules. These diagrams provide a thorough visual representation of the methodologies used in this process, revealing the complexities of our design strategy. In these schematics, we can observe the use of different digital electronics components that represent our VHDL implementation. The architecture and functionality embedded within each module are revealed through elements like shifting registers, distinct control signals, and other essential circuitry. In addition, the diagrams offer valuable insights into the logical elements used, serving as a measure to evaluate and define the overall framework that governs the structure of the protocol. We can obtain the information from the RTL viewer, as shown in the figure below.

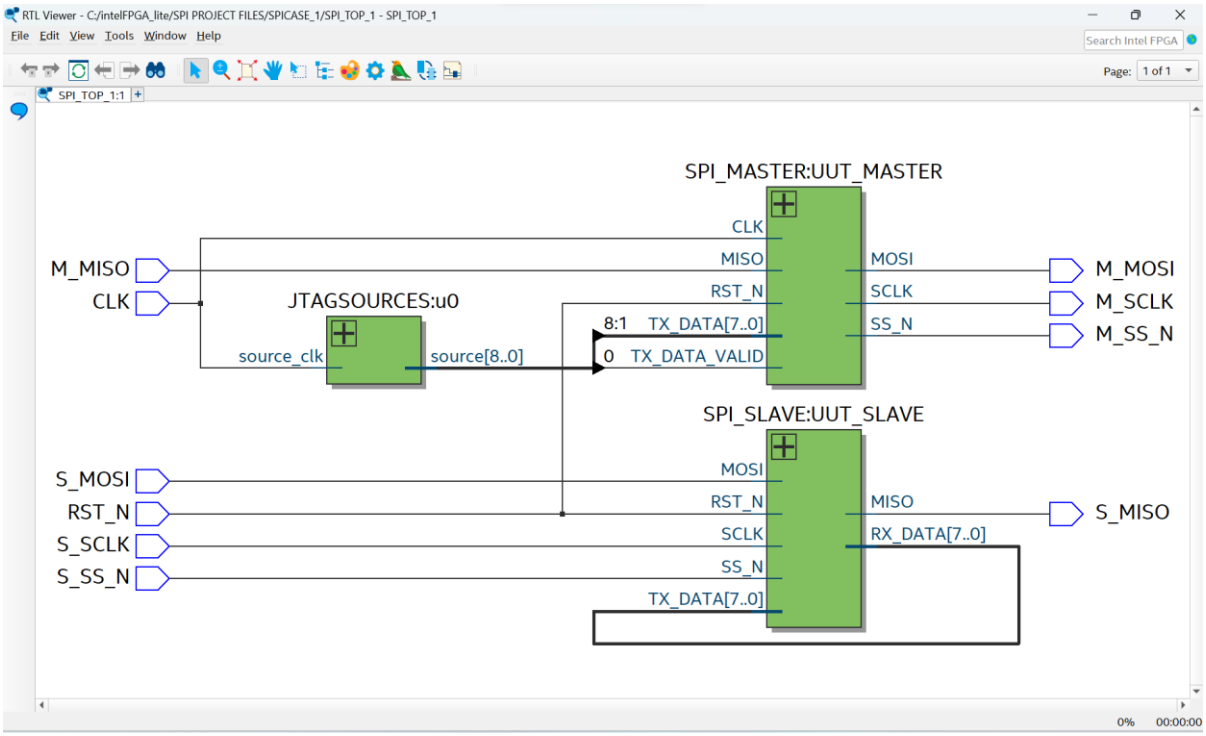
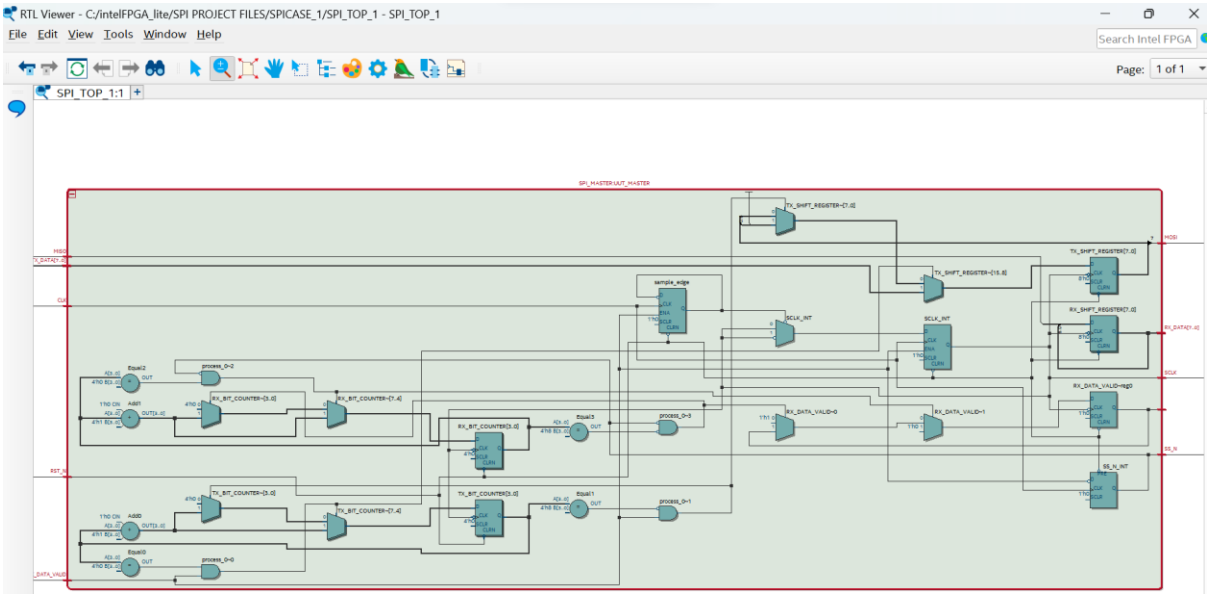


Figure 4.2.1.4 RTL Viewer in Quartus Prime – Personal Elaboration

Let's take a closer look at the digital electronics elements found in both the master and slave modules. These include shifting registers, multiplexers, flip-flops, control signals, and various other components that are crucial for my VHDL implementation. We can explore signal paths within these modules to gain insights into how data flows through various components and how different elements interact. Displayed in the diagram below, a multitude of digital components are utilized to attain our desired master and slave outcomes.



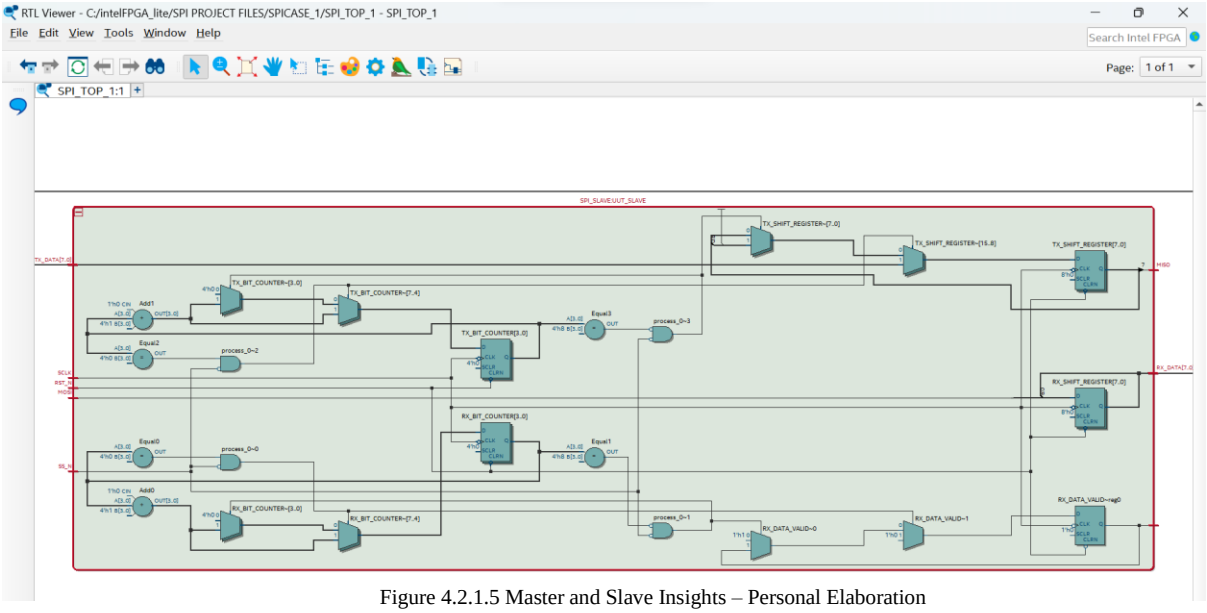


Figure 4.2.1.5 Master and Slave Insights – Personal Elaboration

After examining the master and slave modules within the digital components, we can obtain a comprehensive overview of the memory bits, logic elements, and registers utilized in the processes. This allows us to access the final Synthesis and P&R results summary.

1. Synthesis Results summary

The metrics indicate a well-executed design implementation, showcasing a harmonious blend of logic elements, registers, memory utilization, and pin count. The design's functionality heavily relies on logic elements and registers, as it does not incorporate embedded multipliers and PLLs. The resource allocation is well-suited for the Cyclone 10 LP family, demonstrating an efficient utilization of the available hardware resources for the SPI_TOP_1 project.

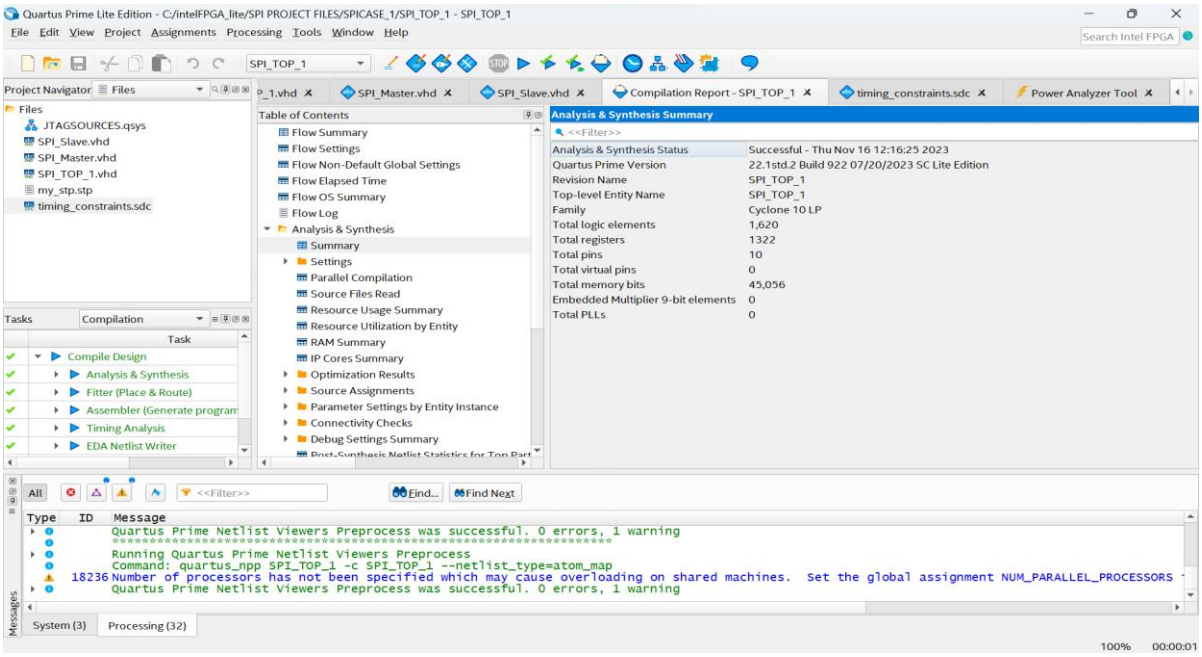


Figure 4.2.1.6 Synthesis Summary – Personal Elaboration

2. Place and Route Results summary

The Place and Route reports and results provide a comprehensive overview of the physical implementation of the design. They include information on placement, routing, timing, resource utilization, and adherence to constraints. Their expertise helps designers enhance the physical layout, maximize resource utilization, meet timing requirements, and successfully implement the digital design in the desired FPGA or ASIC technology.

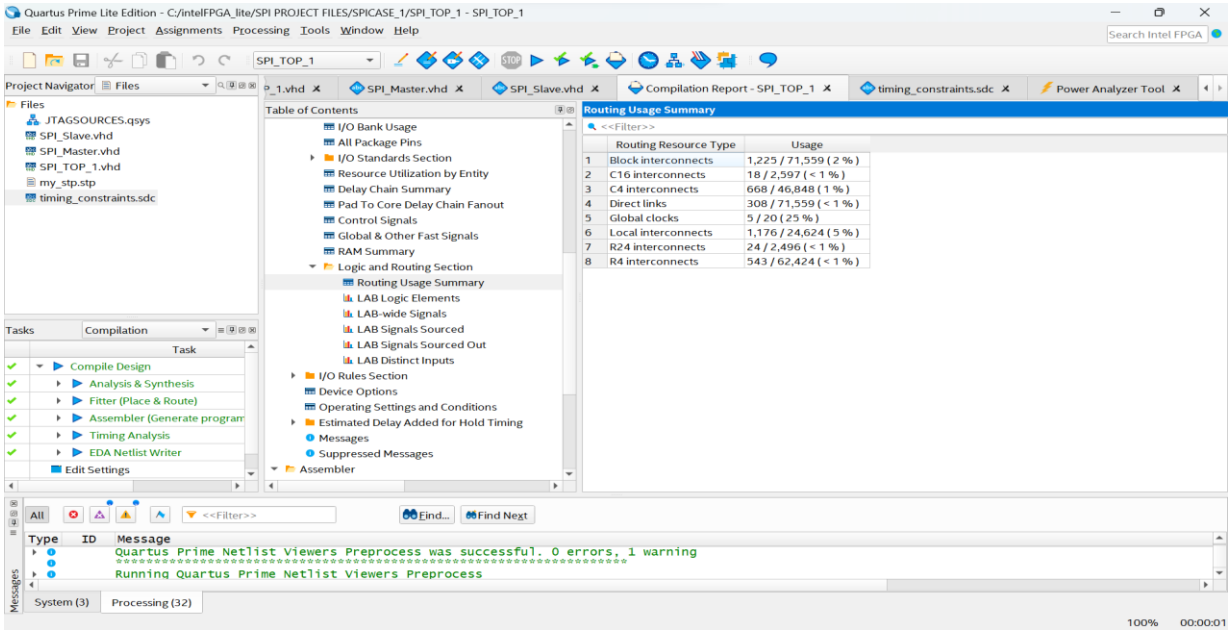


Figure 4.2.1.7 Place and Route Summary – Personal Elaboration

Once we have reviewed the Synthesis and P&R results, we can move forward with analyzing power estimation and timing parameters in our design.

4.2.2 Power consumption, Timing Constraints Analysis Results

During synthesis and place-and-route analysis, power estimation is a crucial step in forecasting the power consumption of a digital design prior to its physical implementation on hardware. Although the precision of these estimations may differ, they offer valuable insights into the power profile of the design and assist in optimizing the design.

❖ *Estimated Power Consumption: -*

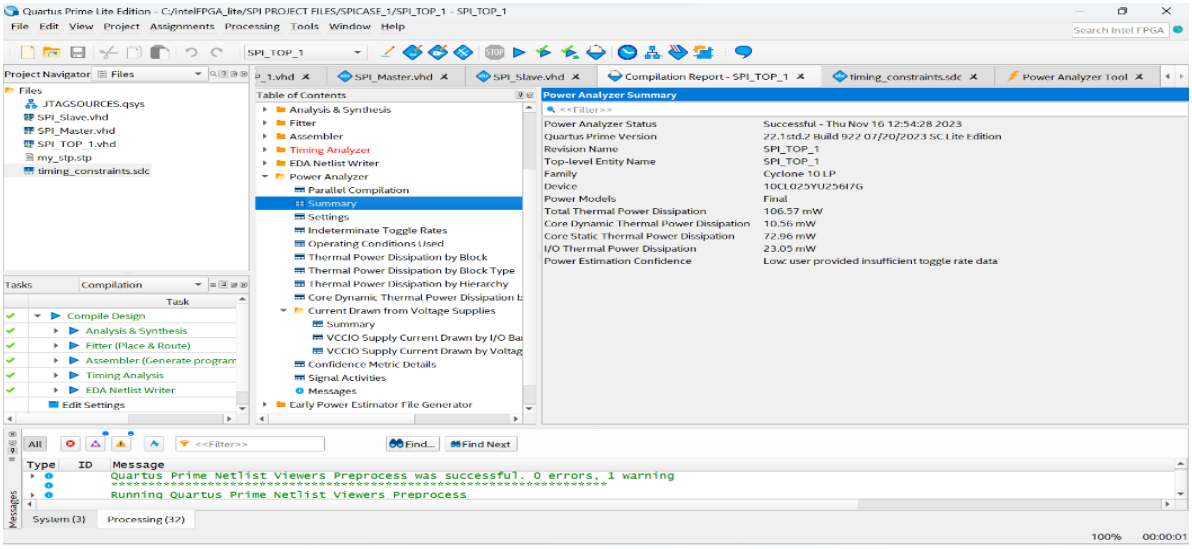


Figure 4.2.2.1 Power Analyzer Summary – Personal Elaboration

❖ *Timing Constraints: -*

During the design process, the Synopsys Design Constraints (SDC) files played a crucial role in establishing the essential timing constraints for the synthesis tool. These SDC files serve as a comprehensive set of instructions that direct the synthesis process by defining various parameters, including clock frequencies, input/output delays, and clock relationships. Through the use of SDC syntax, the synthesis tool was able to effectively optimize the design layout and routing to meet the specified timing requirements. This enabled precise timing analysis and guaranteed that the design functioned within the designated performance limits, essential for ensuring dependable functionality and meeting timing goals. In terms of timing parameters, there are a total of 4 clocks available on the Cyclone 10LP board, each operating at a frequency of 50MHz. As evident in the clock displayed below, it was utilized within our design constraints.

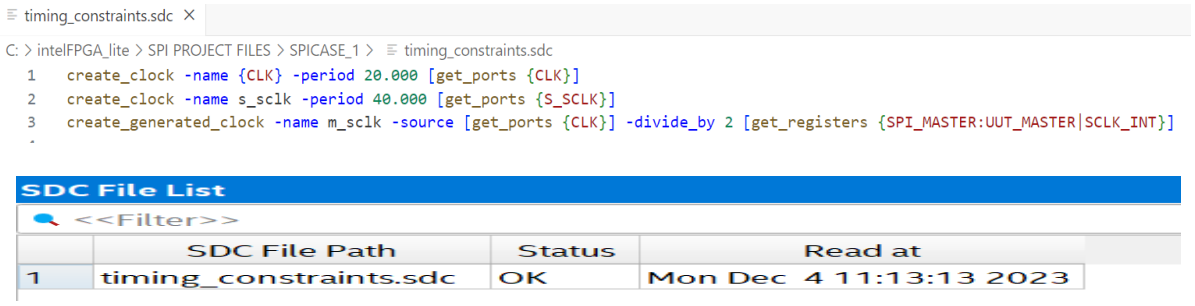


Figure 4.2.2.2 Timing Constraints (SDC) – Personal Elaboration

It is evident that we employ different clock frequencies to operate our master and slave modules. However, it is important to note that the maximum attainable frequency exceeds the

one you have specified, primarily due to design limitations. The observed difference between the specified clock frequencies and the actual restricted clock frequencies, as shown in the figures below, can be explained by various factors. These include the impact of advanced optimization algorithms and the variations in Process, Voltage, and Temperature (PVT). Process: Each chip is unique and distinct from the others. Within a specific FPGA speed grade, there will be variations in chip performance. The speed of the chip can be influenced by the voltage it receives. Increasing the Vcc can result in a faster chip, while decreasing the Vcc can lead to a slower chip. Temperature has a significant impact on the performance of chips. Lower temperatures can make the chips operate faster, while higher temperatures can cause them to slow down. It's important to note that -40°C is equivalent to -40ºC, and 100°C is equivalent to 100 ºC. These folders labelled 'slow', 'slow', and 'fast' can be located in the timing analysis section of Quartus Prime.

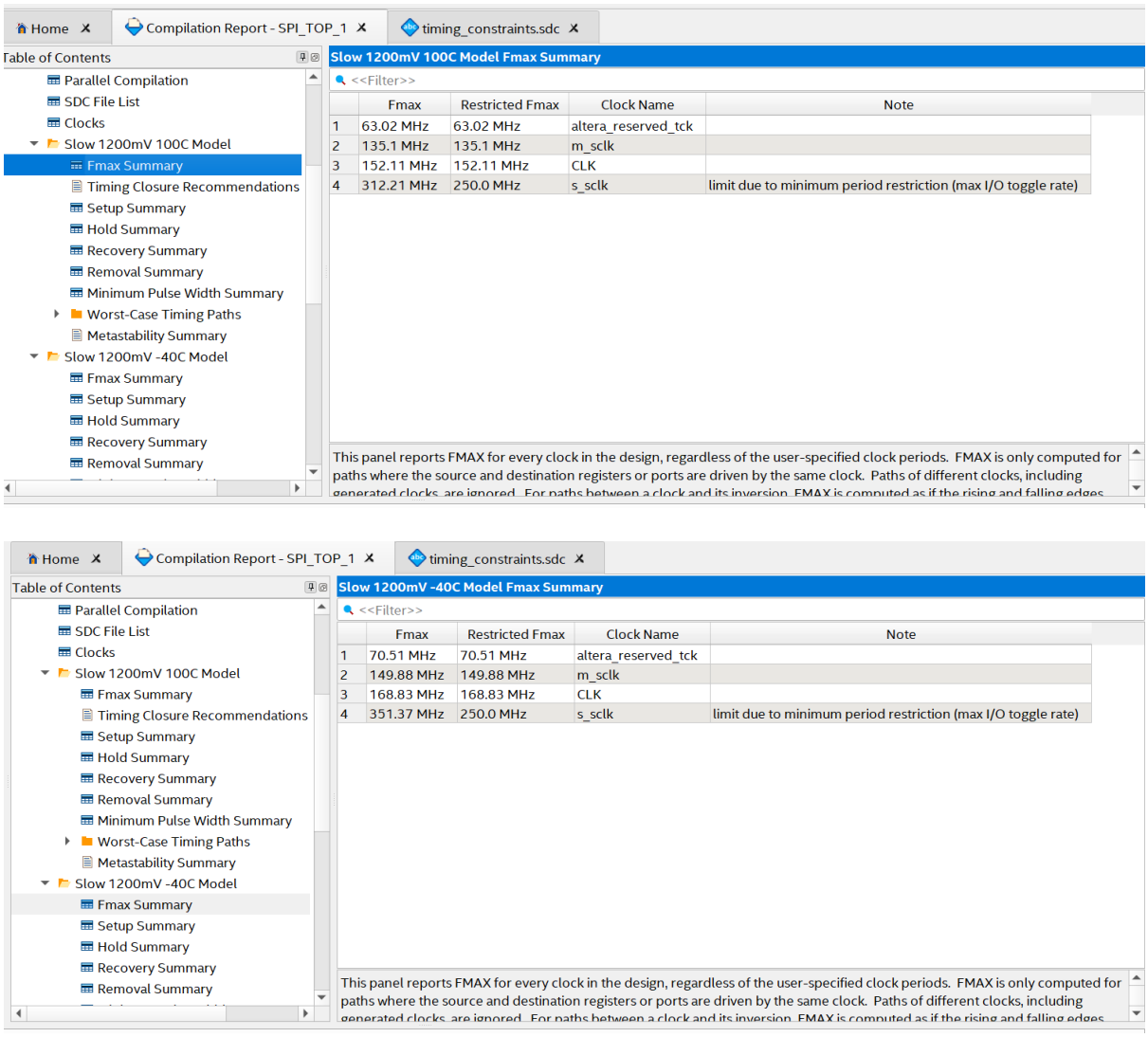


Figure 4.2.2.3 Fmax summary – Personal Elaboration

This panel provides information on FMAX for each clock in the design, regardless of the user's specified clock periods. FMAX is calculated exclusively for paths in which the source and destination registers or ports are driven by the same clock. Paths of various clocks, including clocks that are generated, are disregarded. When calculating FMAX for paths between a clock and its inversion, the scaling of rising and falling edges is taken into account. This ensures that the duty cycle is maintained, expressed as a percentage. When the temperature reaches 100°C or higher, the chip's performance is reduced. When exposed to extremely low temperatures, such as -40°C or below, the chip experiences a further decrease in its speed. This alteration demonstrates an understanding that higher temperatures generally impede the performance of chips, whereas lower temperatures still contribute to this slowdown. This stands in contrast to the previous claim that implied lower temperatures can improve chip speed. It is essential to consistently utilize clock constraints and other slack reports for sign-off analysis.

Now we need to assess if there are any unauthorized clocks accessible along the unrestricted path to ensure the safety of our design in terms of timing parameters.

Unconstrained Paths Summary

<<Filter>>

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	6	6
4	Unconstrained Input Port Paths	148	148
5	Unconstrained Output Ports	5	5
6	Unconstrained Output Port Paths	5	5

Clock Status Summary

<<Filter>>

	Target	Clock	Type	Status
1	CLK	CLK	Base	Constrained
2	SPI_MASTER:UUT_MASTER|SCLK_INT	m_sclk	Ge...ed	Constrained
3	S_SCLK	s_sclk	Base	Constrained
4	altera_reserved_tck	altera_reserved_tck	Base	Constrained

Figure 4.2.2.4 Unconstrained clock and summary – Personal Elaboration

From the above figure, it is evident that our design incorporates tightly constrained clocks, with no illegal clocks present. In addition, with our efficient design process, there is no need to concern ourselves with setting up extra timing parameters or performing hold time analysis.

4.3 FPGA Board Testing

Now, we can proceed with on-board testing to verify that our design aligns with the outcomes of our simulation. This will be done after thoroughly understanding and reviewing all the stages of ModelSim and design implementation. In order to tackle this matter, we have opted for the utilization of an FPGA board known as the Cyclone 10LP (10CL025YU256I7G).

4.3.1 Design Prototype on FPGA

After covering the previous chapter, we have a good understanding of the JTAG and STP logic analysers' features. Now, our task is to customize and adjust them according to our specific needs. Our design requires the initial assignment of the JTAG probe and STP node. Following

that, it is necessary to carry out onboard testing to evaluate the accuracy of the Signal Tap Analyzer in replicating real-world situations. With Quartus Prime, all the necessary pin configurations and design parameters have been established. The only remaining task is to make a few adjustments to the code in order to ensure accurate data transmission between the master and the slave. To achieve the desired outcomes, it is essential to configure the FPGA board accordingly.

The diagram illustrates the interconnection of the four wires on the FPGA board.

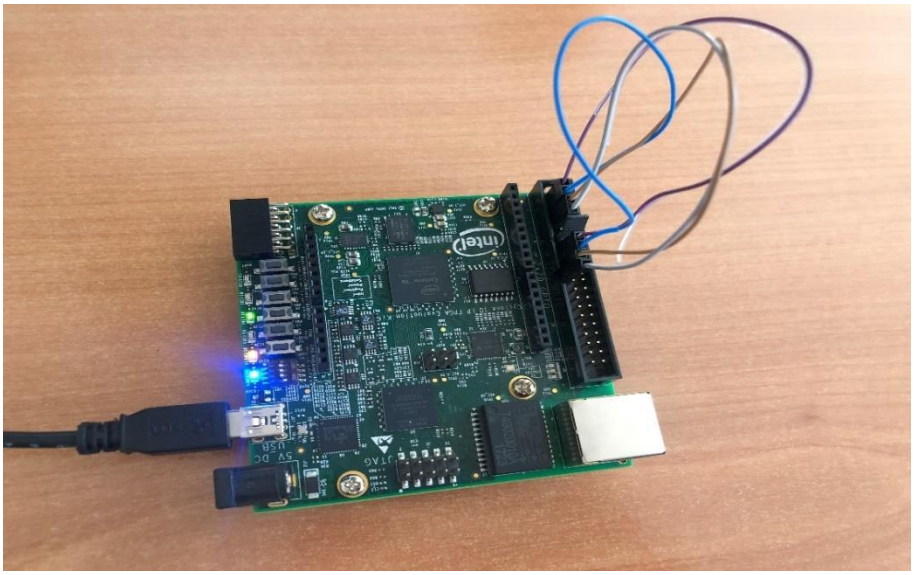
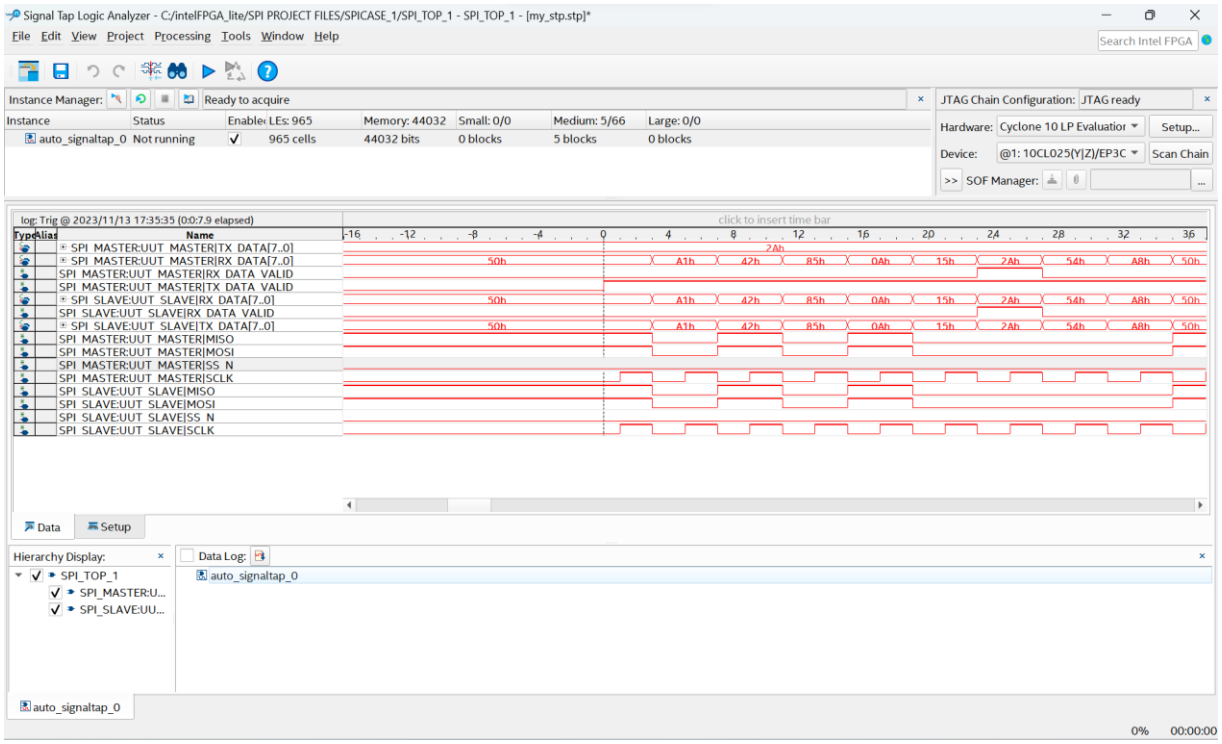
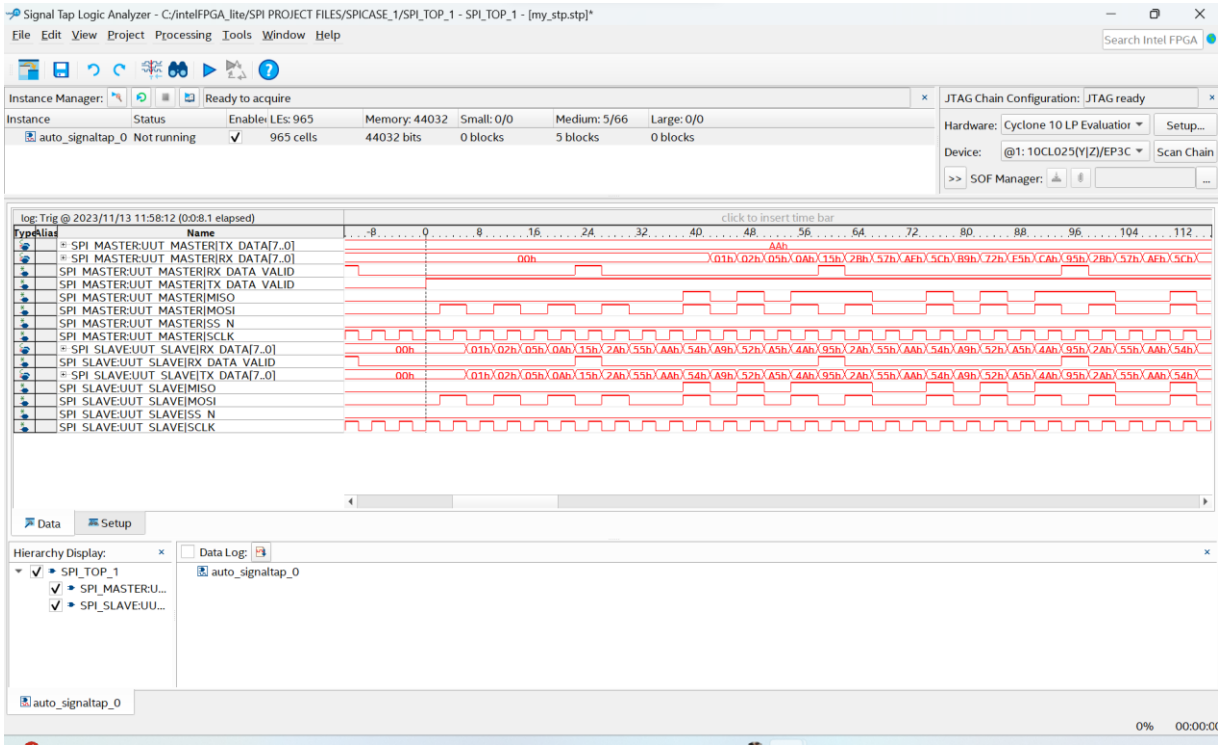


Figure 4.3.1.1 Wire Connection on FPGA – Personal Elaboration

Here is a sample of debugging design with on-board test results.


Signal Tap Logic Analyzer - C:/intelFPGA_lite/SPI PROJECT FILES/SPICASE_1/SPI_TOP_1 - SPI_TOP_1 - [my_stp.stp]*
File Edit View Project Processing Tools Window Help
Search Intel FPGA
Instance Manager: Ready to acquire
Instance Status Enable LEs: 965 Memory: 44032 Small: 0/0 Medium: 5/66 Large: 0/0
auto_signaltap_0 Not running 965 cells 44032 bits 0 blocks 5 blocks 0 blocks
JTAG Chain Configuration: JTAG ready
Hardware: Cyclone 10 LP Evaluation
Device: @1: 10CL025(Y|Z)/EP3C
Setup...
Scan Chain
SOF Manager:
log: Trig @ 2023/11/13 17:35:35 (0:0:7.9 elapsed)
click to insert time bar
Type Alias Name
SPI_MASTER:UUT_MASTER|TX_DATA[7..0]
SPI_MASTER:UUT_MASTER|RX_DATA[7..0]
SPI_MASTER:UUT_MASTER|RX_DATA_VALID
SPI_MASTER:UUT_MASTER|TX_DATA_VALID
SPI_SLAVE:UUT_SLAVE|RX_DATA[7..0]
SPI_SLAVE:UUT_SLAVE|RX_DATA_VALID
SPI_SLAVE:UUT_SLAVE|TX_DATA[7..0]
SPI_MASTER:UUT_MASTER|MISO
SPI_MASTER:UUT_MASTER|MOSI
SPI_MASTER:UUT_MASTER|SS_N
SPI_MASTER:UUT_MASTER|SCLK
SPI_SLAVE:UUT_SLAVE|MISO
SPI_SLAVE:UUT_SLAVE|MOSI
SPI_SLAVE:UUT_SLAVE|SS_N
SPI_SLAVE:UUT_SLAVE|SCLK
Data
Setup
Hierarchy Display:
Data Log:
SPI_TOP_1
SPI_MASTER:U...
SPI_SLAVE:UU...
auto_signaltap_0
0%
00:00:00


Signal Tap Logic Analyzer - C:/intelFPGA_lite/SPI PROJECT FILES/SPICASE_1/SPI_TOP_1 - SPI_TOP_1 - [my_stp.stp]*
File Edit View Project Processing Tools Window Help
Search Intel FPGA
Instance Manager: Ready to acquire
Instance Status Enable LEs: 965 Memory: 44032 Small: 0/0 Medium: 5/66 Large: 0/0
auto_signaltap_0 Not running 965 cells 44032 bits 0 blocks 5 blocks 0 blocks
JTAG Chain Configuration: JTAG ready
Hardware: Cyclone 10 LP Evaluation
Device: @1: 10CL025(Y|Z)/EP3C
Setup...
Scan Chain
SOF Manager:
log: Trig @ 2023/11/13 11:58:12 (0:0:8.1 elapsed)
click to insert time bar
Type Alias Name
SPI_MASTER:UUT_MASTER|TX_DATA[7..0]
SPI_MASTER:UUT_MASTER|RX_DATA[7..0]
SPI_MASTER:UUT_MASTER|RX_DATA_VALID
SPI_MASTER:UUT_MASTER|TX_DATA_VALID
SPI_MASTER:UUT_MASTER|MISO
SPI_MASTER:UUT_MASTER|MOSI
SPI_MASTER:UUT_MASTER|SS_N
SPI_MASTER:UUT_MASTER|SCLK
SPI_SLAVE:UUT_SLAVE|RX_DATA[7..0]
SPI_SLAVE:UUT_SLAVE|RX_DATA_VALID
SPI_SLAVE:UUT_SLAVE|TX_DATA[7..0]
SPI_SLAVE:UUT_SLAVE|MISO
SPI_SLAVE:UUT_SLAVE|MOSI
SPI_SLAVE:UUT_SLAVE|SS_N
SPI_SLAVE:UUT_SLAVE|SCLK
Data
Setup
Hierarchy Display:
Data Log:
SPI_TOP_1
SPI_MASTER:U...
SPI_SLAVE:UU...
auto_signaltap_0
0%

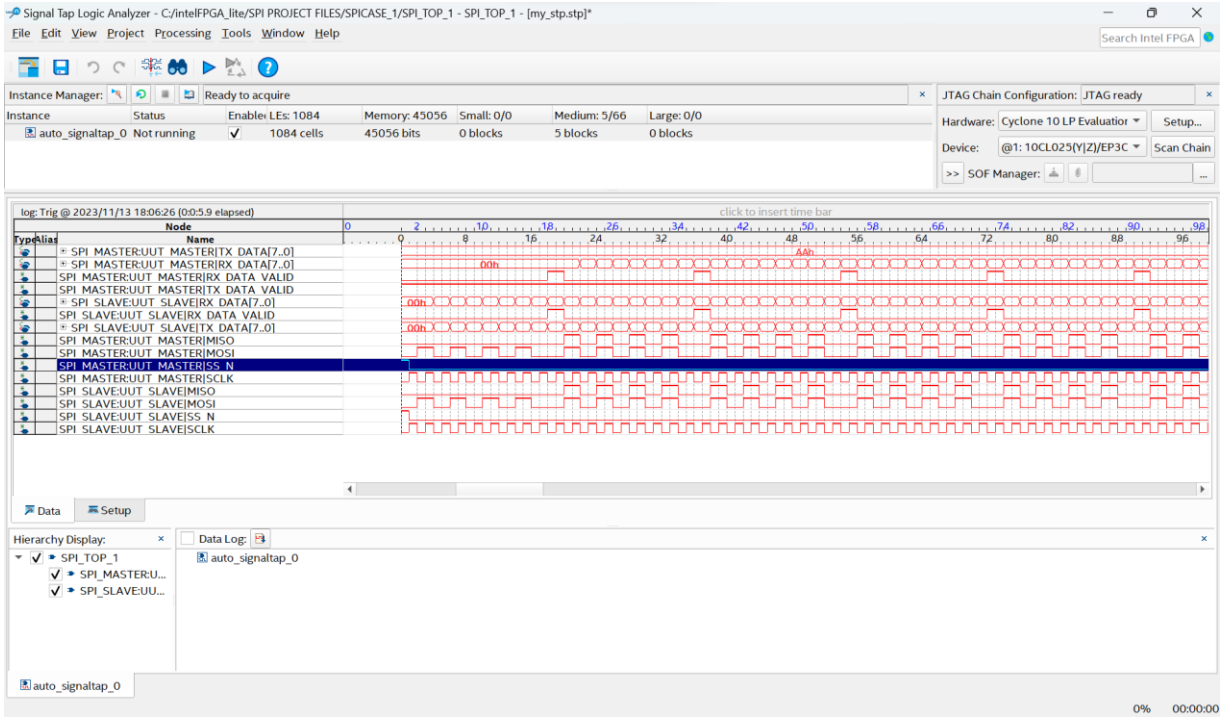


Figure 4.3.1.2 Debugging Results using Signal Tap logic Analyzer – Personal Elaboration

As depicted in the first figure, certain signals exhibit malfunctioning behaviour in the real world, whereas in the ModelSim simulation, they demonstrate flawless functionality. Therefore, it will be necessary to debug our code in order to achieve the desired outcomes.

After some code debugging, we can determine the final expected behaviour of the SPI protocol during the on-board FPGA chip test.

4.3.2 Verify the results through Oscilloscope

In the course of the last section of this paper, the installation of oscilloscope testing is critical. This tool is essential in academic and creative fields, illustrating the fluctuations in voltage graphically as time progresses. The main purpose of this is to capture and analyse electrical signals by plotting waveforms. This allows for a deeper understanding of signal behaviour, frequency analysis, and transient phenomena.

For this purpose, we will require the utilization of a Siglent SDS6104A digital storage oscilloscope. The Siglent SDS6104A is a cutting-edge digital storage oscilloscope known for its accuracy and versatility in analysing signals across a broad frequency range, with an impressive 1GHz bandwidth. This instrument is widely recognized for its impressive capabilities, including a high sampling rate, large memory depth, and a user-friendly display that allows for detailed waveform analysis. With its impressive 1GHz bandwidth, this tool is a

must-have in industries such as telecommunications, research and development, and electronics manufacturing. It excels at capturing intricate electronic signals with precision and speed. This oscilloscope is designed to provide professionals with an intuitive interface and powerful functionalities. It enables efficient diagnosis, troubleshooting, and validation of complex electronic systems, ensuring optimal performance and reliability. The Siglent SDS6104A is a cutting-edge digital oscilloscope that delivers exceptional precision and functionality, making it ideal for complex engineering tasks.

Figure 4.3.2.1 Siglent SDS6104A Oscilloscope

Before we can proceed with the four SPI modes tests on the oscilloscope, it is necessary to configure all the required settings.

❖ *Experimental Setup:*

1. Hardware Configuration:

Utilize the Cyclone 10 LP 10CL025YU256I7G FPGA board equipped with the necessary connections for SPI communication. Ensure the board has dedicated pins or connectors mapped for SPI signals—Serial Clock (SCLK), Master Out Slave In (MOSI), Master In Slave Out (MISO), and Chip Select (CS).

2. Oscilloscope Connection: Connect the oscilloscope to the FPGA board

Probe Connections: Use oscilloscope probes to connect to the SPI signal pins (SCLK, MOSI,

MISO, CS) on the FPGA board.

3. Ground Reference: Connect the oscilloscope ground probe to the FPGA board's ground to establish a common reference.

The diagram below shows how we can connect the oscilloscope probe to our FPGA board for safety and to avoid noise in the system.

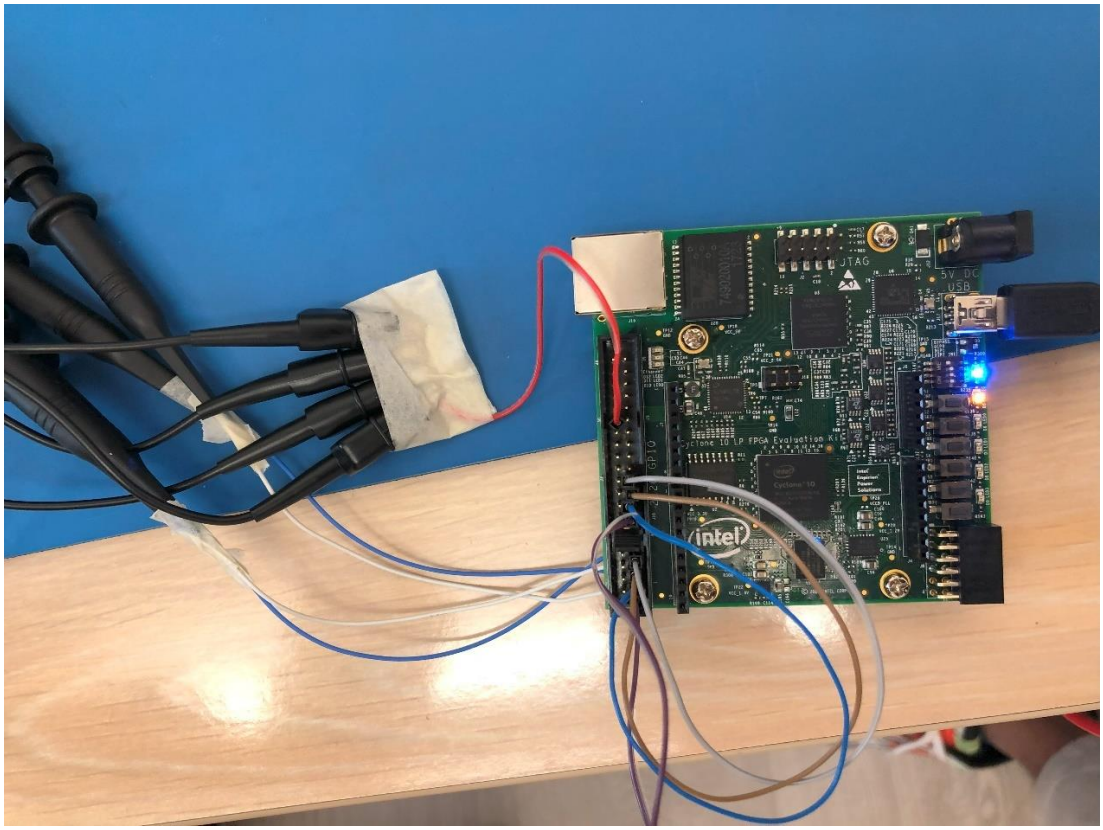


Figure 4.3.2.2 Oscilloscope to FPGA Connection

❖ *Test Scenarios:*

1. Clock and Data Signals Verification

Monitor SCLK and MOSI signals on the oscilloscope to verify the clock's frequency, duty cycle, and data transmission on the MOSI line. Ensure the SCLK frequency matches the expected SPI clock rate configured in the FPGA.

2. MISO Line and Chip Select Verification:

Observe the MISO signal behaviour when the FPGA initiates communication (CS is asserted). Check the logic levels and data transmission on the MISO line when the FPGA is in both active and inactive states (CS high and low).

❖ *Test Execution and Observations:*

Test Procedures:

1. FPGA Configuration: Load the FPGA with the SPI communication design.

2. Oscilloscope Setup: Configure the oscilloscope to display and capture the SPI signal waveforms for analysis.

3. Test Execution: Initiate SPI communication routines in the FPGA, performing read and write operations to SPI-connected devices.

4.Signal Capture: Use the oscilloscope to capture and analyse SCLK, MOSI, MISO, and CS waveforms during the communication sequences.

❖ *Observations:*

1. Clock Timing: Validate the clock frequency, duty cycle, and integrity of SCLK for proper synchronization.

2. Data Transmission: Verify accurate data transmission on the MOSI and MISO lines, ensuring data integrity.

3. Chip Select Functionality: Confirm the proper assertion and de-assertion of the CS line during communication transactions.

The figures below show the oscilloscope results for all modes of SPI communication.

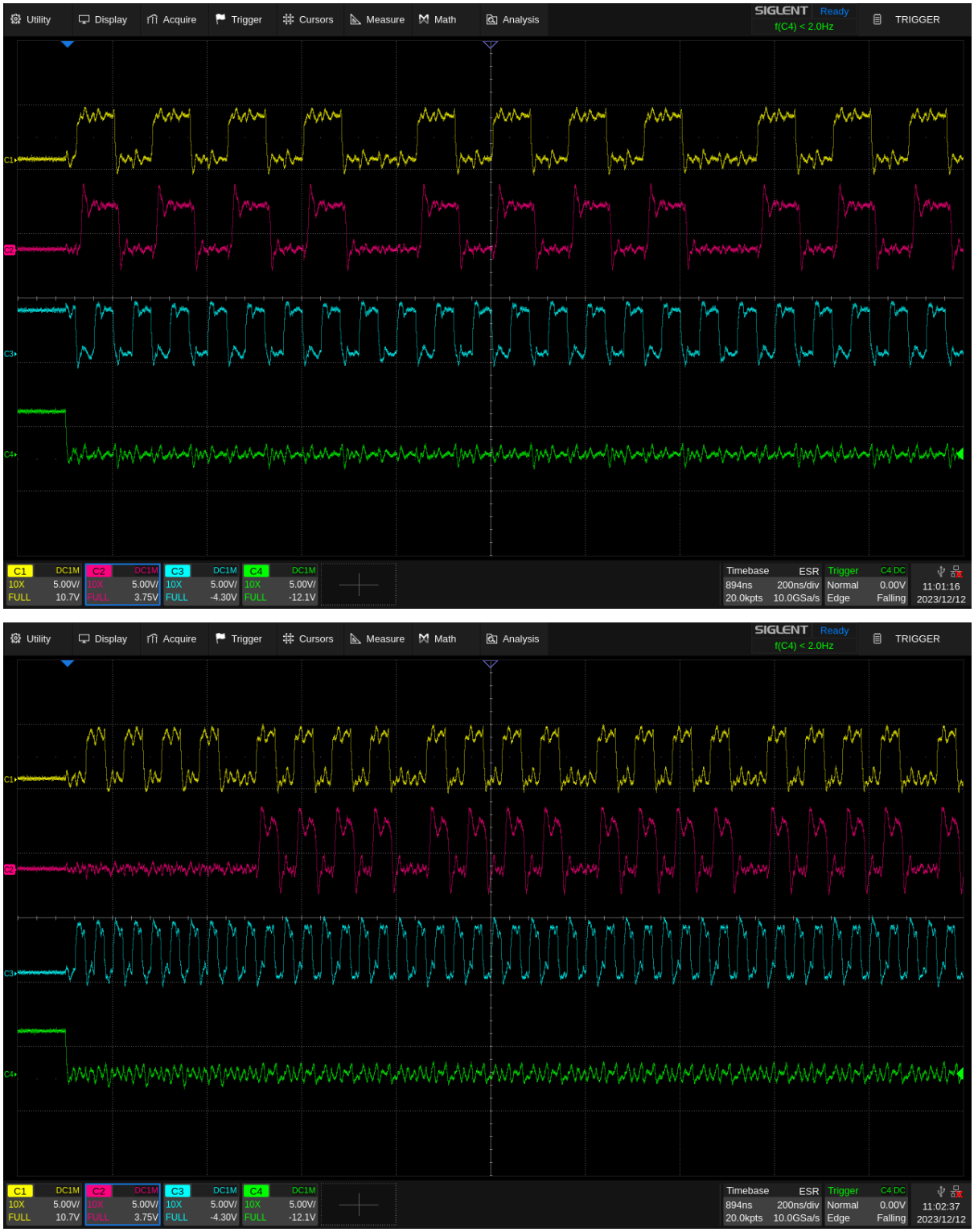


Figure 4.3.2.3 Oscilloscope Results of Modes (0,1) – Personal Elaboration

Figure 4.3.2.4 Oscilloscope Results of Modes (2,3) – Personal Elaboration

The oscilloscope acquisition pictures highlight the SPI protocol signals, with each signal clearly identified for improved readability and comprehension.

1. MISO (Master Input, Slave Output): Illustrating the flow of data from the slave to the master, the MISO signal showcases a vivid yellow trace that represents the path of the

response from the slave device to the master. This trace encapsulates the transmission of data from the slave to the master.

2. MOSI (Master Output, Slave Input): The MOSI signal transmits information from the master to the slave device. The vibrant pink hue beautifully showcases the path of data as it originates from the master device and makes its way to the designated slave device.
3. SCLK (Serial Clock): This signal is a crucial component in ensuring the smooth and efficient transmission of data. The rhythmic oscillation captured in a striking blue waveform embodies the synchronization heartbeat of the SPI protocol. This signal coordinates the exact timing of data bits being transmitted between devices.
4. SS/CS (Slave Select/Chip Select): This signal indicates the chosen slave device for communication. Furthermore, this fundamental indicator, displayed prominently in green, signifies the initiation of a particular device for the transfer of information. The significance of its position at the base lies in its crucial role in initiating communication.

The evident patterns, carefully coordinated, tell the story of the SPI communication sequence when transmitting single-byte data. Using color-coded labelling not only improves the visual appeal, but also adds educational value by providing clear information about the roles and timing relationships among essential SPI signals.

The objective of the experiment is to validate SPI communication by analysing waveform characteristics using the Cyclone 10 LP 10CL025YU256I7G FPGA board and oscilloscope. This configuration allows for live monitoring of SPI signals, ensuring compliance with protocol specifications and detecting any irregularities in signal behaviour during data transmission. The observations and measurements obtained from the oscilloscope offer valuable insights into the functionality and accuracy of the FPGA's SPI communication implementation.

The chapter Results and Board Testing follows a well-organized design flow with the goal of validating the SPI protocol. Starting with ModelSim, simulation results provide a virtual comprehension of protocol functionality. Afterwards, the Quartus Prime software carefully analyses and verifies the FPGA chip, ensuring that the design is sound and compatible. At last, the SPI protocol's practical adherence is confirmed through real-world verification using an oscilloscope. This systematic approach guarantees a thorough assessment, beginning with insights from simulations, advancing to validation on FPGA chips, and concluding with real-world confirmation. This rigorous process ensures that the protocol is effective and reliable in all stages, including simulation, digital implementation, and practical application.

Conclusions

This paper delves into a thorough examination of four important chapters. It explores the Serial Peripheral Interface (SPI) protocol, the architecture of Field-Programmable Gate Arrays (FPGAs), the intricate design and implementation process using VHDL, and empirical testing to validate functionality. Chapter 1 provided a comprehensive exploration of the operational intricacies and significance of the SPI protocol, laying a strong foundation for further study. Chapter 2 thoroughly explored FPGA architecture and highlighted its crucial role in enabling intricate digital systems. Chapter 3 provided a thorough explanation of the VHDL implementation process, offering valuable insights into the development and utilization of an SPI module within the FPGA. The empirical findings, showcased in Chapter 4, confirmed the effectiveness and productivity of the implemented SPI module.

The results obtained from the implemented FPGA-based 4-wire interface project demonstrate its versatility and effectiveness in enabling smooth data acquisition and generation processes. The interface's impressive versatility accommodates a wide range of operational modes, including ADC/DAC serial interfaces and connections to I/O expanders and serial communication-enabled memories. The robust performance evaluations confirm its dependability and adaptability across a wide range of applications, showcasing its potential usefulness in situations that require flexible and effective data exchange mechanisms.

Anticipating the future, the path of this FPGA-based 4-wire interface paves the way for potential progress. Possible advancements may involve improving compatibility with various communication protocols, strengthening security measures to safeguard data integrity, and optimizing performance metrics for faster speeds and greater power efficiency. The incorporation of cutting-edge technologies such as AI and machine learning, along with the ability to monitor in real-time, opens up exciting possibilities for predictive analysis and adaptive behavior. In addition, adhering to industry protocols and ensuring compatibility across different platforms could enhance its usefulness in various fields. These potential advancements strive to strengthen the interface's adaptability, dependability, and expandability, placing it at the forefront of developing data acquisition and generation methods.

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Appendix

For a more in-depth look at my SPI protocol project, you can find the complete VHDL code by following this link. It will give you a better understanding of the project's structure and implementation details.

Link: https://github.com/parthbhalani2511/SPI-PROTOCOL