Dept. of CSE, Bennett University

Digital Design – ECSE 108L

Lab Assignment – 2

In this Lab, we shall start Verilog. To run Verilog, we shall use http://www.edaplayground.com. After opening you will find Design or Testbench window pane. In the Design window you need write the Verilog Code and in the Testbench window, the testbench verification code will be written.

1. Write a Verilog code to implement AND gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of AND Gate:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2. Write a Verilog code to implement OR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of OR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. Write a Verilog code to implement XOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of XOR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

4. Write a Verilog code to implement NOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of NOR Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

5. Write a Verilog code to implement NAND gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of NAND Gate:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

6. Write a Verilog code to implement XNOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of XNOR Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

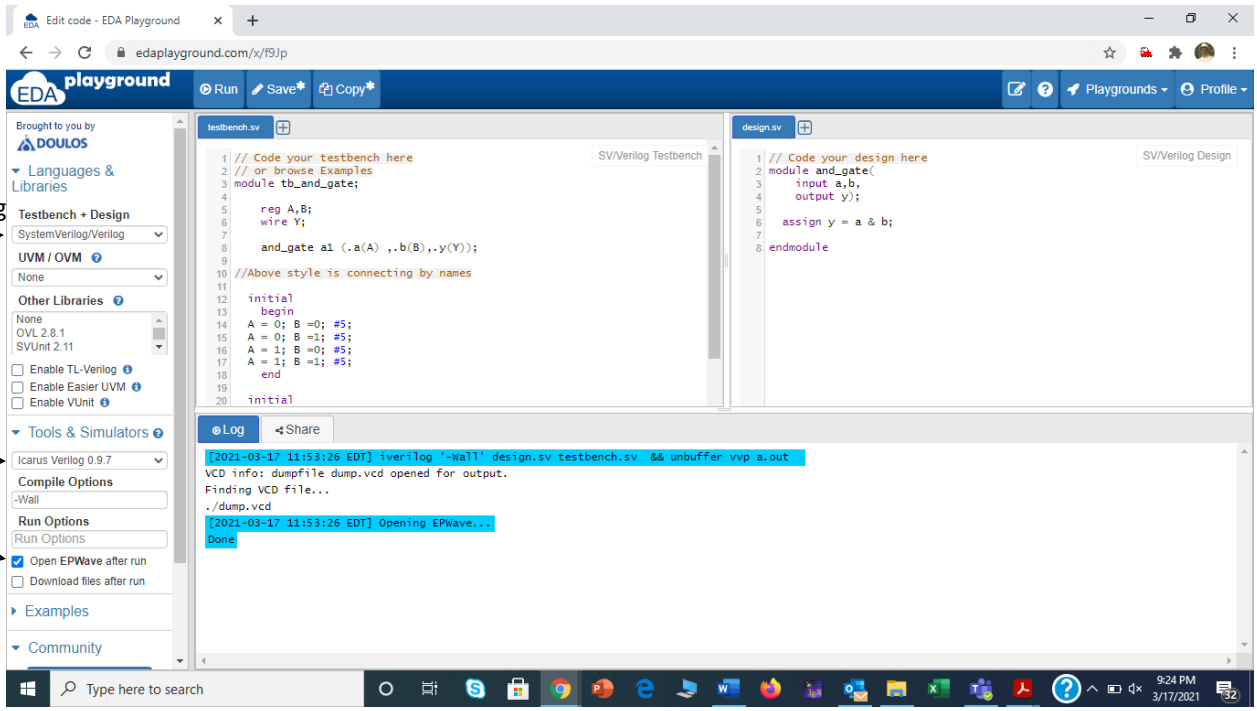
Procedure to run the programs in EDAPlayground:

- **Open** http://www.edaplayground.com
- **Go to Design Window to write the Verilog Code.**
- **Go to TestBench Window to write the TestBench Verification Code.**
- **All the other setup should be done according to the following Screenshot**

(1)
Select SystemVerilog

(2)
Select Icarus Verilog 0.9.7 in Tools and Simulator

(3)
Make it sure the check box has been clicked “Open EPWave after run”



- **Sample Verilog Code for AND Gate:**

```
module and_gate(
   input a,b,
   output y);
   assign y = a & b;
endmodule
```

- **Sample TestBench Code for the AND Gate:**

```
module tb_and_gate;

   reg A,B;
   wire Y;
   and_gate a1 (.a(A) ,.b(B),.y(Y));

initial
   begin
         A = 0; B =0; #5;
         A = 0; B =1; #5;
         A = 1; B =0; #5;
         A = 1; B =1; #5;
   end
```

```
initial
  begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end

endmodule
```

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
    5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment2.pdf)**.
    6. Submit your file on LMS **within the deadline**.

- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.
- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.