Dept. of CSE, Bennett University

Digital Design – ECSE 108L

Lab Assignment – 5

In this lab, we shall learn about the procedures in Verilog, generation of modules from a truth table, and if-else conditional statements.

We also further explore the “Module Instantiation”, where a previously designed module will be used other modules.

Q1. Consider the following expressions. Here A, B, and C are acting as input.

X = A.B’.C + A’.B.C’

Y = A’.B’ + B.C’

Z = X’.Y + Y’.X

(i) Generate the truth table for each expression.

(ii) Write down the modules for X and Y. use the instances of X and Y to implement the module for Z.

(iii) Verify the same with the corresponding Testbench code.

Q 2. Observe the given truth table.

A	**B**	**C**	**Output**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(i) Generate the corresponding Boolean expression for the above truth table and express them using Universal NAND gate representation.

(ii) Write a module for a 3 input NAND gate and use its instance to develop the Verilog code for the expression in step one.

(iii) Verify the same with corresponding Testbench code.

Q 3. Design Verilog module for BCD to 7 segment display circuit using structural design. Test using test bench. (Utilize don't care to optimize the circuit) utilize modular design to make task easier. It means make separate module for all seven output separately then utilize then in the final module.

Q4. Design a Verilog code for BCD to excess-3 code. Using behavioral design then test with test bench code.

(i) Prepare truth table.
(ii) Identify Boolean function for each output using K-maps.
(iii) Write Verilog code for implement the module.
(iv) Check with test bench.