Dept. of CSE, Bennett University

Digital Design – ECSE 108L

Lab Assignment – 3

In this Lab, we shall go for more elaboration of Verilog. Students will start coding in Structural as well as Behavioral Verilog coding. For a reminder, to run Verilog, we shall use http://www.edaplayground.com. After opening you will find Design and Testbench window pane. In the Design window you need write the Verilog Code and in the Testbench window, the testbench verification code will be written.

1. Write down a **Structural** Verilog code to implement XOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of XOR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

2. Write down a **Structural** Verilog code to implement XNOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of XNOR Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

3. Write down both the (i) **behavioural and (ii) structural** Verilog code to implement the following expression.

   Y = A.B.C + A'.B.C + A'.B'.C + A'.B'.C' + A.B'

   (iii) Generate the Truth Table manually for the same.

   (iv) Verify the same with corresponding Testbench Code.

- **Sample Structural Verilog Code for XOR Gate:**

```
module build_xor (a, b, c);
 input a, b;
 output c;
 wire x, y, a_not, b_not;
   not a_inv (a_not, a);
   not b_inv (b_not, b);
   and a1 (x, a_not, b);
   and a2 (y, b_not, a);
   or out (c, x, y);
endmodule
```

- **Sample TestBench Code for the XOR Gate:**

```
module tb_xor_str;
    reg A,B;
    wire C;
  build_xor a1 (.a(A) ,.b(B),.c(C));
//Above style is connecting by names
  initial
    begin
  A = 0; B =0; #5;
  A = 0; B =1; #5;
  A = 1; B =0; #5;
  A = 1; B =1; #5;
    end
  initial
  begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
endmodule
```

Submission Instructions:

- Prepare the submission file according to the following process:

    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.

4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.
5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: E20CSE001_ Assignment3.pdf)**.
6. Submit your file on LMS **within the deadline**.

- Write your **Name and Roll No. as comment before starting of each program**. Keep in mind this is **Mandatory**. Failing which you may lose your marks.
- Make it sure that in each program, **you have mentioned enough comments** regarding the explanation of program instructions.
- **Each student will submit their assignment on their corresponding group slot only.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead penalty.