REGENT EDUCATION & RESEARCH FOUNDATION

GROUP OF INSTITUTIONS

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SEMESTER: 4TH **YEAR:** 2ND

SUBJECT: Analog Electronics

ASSIGNMENT: Assignment - 1

1. What are the advantages of Representation of Gain in Decibels (dB).

=> Logarithmatic scale is preferred over linear scale to represent voltage & Power gains because of the following reasons:-

• In multistage amplifiers, it permits to add individual gains of the stages to calculate overall gain.

• It allows us to denote, both very small as well as very large quantities of linear scale by considerably small figures.

For example, voltage gain of 0.0000001 can be represented as - 140 dB & voltage gain of 1,00,000 can be represented as 100 dB.

• Many times output of the amplifier is fed to loudspeakers to produce sound which is received by human ear. It is important to note that the ear responds to the sound intensities on a proportional or logarithmatic scale rather than linear scale. Thus used dB unit is more appropriate for representation of amplifier gains.

2. Draw a half-wave rectifier circuit with Capacitor filter & equivalent operation.

=>

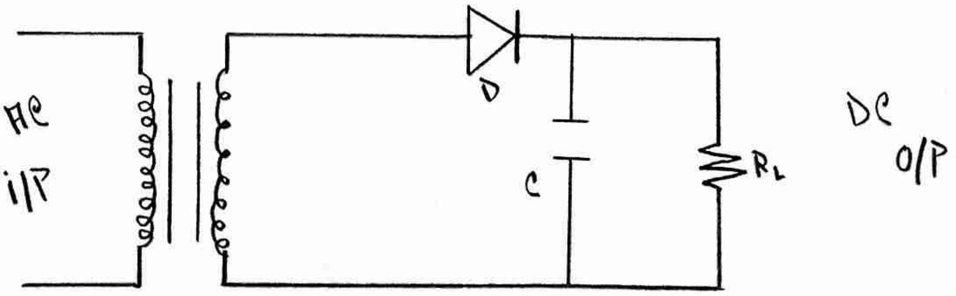


Fig:- Half wave rectifier circuit with capacitor filter

The O/P waveform of a half-wave rectifier is a Pulsating DC waveform. Filters in a half wave rectifiers are used to transform the Pulsating waveform into constant DC waveforms. A capacitor or an inductor can be used as a filter.

The circuit diagram above shows how a capacitive filter is used with half wave rectifier to smoothen out a Pulsating DC waveform into a constant DC waveform.

3. Draw a common Emitter Amplifier circuit & explain it's circuit operation.

=>

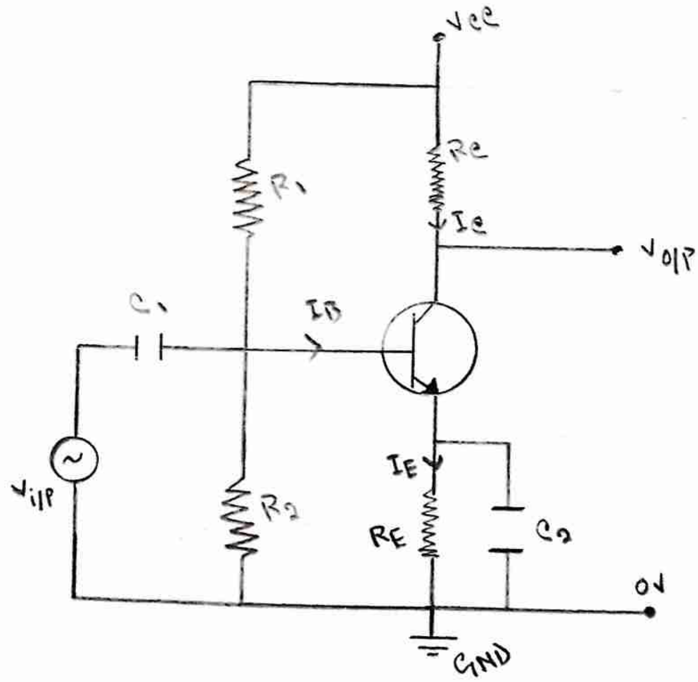


Fig:- A common emitter Amplifier circuit

A signal is applied across the emitter base junction, the forward bias across this junction, the forward bias across this junction increases during the upper half-cycle. This leads to as increase in the flow of electrons from the emitter to a collector through the base. hence increases the collector current. The increasing collector current makes more voltage drops across the collector load resistor R_C. The negative half cycle decreases the forward bias voltage across the emitter base junction.

4. what is Q-Point & DC load line? write different type of biasing arrangement is used in BJT circuits.

=> Q Point or the operating point of a device also known as a bias point, or quiescent point is the steady-state DC voltage or current at a specified terminal of an active device such as a diode or transistor with no input signal applied.

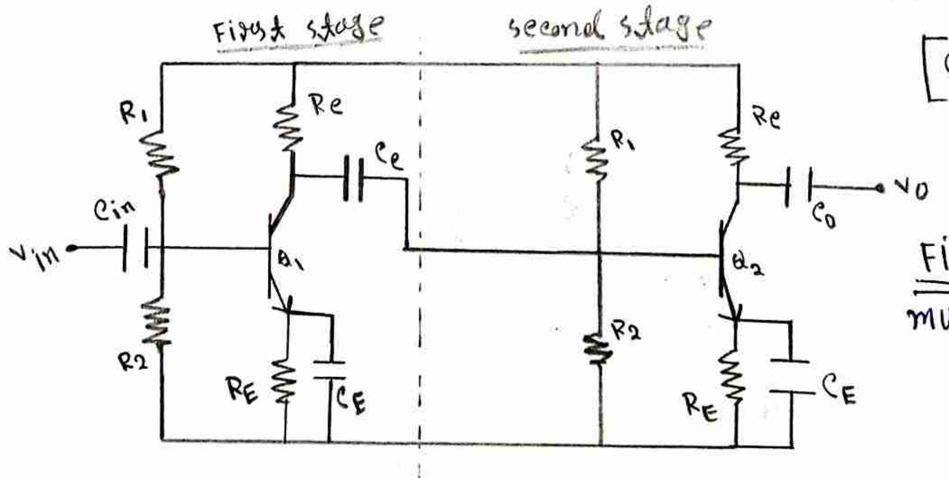
The DC load line is the load line of the DC equivalent circuit, defined by reducing the reactive compound to zero.

→ 5 different types of biasing arrangements is used in BJT circuits,

i) Fixed bias,
ii) Collector-to-base bias,
iii) Fixed bias with emitter resistor,
iv) voltage devider bias or Potential bias,
v) Emitter bias.

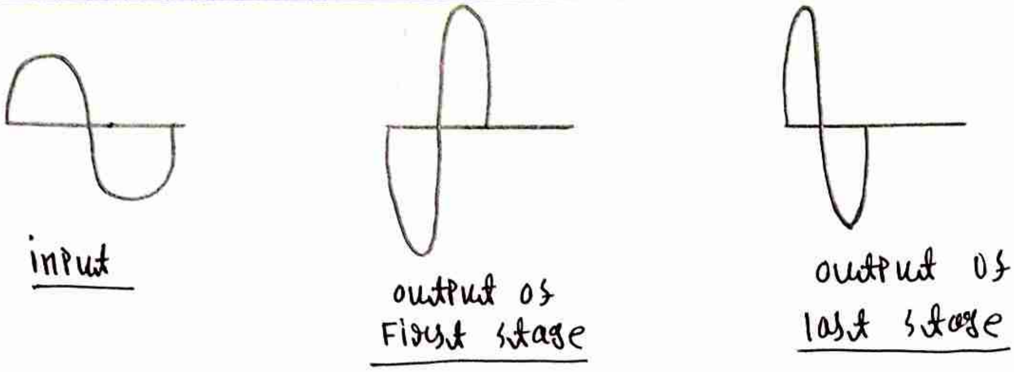
5) Draw a RC couple circuit multistage BJT amplifier. what is Phase difference between input and output signal?

=>



[C_C = Coupling capacitor]

Fig:- RC Coupled multistage BJT amplifier.



In this kind of amplifier, the input signal applied at the base of the transistor in stage 1 (Q_1) is amplified and appears at its collector terminal with a phase shift of 180°.

6. What is ripple factor? Write the expression of ripple factor of halfwave rectifier circuit.

⇒ The ripple factor is defined as the ratio of the RMS value of the AC component of the output voltage to the average value of the output voltage. A lower ripple factor indicates a smoother DC voltage output with less AC voltage ripple.

Mathematically, the ripple factor can be expressed as:

$$\text{Ripple factor} = \frac{V_{rms}}{V_{dc}}$$

where V_{rms} is the RMS voltage of the AC component of the output voltage, and V_{dc} is the average value of the output voltage

→ Ripple factor of half wave rectifier:-

From the formula of ripple factor, we know that

$$r = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

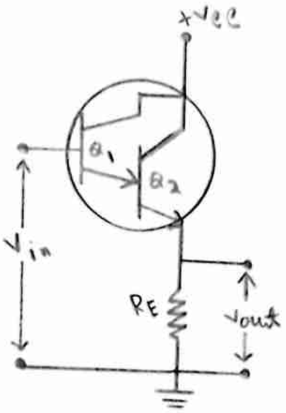
Rearranging the above equation, we get the ripple factor of half wave rectifier as:

$$r = \frac{I^2_{rms} - I^2_{dc}}{I_{dc}} = 1.21$$

Half wave rectifier

7) Draw a Darlington emitter follower circuit. Calculate the current gain.

⇒



Let, we have a Darlington emitter follower circuit with a first transistor (Q1) having a current gain of 100 and a second transistor (Q2) having a current gain of 200. Using the formula, we can calculate the current gain of the Darlington pair:

$$\text{current gain} = \beta_1 \times \beta_2 \times (\beta_1 + \beta_2 + 1)$$

$$= 100 \times 200 \times (100 + 200 + 1)$$

$$= 6,060,000$$

Therefore, the current gain of the Darlington emitter follower circuit is 6,060,000. where β_1 & β_2 are the current gains of the individual transistors in the Darlington Pair.

8) In an amplifier of common Emitter configuration estimate current Gain.

=> In a common emitter configuration, the input signal is applied to the base terminal, and the output is taken from the collector terminal. The emitter terminal is connected to common ground.

The current gain of a common emitter amplifier can be estimated using the following formula.

$$A_i = \Delta I_C / \Delta I_b$$

where A_i is the current gain, ΔI_c is the change in collector current, and ΔI_b is the change in base current.

In a common emitter configuration, the collector current is given by:

$$I_c = \beta I_b$$

where β is the common emitter current gain or h_{fe} of the transistor.

Therefore, the current gain of a common emitter amplifier can be estimated as:

$$A_i = \Delta(\beta I_b) / \Delta I_b$$
$$A_i = \beta$$

So, the current gain of a common emitter amplifier is approximately equal to the current gain of the transistor in the circuit, which is typically between 50 to 500 for most transistors.

9) In a voltage divider bias circuit, determine the collector current (I_C) and collector emitter voltage. Assume $V_{BE} = 0.65\,V$ and $\beta = 60$, $V_{CC} = 15\,V$, $R_1 = 10\,K\Omega$, $R_2 = 4.7\,K\Omega$, $R_C = 500\,\Omega$ and $R_E = 350\,\Omega$.

⇒ Given circuit,

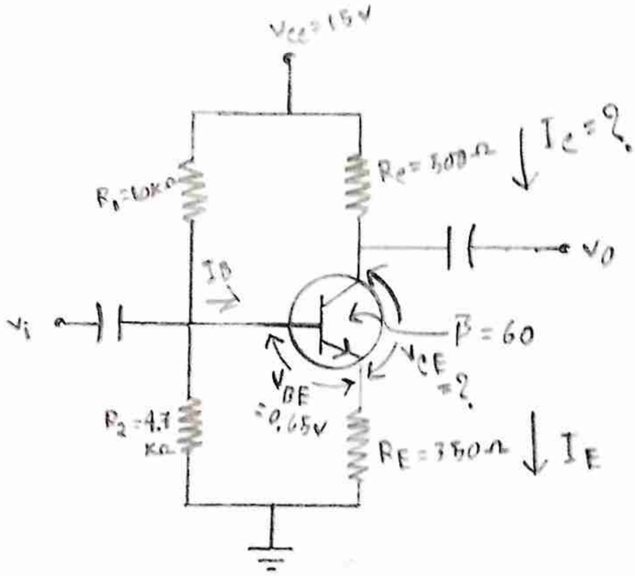


Fig:- voltage devider bias circuit

Step-1 Find V_B (Base voltage)

we know that,

$$V_B = V_{CC} \times R_2 / (R_1 + R_2)$$

$$\therefore V_B = 15\,V \times 4.7\,K\Omega / (10\,K\Omega + 4.7\,K\Omega) = 5.14\,V$$

Step-2 Calculate I_B (Base current)

we know that,

$$I_B = (V_B - V_{BE}) / R_E$$

$$\therefore I_B = (5.14\,V - 0.65\,V) / 350\,\Omega = 12.11\,mA$$

Step-3 calculate I_C (Collector current)

we know that,

$$I_C = \beta \times I_B$$

$$\therefore I_C = 60 \times 12.11 \text{ mA} = 726.6 \text{ mA}$$ Ans

Step-4 calculate voltage drop across collector resistor,

$$V_C = V_{CC} - I_C \times R_C$$

$$= 15V - 726.6 \text{ mA} \times 500\Omega = 8.66V$$

Step-5 calculate V_{CE} (Collector-emitter voltage)

we know that,

$$V_{CE} = V_C - V_{BE}$$

$$\therefore V_{CE} = 8.66V - 0.65V = 8.01V$$ Ans

Therefore, the collector current is 726.6 mA and the collector-emitter voltage is 8.01 V.

10. In a amplifier of common Emitter configurations estimate voltage gain.

⇒ A common emitter amplifier is a type of transistor amplifier that uses an NPN transistor in the common emitter configuration. The voltage gain of a common emitter amplifier can be estimated using the following formula:

$$A_V = -g_m \times R_C$$

where A_V is the voltage gain, g_m is the transconductance of the transistor, and R_C is the collector Resistance.

The transconductance of the transistor depends on its Physical properties and can be found in its datasheet. Assuming a typical NPN bipolar transistor with a transconductance of 0.05 A/V, and a collector Resistance of 1 KΩ, we can estimate the voltage gain as:

$$A_V = -0.05\ A/V \times 1\ K\Omega = -50$$

Therefore, the estimated voltage gain of the common emitter amplifier is -50, meaning the output voltage is inverted and amplified by a factor of 50 compared to the input voltage.

In conclusion, the voltage gain of a common emitter amplifier can be estimated using the formula $A_V = -g_m \times R_C$, and the actual voltage gain may vary depending on the specific properties of the transistor and the circuit design.