A 4-6 GHz Low-Power Voltage Controlled Oscillator with Wide Voltage Range Operation

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***Abstract*—Voltage Controlled Oscillator is one of the crucial component in communication systems. This paper discusses the design of a low-power VCO tailored for GHz frequency applications. The VCO is developed using CMOS technology and the Sky water 130nm PDK. This VCO operates within a wide voltage range and delivers an output frequency of 4-6 GHz and the designed VCO is expected to consume less than 1mW power at 1.8 V. This low power consumption makes the VCO suitable for applications such as IoT and battery-operated wireless systems, where energy efficiency is essential.**

***Index Terms*—Single ended voltage-controlled ring oscillator (SEVCRO), Phase noise, Differential VCRO**

I. Introduction

VCOs are essential in wireless and optical communication systems, serving a critical role in frequency synthesis for modulation and demodulation in RF signal processing. In CMOS technology, VCOs are implemented using ring oscillators, relaxation circuits, or LC resonant circuits, with ring oscillators favored for their compact design, as they eliminate the need for on-chip inductors and capacitors. This advantage makes ring oscillator-based VCOs particularly suitable for integrated circuits, providing scalability and a broad tuning range controlled through current adjustments. VCOs are also crucial in phase-locked loops (PLLs), where they generate the local oscillator signal used to lock onto a specific frequency. This paper further explores implementation strategies, pros and cons, conclusion, and future scope.

II. Implementation

The main goals of the proposed architectures are to minimize power consumption, reduce phase noise, and increase the oscillation frequency. This design consists of 3-stage CMOS single-ended oscillators. The circuit diagram of the single-ended VCRO is shown in Fig.1. This ring oscillator includes a minimum of three

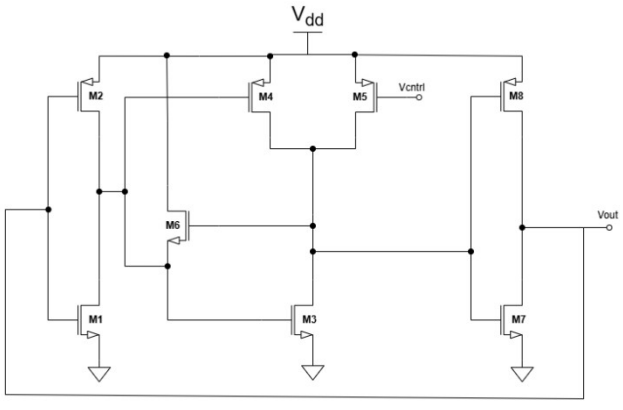

Fig. 1: The circuit diagram of single ended VCO.

delay stages, which enables it to achieve higher frequencies. In this design, transistors M1,M2 and M7,M8 form the inverter delay cells, while the M5 works as a load to control the frequency of operation.To enhance the oscillator's Q factor and reduce phase noise, transistor M6 is connected as a composite load. This architecture allows to achieve higher oscillation frequencies due to reduced capacitance and design simplicity. The proposed architecture can oscillate up to 6 GHz.

The proposed circuit are simulated for various analysis such as transient analysis, variation in oscillation frequency as a function of variation in control voltage

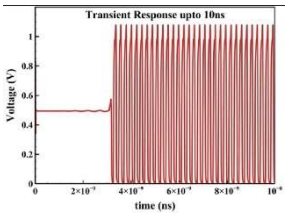

Fig. 2: Transient analysis

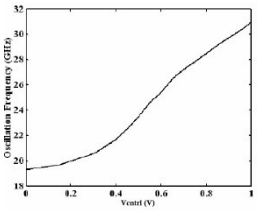

Fig. 3: Kvco

III. Pros and cons

This architecture is efficient in terms of transistor count, as it uses a minimal number of transistors. With only three stages, it achieves lower power consumption. Additionally, the reduced stage count and carefully designed structure allow the oscillator to reach high frequencies, making it suitable for high-frequency applications.

However, this design also has some limitations. The phase noise performance is generally poorer, It is also more susceptible to common-mode noise, which can lead to instability in the output signal. Furthermore, as a ring oscillator, it typically has a lower Q factor than LC oscillators.

IV. Conclusion and Future scope

In conclusion, the proposed circuit achieves a lock period of approximately 700-800 ps, delivering high frequency performance with low power consumption at 1.8V. Implementing this design in smaller technology nodes can further increase frequency and improve phase noise performance, making it a promising solution for high-speed, low-power applications.

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