School of Electrical and Electronics Engineering

CIA III Examinations July 2021

Class: I B. Tech (CSBS)

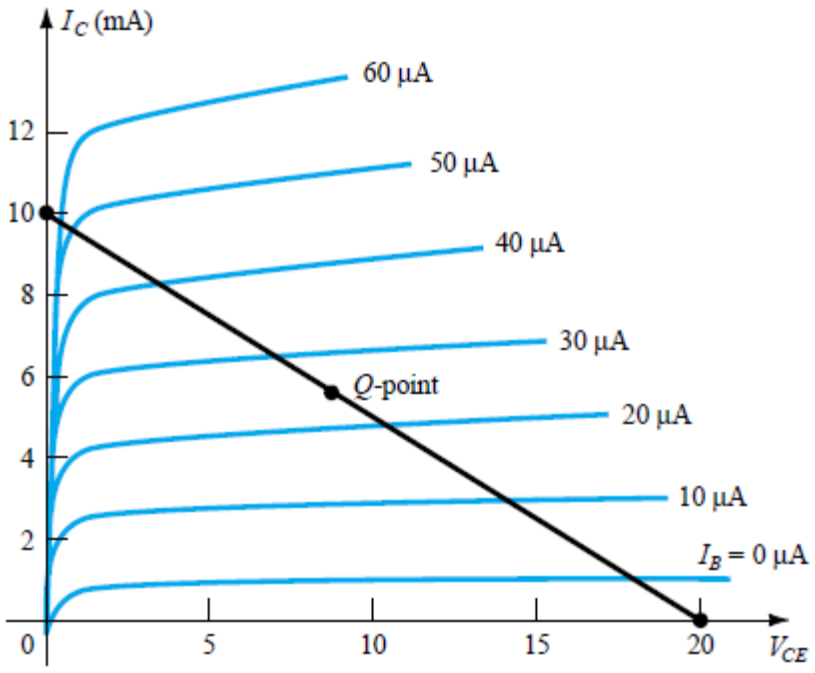
Course Code: EIE 110 **Course name: principles of Electronics**

Duration: 90 Min **Max Marks: 50**

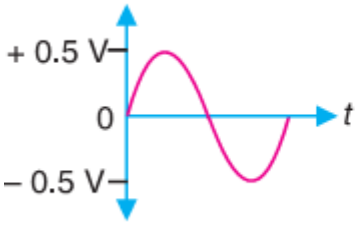
ANSWER ALL QUESTIONS

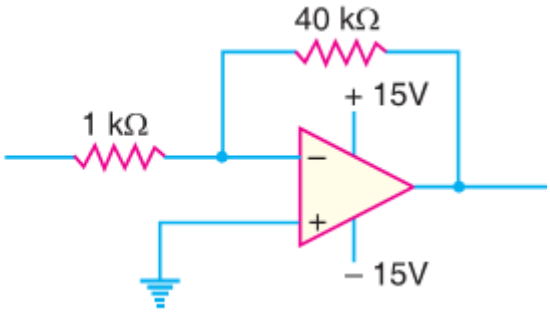
PART – A **10 * 02 = 20**

1. How do you use the diode as a switch? Explain with a neat schematic.
2. Why is the energy of electron in outer orbit is more?
3. Draw a graph showing the knee voltage for germanium and silicon semiconductor.
4. In a common base transistor connection, the emitter current is 1mA. The collector current is 50μA when emitter circuit is open. Determine the total collector current when α is 0.92.
5. For the following load line and defined Q point, determine the required values of V_{CC}, R_C and R_B for the fixed bias configuration. The transistor is made up of Si.



6. With neat schematic briefly explain the working of zero crossing detector.
7. Draw the output waveform of the following circuit





8. Draw the logic diagram using basic logic gates that implements the expression $X = AB(C\overline{D} + EF)$
9. Simplify the following Boolean expression with minimum literals $X = \overline{A}\overline{B}C + A\overline{B}C + AB\overline{C} + ABC$
10. Draw the logic diagram and truth table of RS flipflop.

PART – B **3 * 10 = 30**

11. Among the two ideal diodes that are used in a rectifier circuit, one is used to rectify the positive half cycle of the sinusoidal waveform and the other diode to rectify the negative half cycle. The input voltage to the rectifier circuit through the transformer secondary is 50 V and the load resistance is 25 ohms. Determine the peak DC voltage, peak DC current, AC component of load voltage and AC component of load current.
12. Design a circuit using operational amplifier that converts the given sinusoidal signal into square wave with lesser on-time and greater off-time. Explain the working of this circuit with neat sketches.
13. With the help of the truth table of half adder circuit, develop the logical expression for the same and draw the logic diagram using only NAND gates.