School of Electrical and Electronics Engineering
CIA III Examinations July 2021
Class: I B. Tech (CSBS)

Course Code: EIE 110 **Course name: principles of Electronics**
Duration: 90 Min **Max Marks: 50**

ANSWER ALL QUESTIONS

PART – A **10 * 02 = 20**

1. Forward bias – Closed switch, Reverse bias – Open switch
2. Energy is higher in higher orbits as in higher orbits distance is greater from the nucleus than the lower orbit. Therefore, the nucleus gives less opposing force to higher orbits. So, the energy of higher orbits is greater.
3. The VI characteristics graph of PN junction diode should show the knee voltage of 0.7 V for Si and 0.3 V for Ge.
4. Solution

Solution. Here, $I_E = 1\text{ mA}, \alpha = 0.92, \quad I_{CBO} = 50\ \mu\text{A}$

$\therefore$ Total collector current, $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$

$= 0.92 + 0.05 = \mathbf{0.97\ mA}$

5. Solution

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0 \text{ mA}$$

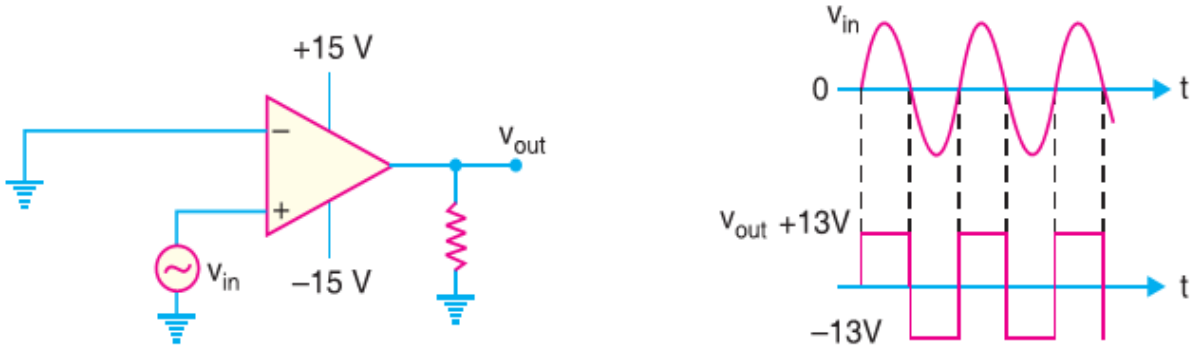
$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = \mathbf{2\ k\Omega}$$

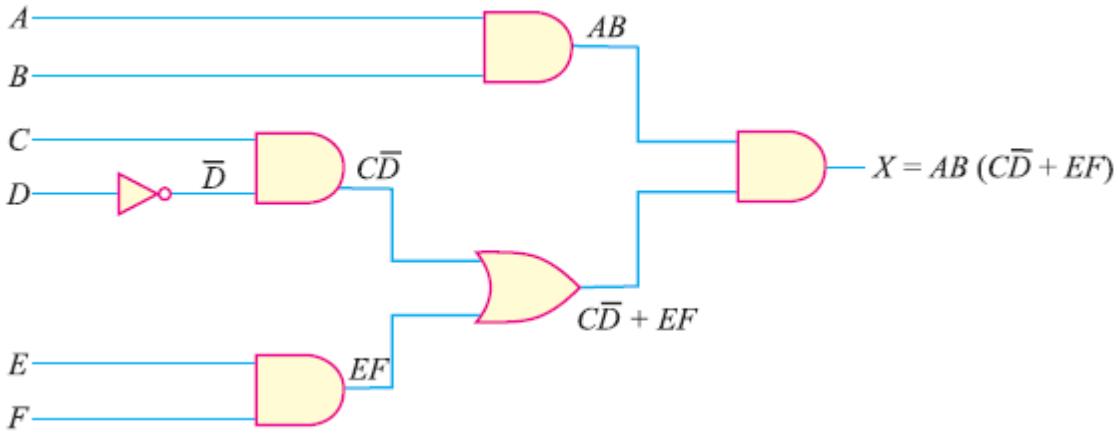
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

6.



7. Wave form showing positive and negative V saturation voltages
8. Solution



9.

Solution.

$$X = \overline{A}\overline{B}C + A\overline{B}C + AB\overline{C} + ABC$$

Step 1. Note that the first two terms have $\overline{B}C$ as common factors while the last two terms have AB as common factors.

$$\therefore \quad X = \overline{B}C\,(A + \overline{A}) + AB\,(C + \overline{C})$$

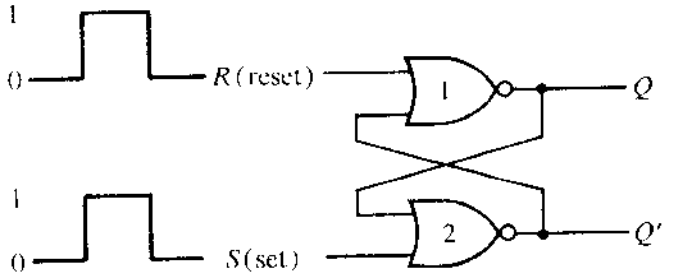
Step 2. $A + \overline{A} = 1$ and $C + \overline{C} = 1$ so that :

$$X = \overline{B}C \cdot 1 + AB \cdot 1$$

Step 3. Since $\overline{B}C \cdot 1 = \overline{B}C$ and $AB \cdot 1 = AB$ so that :

$$X = AB + \overline{B}C$$

10.



(a) Logic diagram

S	R	Q	Q′	
1	0	1	0	
0	0	1	0	(after S = 1, R = 0)
0	1	0	1	
0	0	0	1	(after S = 0, R = 1)
1	1	0	0	

(b) Truth table

PART – B **3 * 10 = 30**

11.

For a FWR circuit, the A.C. Voltage input to transformer primary = 115V. Transformer secondary voltage is 50V. R_L = 25Ω. Determine

1. *Peak DC component, RMS and AC component of load voltage.*
2. *Peak DC component, RMS and AC component of load current.*

Solution

Since, the transformer develops 50V between secondary terminals, there must be 25V across each half of the secondary winding.

The peak value across each half of secondary is $25\sqrt{2} = 35.4V$

Assuming ideal diodes, the rectified voltage across R_L also has a peak value of 35.4V(V_m).

$\therefore$ Average value V_{DC} for FWR circuit is

$$= \frac{2V_m}{\pi} = 0.636V_m$$

$$V_{DC} = 0.636 \times (35.4) = 22.5V.$$

A.C.Component load voltage is

$$V'_{rms} = \sqrt{V_m^2 - V_{DC}^2}$$

$$= \sqrt{(25)^2 - (22.5)^2} = 10.9V.$$

$$I_m = \frac{V_m}{R_L} = \frac{35.4}{25} = 1.41A.$$

$$I_{DC} = \frac{2I_m}{\pi} = 0.636I_m = 0.636(1.41) = 0.897A.$$

$$I_L(rms) = 0.707\ I_m$$

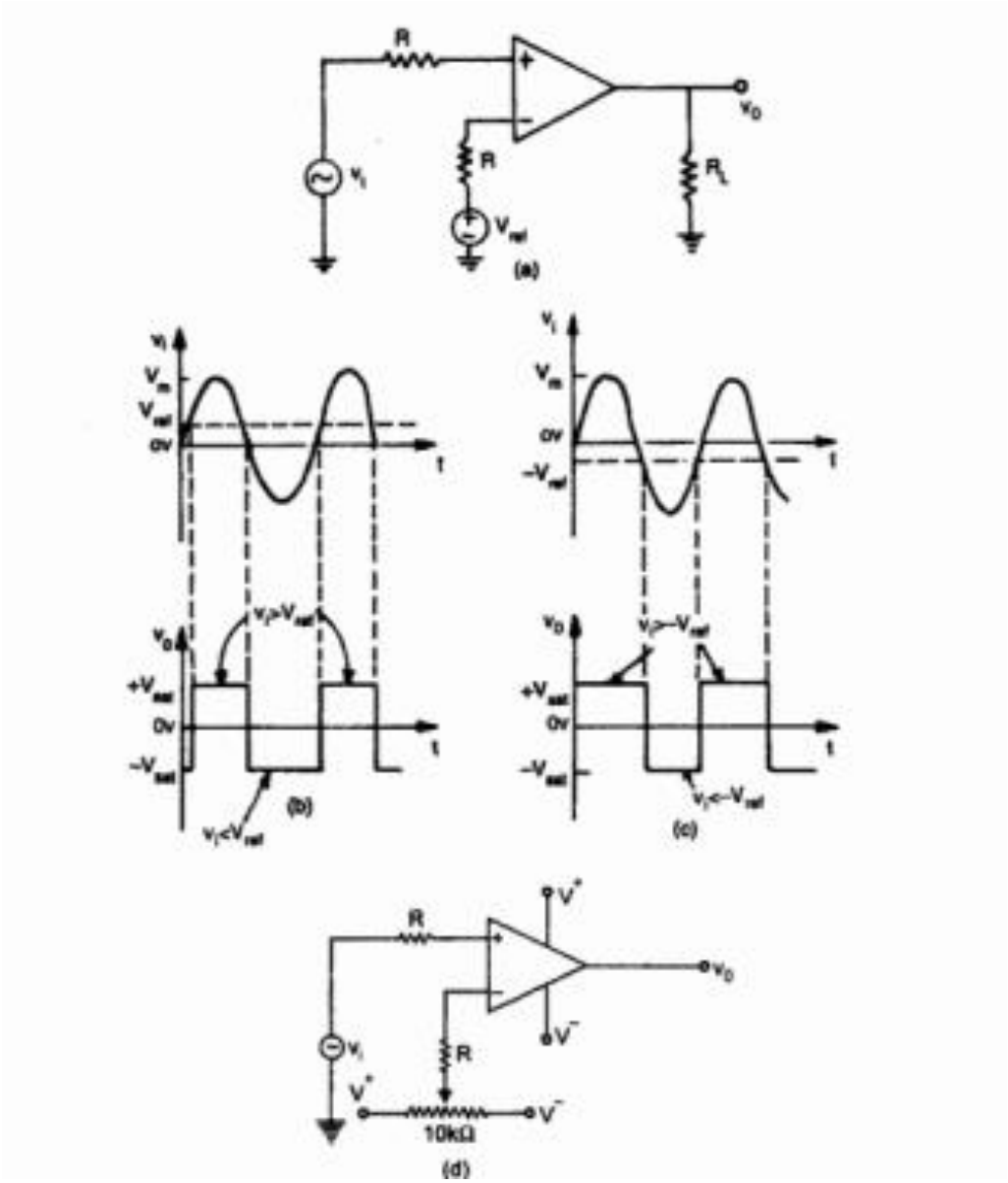
$$= 1.41(0.707) = 1A$$

$$I'_{rms} = \sqrt{(I_{rms})^2 - (I_{DC})^2}$$

$$= \sqrt{1^2 - (0.897)^2}$$

$$= 0.441\ A.$$

12


R
R
R_L
v_i
v_0
V_{ref}
(a)
V_m
0V
$-V_{ref}$
t
$v_i > V_{ref}$
$+V_{sat}$
$-V_{sat}$
$v_i < V_{ref}$
(b)
$v_i > -V_{ref}$
$v_i < -V_{ref}$
(c)
V^+
V^-
10kΩ
(d)

13.

Half adder

From the verbal explanation of a half-adder, we find that this circuit needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry. It is necessary to specify two output variables because the result may consist of two binary digits. We arbitrarily assign symbols x and y to the two inputs and S (for sum) and C (for carry) to the outputs.

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

S – LSB

C - MSB

The simplified Boolean functions for the two outputs can be obtained directly from the truth table. The simplified sum of products expressions are

$$S = x'y + xy'$$

$$C = xy$$

Logic diagram implementation using only NAND gates - 06