UNIT – IV **15 Periods**

Memory system: Basic Concepts - Semiconductor RAM Memories - Read-only Memories - Direct Memory Access - Memory Hierarchy - Cache Memories - Performance Considerations - Virtual Memory - Memory Management Requirements - Secondary Storage.

Basic Input/Output: Accessing I/O Devices - Interrupts.

Input / Output Organization: Bus Structure - Bus Operation – Arbitration - Interface Circuits - Interconnection Standards

Memory Systems

Introduction

- Execution speed of programs is highly dependent on the speed with which instructions and data can be transferred between the processor and the memory.

- Ideally, the memory would be fast, large, and inexpensive.Unfortunately, it is impossible to meet all three of these requirements simultaneously.

- Increased speed and size are achieved at increased cost.Much work has gone into developing structures that improve the effective speed and size of the memory, yet keep the cost reasonable.

Basic Concepts

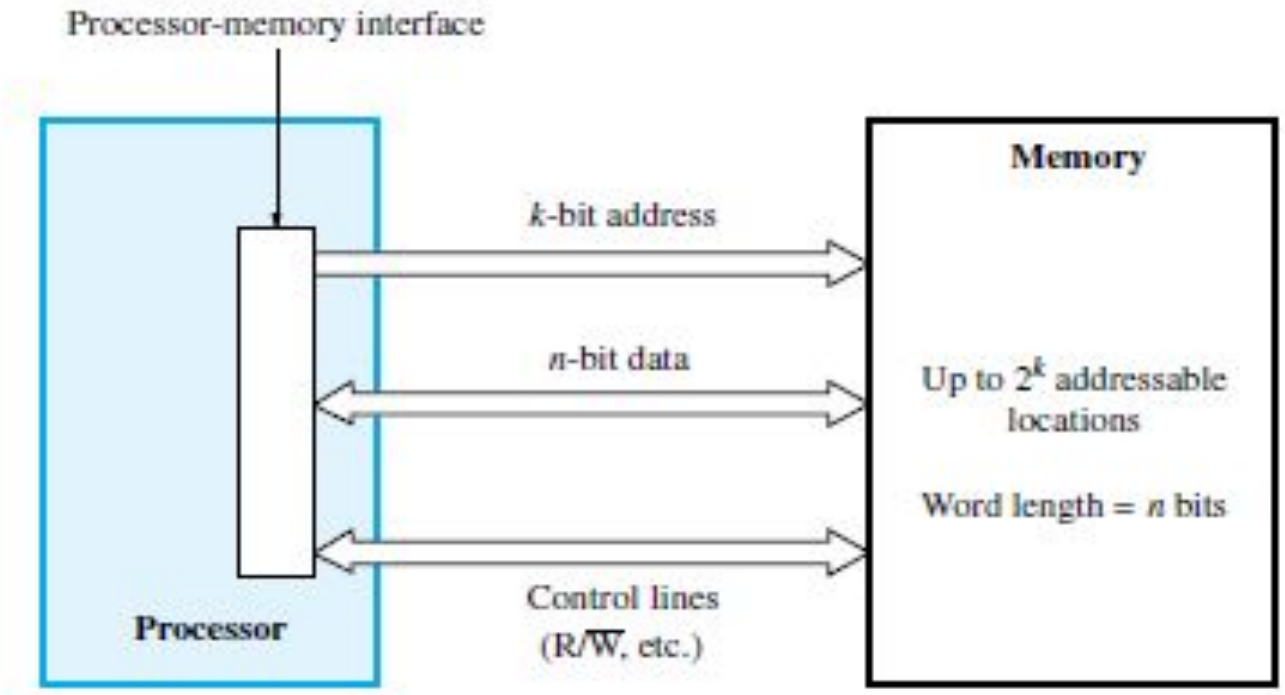
- The maximum size of the memory that can be used in any computer is determined by the addressing scheme.

- For example, a computer that generates 16-bit addresses is capable of addressing up to = 64K (kilo) memory locations

- The memory is usually designed to store and retrieve data in word-length quantities.Consider, for example, a byte-addressable computer whose instructions generate 32-bit addresses.

- When a 32-bit address is sent from the processor to the memory unit, the high order 30 bits determine which word will be accessed. If a byte quantity is specified, the low-order 2 bits of the address specify which byte location is involved.

The connection between the processor and its memory consists of address, data, and control lines,



Connection of the memory to the processor

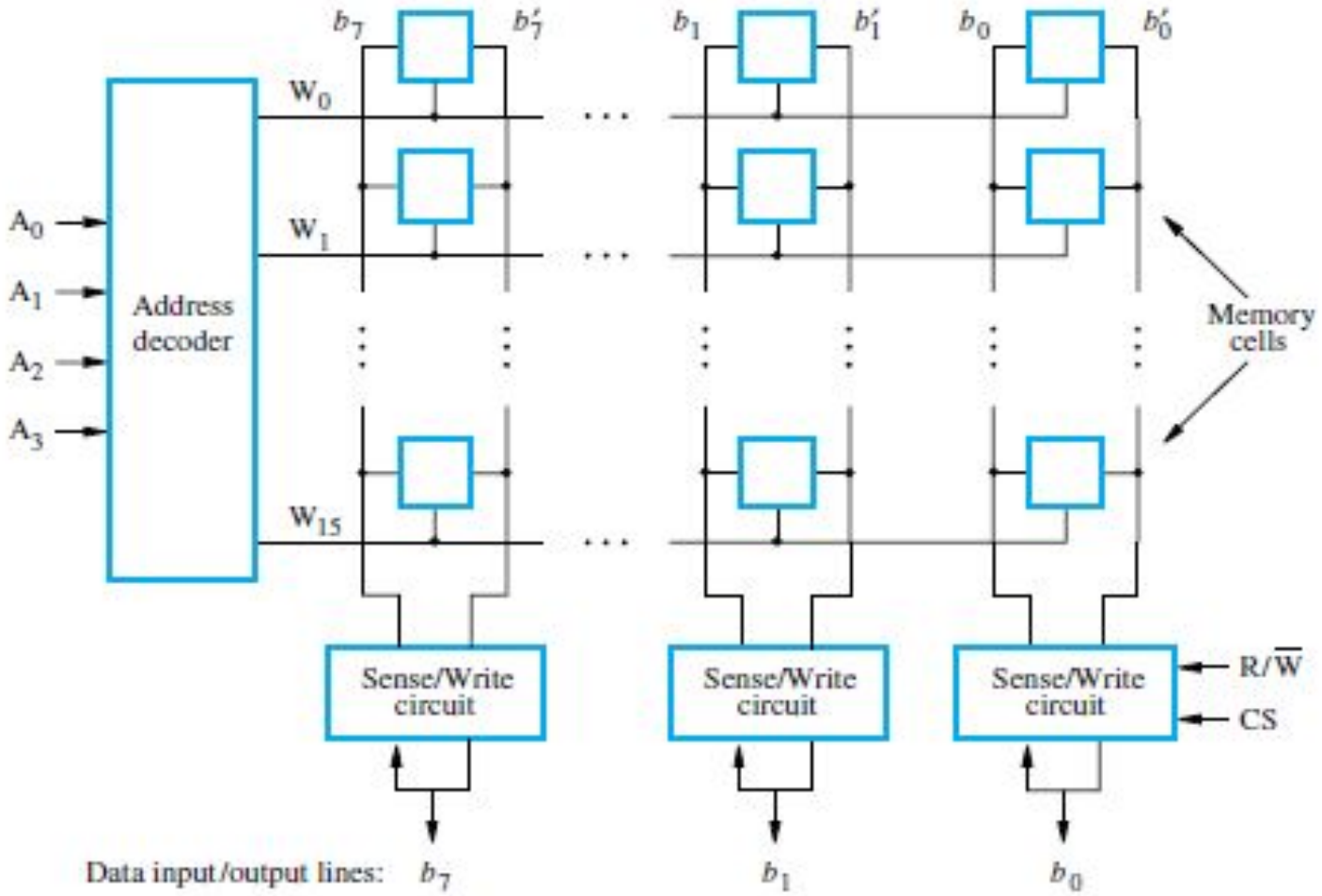
Cache and Virtual Memory

- The processor of a computer can usually process instructions and data faster than they can be fetched from the main memory.
- Hence, the memory access time is the bottleneck in the system.
- One way to reduce the memory access time is to use a cache memory.
- This is a small, fast memory inserted between the larger, slower main memory and the processor.
- It holds the currently active portions of a program and their data.

- Virtual memory With this technique, only the active portions of a program are stored in the main memory, and the remainder is stored on the much larger secondary storage device.
- Sections of the program are transferred back and forth between the main memory and the secondary storage device in a manner that is transparent to the application program.
- As a result, the application program sees a memory that is much larger than the computer's physical main memory.

Semiconductor RAM Memories

Internal Organization of Memory Chips



- Memory cells are in the form of an array, in which each cell is capable of storing one bit of information.

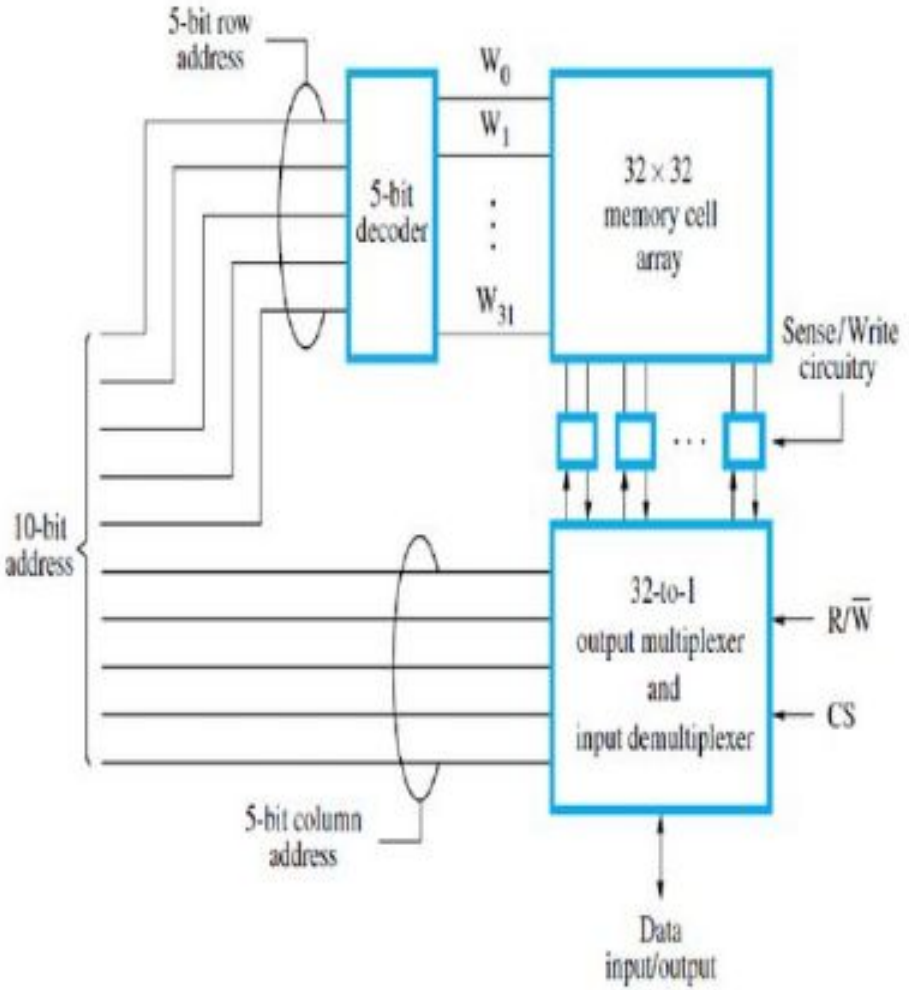
- Each row of cells constitutes a memory word, and all cells of a row are connected to a common line referred to as the word line, which is driven by the address decoder on the chip.

- The cells in each column are connected to a Sense/Write circuit by two bit lines, and the Sense/Write circuits are connected to the data input/output lines of the chip.

- During a Read operation, these circuits sense, or read, the information stored in the cells selected by a word line and place this information on the output data lines.

- During a Write operation, the Sense/Write circuits receive input data and store them in the cells of the selected word.

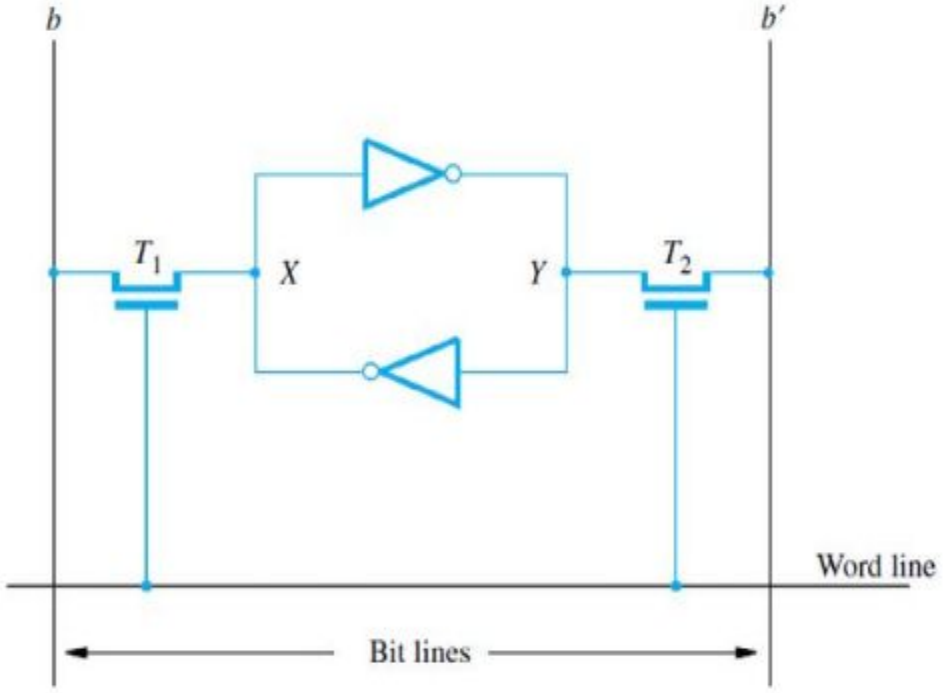
- Organization of a 1K × 1 memory chip.10-bit address is divided into two groups of 5 bits each to form the row and column addresses for the cell array.
- A row address selects a row of 32 cells, all of which are accessed in parallel.
- But, only one of these cells is connected to the external data line, based on the column address



Organization of a 1K × 1 memory chip.

Semiconductor RAM Memories-6 Static Memories (SRAM)

Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.



A static RAM cell.

Semiconductor RAM Memories

Static Memories (SRAM)

- Two inverters are cross-connected to form a latch. The latch is connected to two bit lines by transistors T1 and T2.

- These transistors act as switches that can be opened or closed under control of the word line.

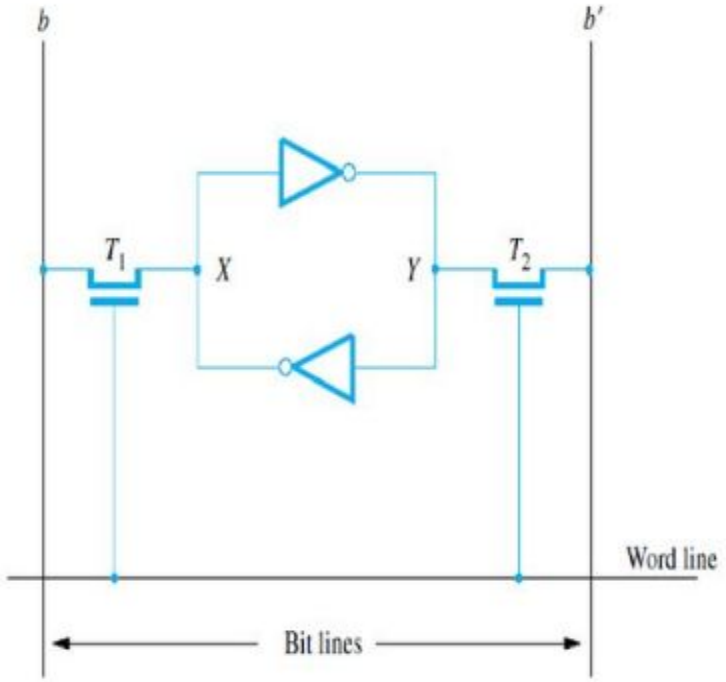
- When the word line is at ground level, the transistors are turned off and the latch retains its state.

- For example, if the logic value at point X is 1 and at point Y is 0, this state is maintained as long as the signal on the word line is at ground level. Assume that this state represents the value 1.

Static Memories (SRAM)

Read Operation

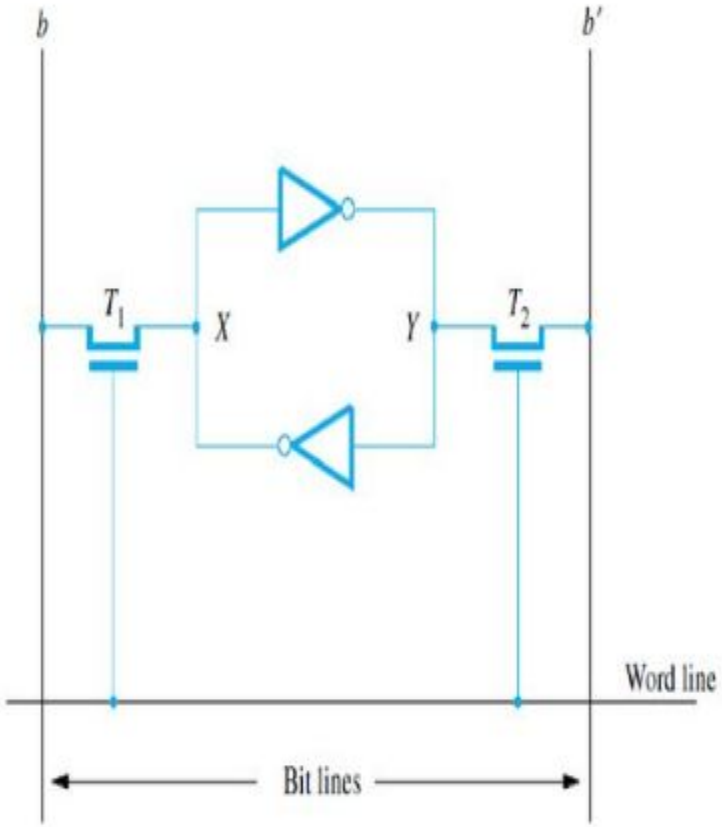
- Assume cell is in state 1.
- To read keep Word line to 1.
- So signal on bit line b is high and the signal on bit line b` is low



A static RAM cell.

Write Operation

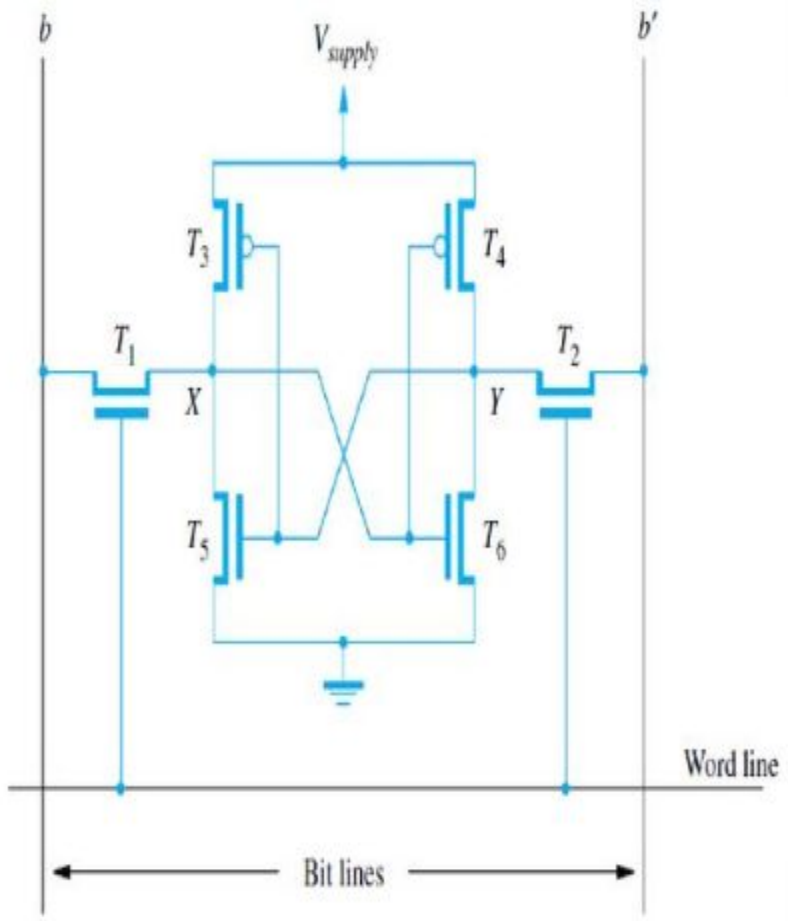
- During a Write operation, the Sense/Write circuit drives bit lines b and b`.
- It places the appropriate value on bit line b and its complement on b` and activates the word line.
- This forces the cell into the corresponding state, which the cell retains when the word line is deactivated.



A static RAM cell.

CMOS Cell

- Transistor pairs (T3, T5) and (T4, T6) form the inverters in the latch.
- The state of the cell is read or written as just explained.
- For example, in state 1, the voltage at point X is maintained high by having transistors T3 and T6 on, while T4 and T5 are off.
- If T1 and T2 are turned on, bit lines b and b` will have high and low signals, respectively.



An example of a CMOS memory cell.

Static memories

- Continuous power is needed for the cell to retain its state. If power is interrupted, the cell's contents are lost. When power is restored, the latch settles into a stable state, but not necessarily the same state the cell was in before the interruption. Hence, SRAMs are said to be volatile memories.

- A major advantage of CMOS SRAMs is their very low power consumption, because current flows in the cell only when the cell is being accessed.Static RAMs can be accessed very quickly.

- Access times on the order of a few nanoseconds are found in commercially available chips. SRAMs are used in applications where speed is of critical concern.

Semiconductor RAM Memories

Asynchronous Memories (DRAM)

- Static RAMs are fast, but their cells require several transistors.
- Less expensive and higher density RAMs can be implemented with simpler cells.
- But, these simpler cells do not retain their state for a long period, unless they are accessed frequently (Refreshed) for Read or Write operations.
- Memories that use such cells are called dynamic RAMs (DRAMs).

Semiconductor RAM Memories

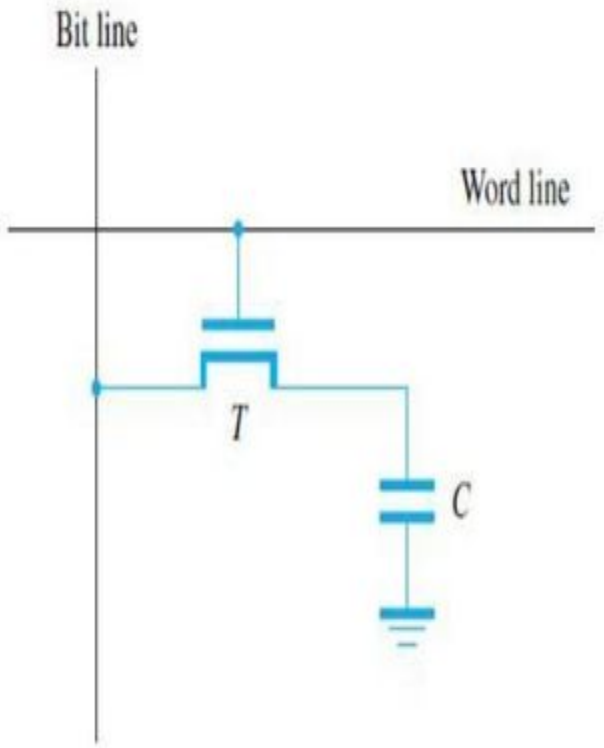
Asynchronous Memories (DRAM)

- Information is stored in a dynamic memory cell in the form of a charge on a capacitor, but this charge can be maintained for only tens of milliseconds.

- Since the cell is required to store information for a much longer time, its contents must be periodically refreshed (read or write) by restoring the capacitor charge to its full value.

Semiconductor RAM Memories
Asynchronous Memories (DRAM)

A single-transistor dynamic memory cell.To store information in this cell, transistor T is turned on and an appropriate voltage is applied to the bit line.
This causes a known amount of charge to be stored in the capacitor.
After the transistor is turned off, the charge remains stored in the capacitor, but not for long.
The capacitor begins to discharge.

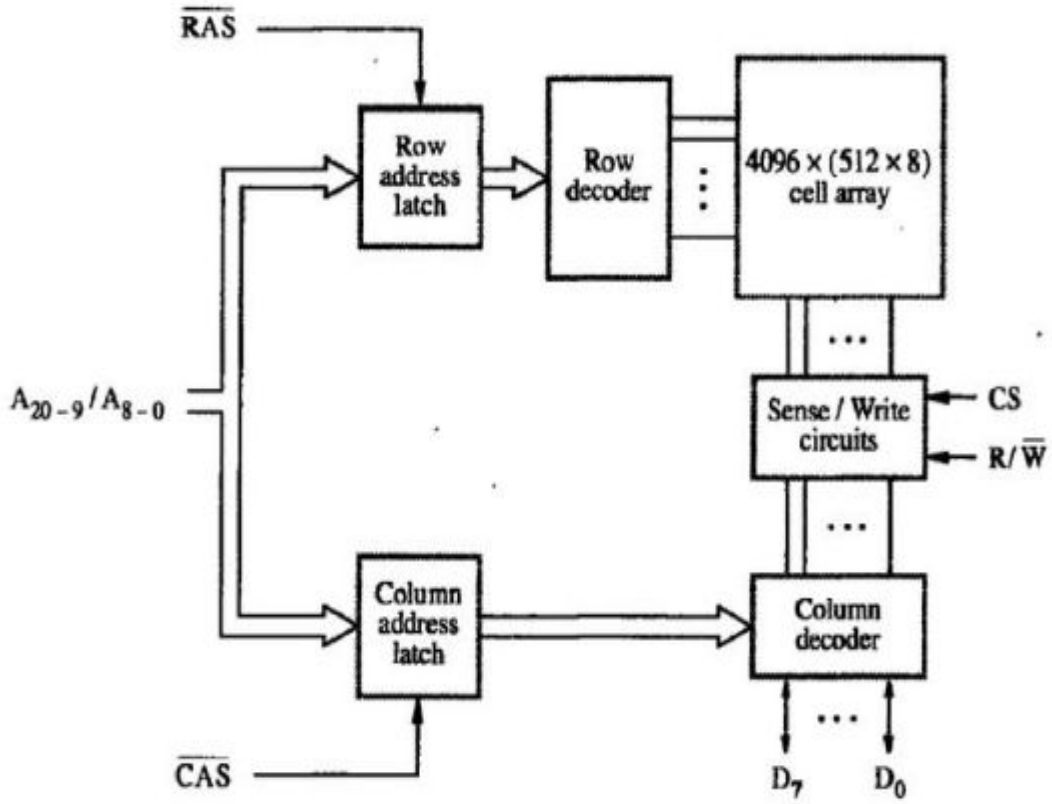


A single-transistor dynamic memory cell.

Semiconductor RAM Memories

Asynchronous Memories (DRAM)

Internal organization of a 2M × 8 dynamic memory chip.



Internal organization of a 2M x 8 dynamic memory chip.

Semiconductor RAM Memories
Asynchronous Memories (DRAM)

- A 16-Megabit DRAM chip, configured as 2M × 8, is shown in above diagram.The cells are organized in the form of a 4K × 4K array.

- The 4096 cells in each row are divided into 512 groups of 8, forming 512 bytes of data.Therefore, 12 address bits are needed to select a row, and another 9 bits are needed to specify a group of 8 bits in the selected row.

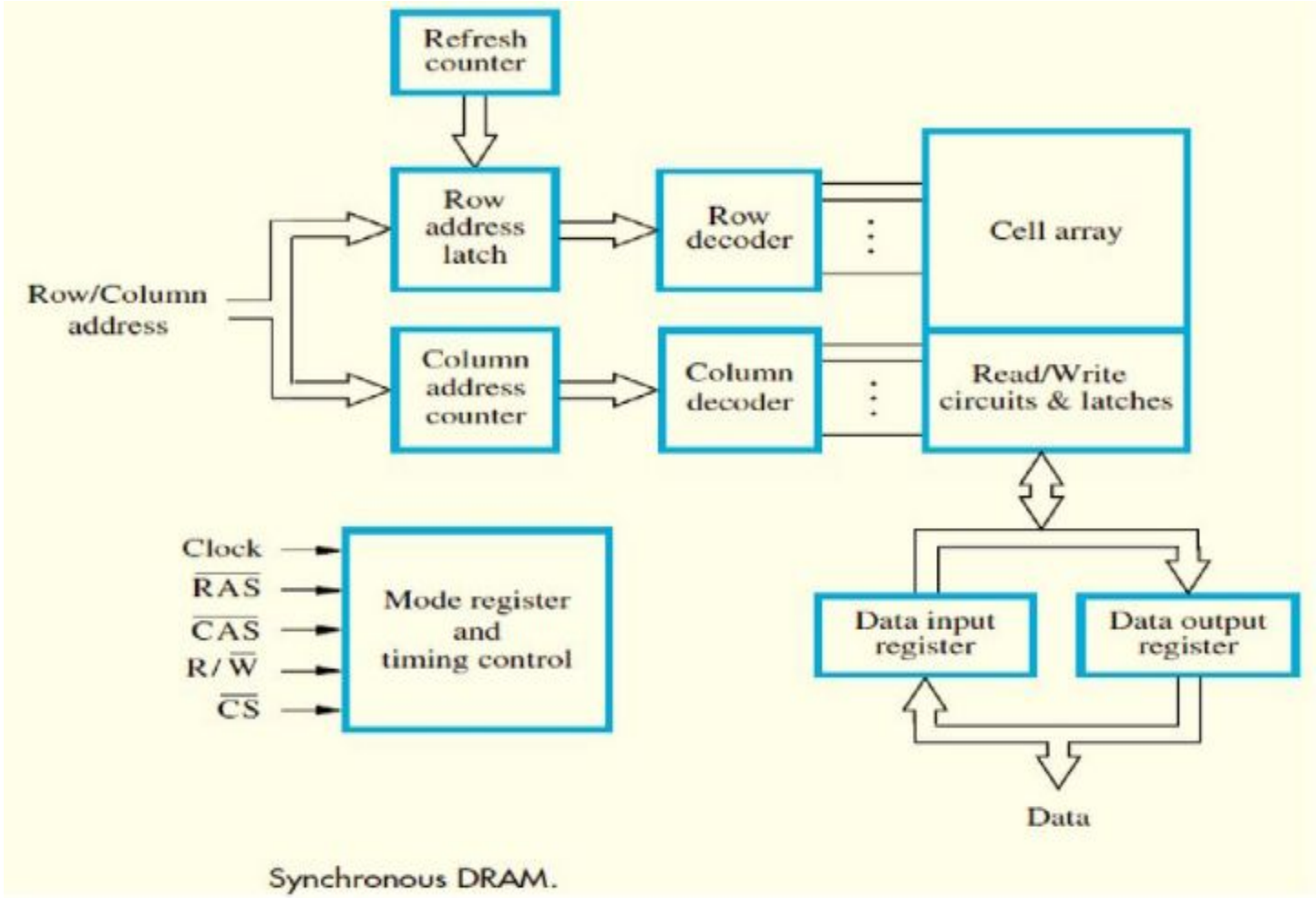
- In total, a 21-bit address is needed to access a byte in this memory.The high-order 12 bits and the low-order 9 bits of the address constitute the row and column addresses of a byte, respectively.

- To reduce the number of pins needed for external connections, the row and column addresses are multiplexed on 12 pins.

Semiconductor RAM Memories
Asynchronous Memories (DRAM)

- During a Read or a Write operation, the row address is applied first.
- It is loaded into the row address latch in response to a signal pulse on an input control line called the Row Address Strobe (RAS).
- This causes a Read operation to be initiated, in which all cells in the selected row are read and refreshed.

Semiconductor RAM Memories-24
Synchronous DRAMs(SDRAM)



Synchronous DRAM.

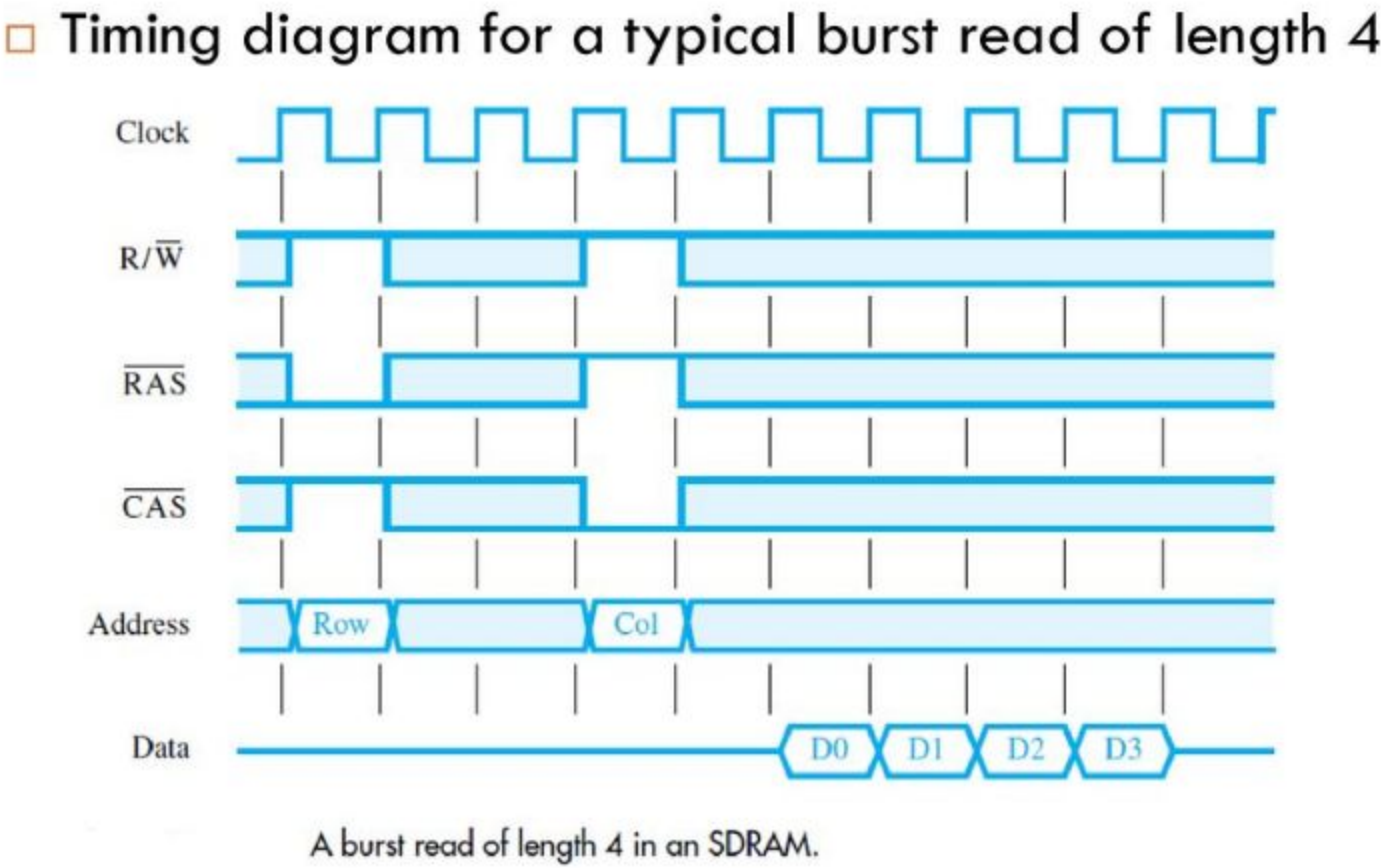
Semiconductor RAM Memories
Synchronous DRAMs(SDRAM)

- SDRAMs have several different modes of operation, which can be selected by writing control information into a mode register.
- For example, in burst operations of different lengths can be specified.
- It is not necessary to provide externally-generated pulses on the CAS line to select successive columns.
- The necessary control signals are generated internally using a column counter and the clock signal.
- New data are placed on the data lines at the rising edge of each clock pulse.

Semiconductor RAM Memories

Synchronous DRAMs(SDRAM)

Timing diagram for a typical burst read of length 4



A burst read of length 4 in an SDRAM.

Semiconductor RAM Memories
Synchronous DRAMs(SDRAM)

Latency and Bandwidth

- Data transfers to and from the main memory often involve blocks of data. The memory access time defined earlier is not sufficient for describing the memory's performance when transferring blocks of data.
- During block transfers, memory latency is the amount of time it takes to transfer the first word of a block. The time required to transfer a complete block depends also on the rate at which successive words can be transferred and on the size of the block.

- The time between successive words of a block is much shorter than the time needed to transfer the first word. For instance, as in the timing diagram, the access cycle begins with the assertion of the RAS signal.
- The first word of data is transferred five clock cycles later. Thus, the latency is five clock cycles. If the clock rate is 500 MHz, then the latency is 10 ns. The remaining three words are transferred in consecutive clock cycles, at the rate of one word every 2 ns.

Semiconductor RAM Memories
Synchronous DRAMs

- Double-Data-Rate SDRAM (DDR-RAM)The key idea is to take advantage of the fact that a large number of bits are accessed at the same time inside the chip when a row address is applied.

- To make the best use of the available clock speed, data are transferred externally on both the rising and falling edges of the clock.

- For this reason, memories that use this technique are called double-data-rate SDRAMs (DDR SDRAMs).

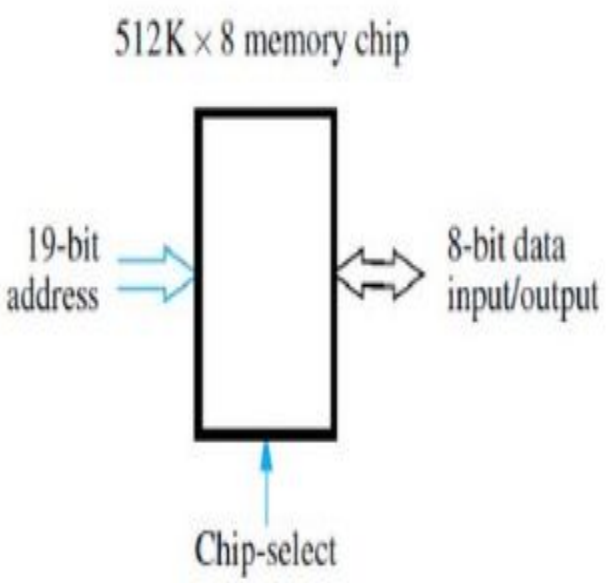
Semiconductor RAM Memories
Structure of Larger Memories

Static Memory Systems

- Consider a memory consisting of 2M words of 32 bits each.
- Shown in next slide, how this memory can be implemented using 512K × 8 static memory chips.
- Each column in the figure implements one byte position in a word, with four chips providing 2M bytes.
- Four columns implement the required 2M × 32 memory.

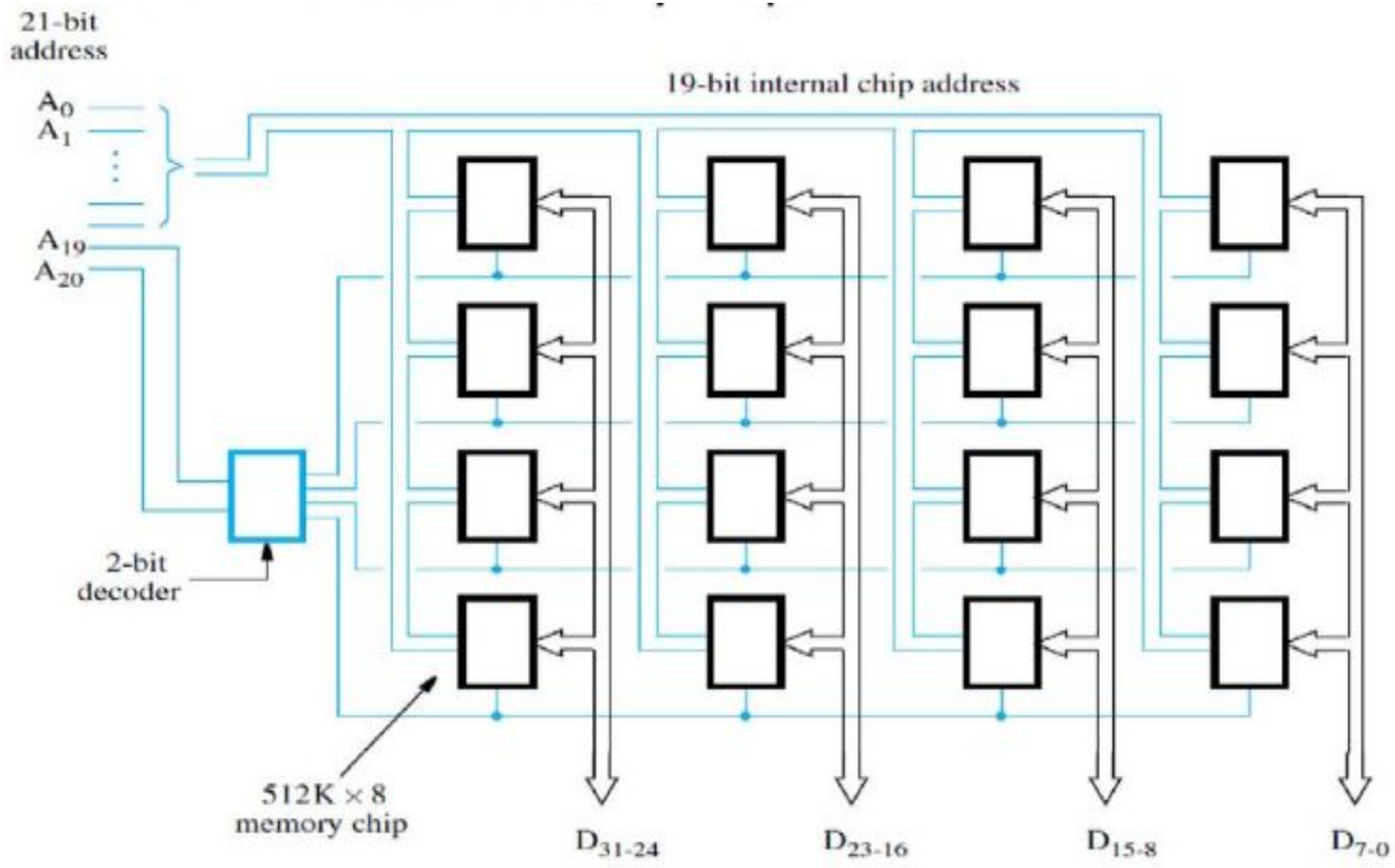
Semiconductor RAM Memories- Structure of Larger Memories

- Each chip has a control input called Chip- select.
- When this input is set to 1, it enables the chip to accept data from or to place data on its data lines.



Semiconductor RAM Memories-35 Structure of Larger Memories

Organization of a 2M × 32 memory module using 512K × 8 static memory chips.



Semiconductor RAM Memories
Structure of Larger Memories

- Only the selected chip places data on the data output line, while all other outputs are electrically disconnected from the data lines.

- 21 address bits are needed to select a 32-bit word in this memory.The high-order two bits of the address are decoded to determine which of the four rows should be selected.

- The remaining 19 address bits are used to access specific byte locations inside each chip in the selected row.

- The R/W inputs of all chips are tied together to provide a common Read/Write control line (not shown in the figure).

Semiconductor RAM Memories
Structure of Larger Memories

Dynamic Memory Systems

- Modern computers use very large memories. Even a small personal computer is likely to have at least 1G bytes of memory.
- Typical desktop computers may have 4G bytes or more of memory.
- A large memory leads to better performance, because more of the programs and data used in processing can be held in the memory, thus reducing the frequency of access to secondary storage.

Semiconductor RAM Memories

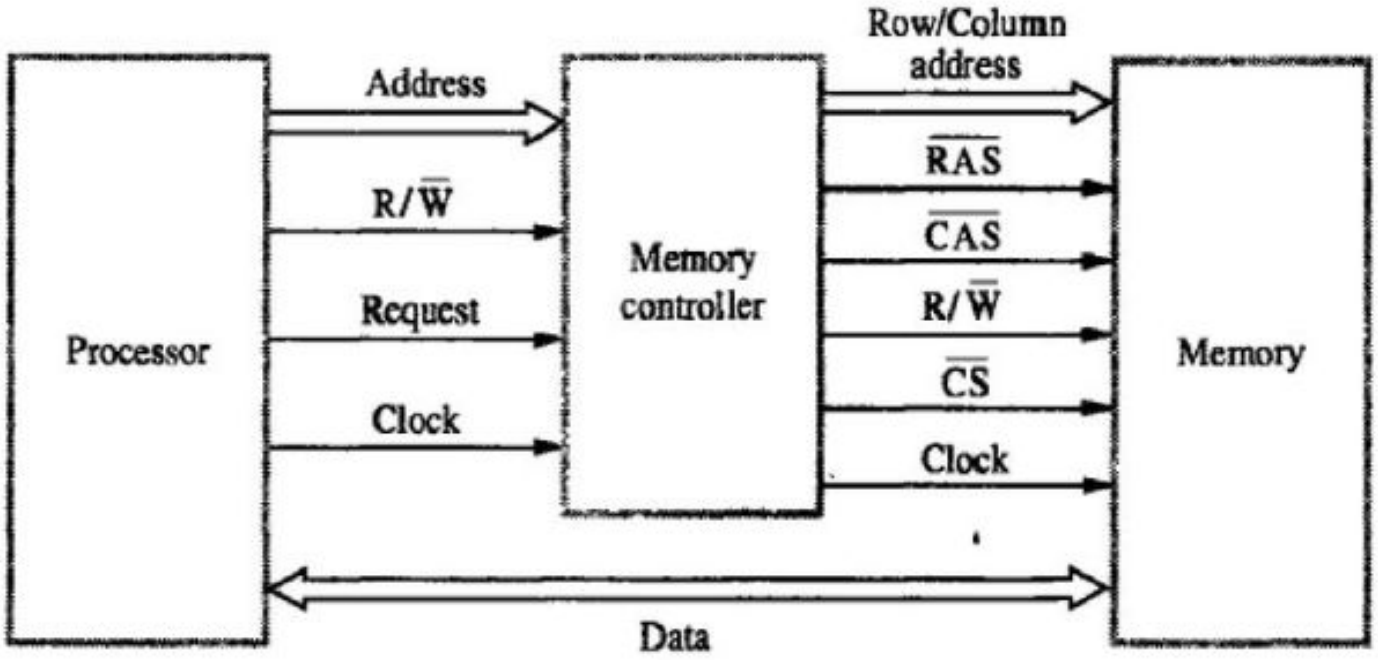
Structure of Larger Memories

Memory Controller

- The address applied to dynamic RAM chips is divided into two parts , i.e. the high-order address bits, which select a row in the cell array by activating the RAS signal.

- Then, the low-order address bits, which select a column, are provided on the same address pins and latched under control of the CAS signal.
- Since a typical processor issues all bits of an address at the same time, a multiplexer is required. This function is usually performed by a memory controller circuit.

- The controller accepts a complete address and the R/W signal from the processor, under control of a Request signal which indicates that a memory access operation is needed.
- It forwards the R/W signals and the row and column portions of the address to the memory and generates the RAS and CAS signals, with the appropriate timing.



Use of a memory controller.

Read-only Memories

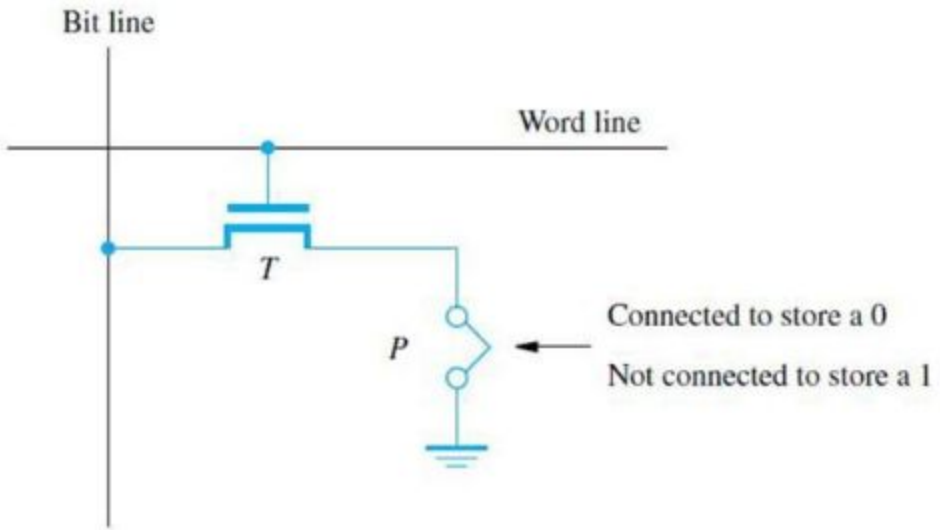
- Both static and dynamic RAM chips are volatile, which means that they retain information only while power is turned on.
- There are many applications requiring memory devices that retain the stored information when power is turned off.

- For example, need to store a small program in such a memory, to be used to start the bootstrap process of loading the operating system from a hard disk into the main memory.
- Many embedded applications do not use a hard disk and require non-volatile memories to store their software.

- Different types of non-volatile memories have been developed. But, a special writing process is needed to place the information into a non-volatile memory.
- Since its normal operation involves only reading the stored data, a memory of this type is called a read-only memory (ROM).

Read-only Memories

A memory is called a read-only memory, or ROM, when information can be written into it only once at the time of manufacture.



A ROM cell.

Read-only Memories
PROM

- Some ROM designs allow the data to be loaded by the user, thus providing a programmable ROM (PROM).

- Programmability is achieved by inserting a fuse at point P in a ROM cell.Before it is programmed, the memory contains all 0s.

- The user can insert 1s at the required locations by burning out the fuses at these locations using high-current pulses. This process is irreversible.

- PROMs provide flexibility and convenience not available with ROMs. The cost of preparing the masks needed for storing a particular information pattern makes ROMs cost effective only in large volumes.

Read-only Memories
EPROM

- It allows the stored data to be erased and new data to be written into it. Such an erasable, reprogrammable ROM is usually called an EPROM.

- EPROMs are capable of retaining stored information for a long time, they can be used in place of ROMs or PROMs while software is being developed.

- An EPROM cell has a structure similar to the ROM cell. However, the connection to ground at point P is made through a special transistor.

- The transistor is normally turned off, creating an open switch. It can be turned on by injecting charge into it that becomes trapped inside.

- By injecting the charges into it that become trapped in the transistors that form the memory cells. This can be done by exposing the chip to ultraviolet light, which erases the entire contents of the chip.

Read-only Memories
EEPROM

- An EPROM must be physically removed from the circuit for reprogramming. Also, the stored information cannot be erased selectively.

- The entire contents of the chip are erased when exposed to ultraviolet light.

- Another type of erasable PROM can be programmed, erased, and reprogrammed electrically. Such a chip is called an electrically erasable PROM, or EEPROM.

- One disadvantage of EEPROMs is that different voltages are needed for erasing, writing, and reading the stored data, which increases circuit complexity.

- However, this disadvantage is outweighed by the many advantages of EEPROMs. They have replaced EPROMs in practice.

Read-only Memories
Flash Memory

- An approach similar to EEPROM technology has given rise to flash memory devices.

- A flash cell is based on a single transistor controlled by trapped charge, much like an EEPROM cell.

- The key difference is that, in a flash device, it is only possible to write an entire block of cells. Prior to writing, the previous contents of the block are erased.

- Flash devices have greater density, which leads to higher capacity and a lower cost per bit. They require a single power supply voltage, and consume less power in their operation.

Flash Memory

Flash Cards

- One way of constructing a larger module is to mount flash chips on a small card. Flash cards with a USB interface are widely used and are commonly known as memory keys. Larger cards may hold as much as 32 Gbytes.

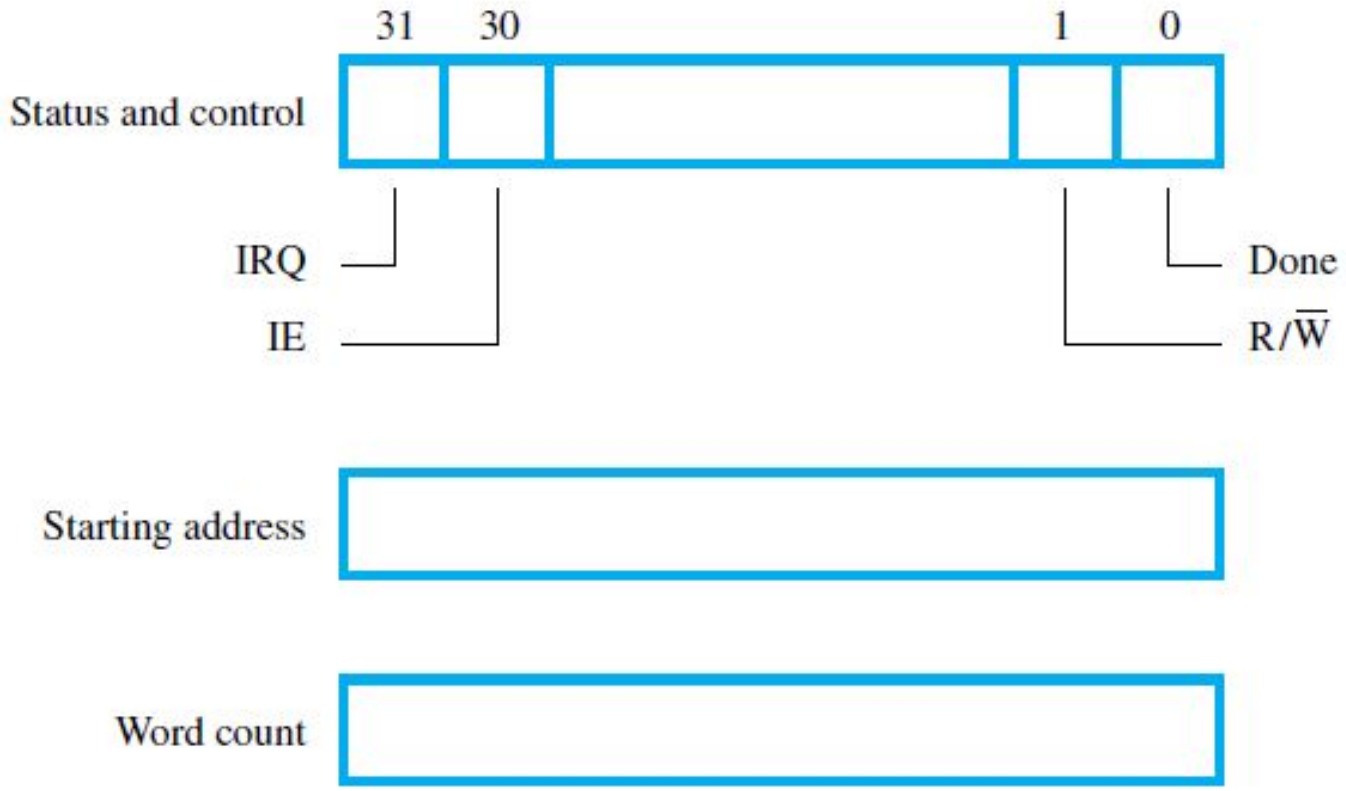
Flash Drives

- Larger flash memory modules have been developed to replace hard disk drives, and hence are called flash drives. However, the storage capacity of flash drives is significantly lower.Currently, the capacity of flash drives is on the order of 64 to 128 Gbytes.
- In contrast, hard disks have capacities exceeding a terabyte. Also, disk drives have a very low cost per bit. They have shorter access times, which result in a faster response.
- They are insensitive to vibration and they have lower power consumption, which makes them attractive for portable, battery-driven applications.

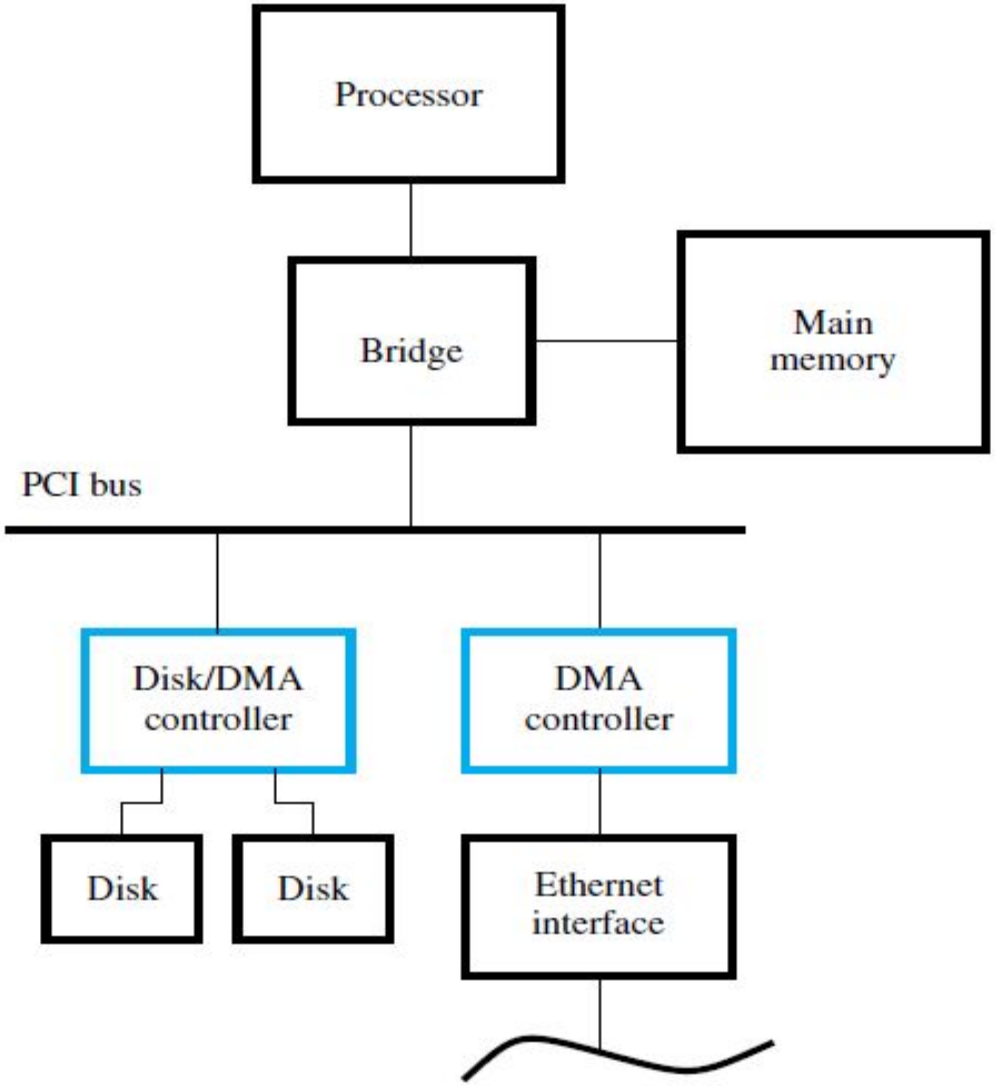
Direct memory access

- Blocks of data are often transferred between the main memory and I/O devices such as disks.
- Data are transferred from an I/O device to the memory by first reading them from the I/O device using an instruction such as Load R2, DATAIN which loads the data into a processor register.
- Data read are stored into a memory location. The reverse process takes place for transferring data from the memory to an I/O device.
- An instruction to transfer input or output data is executed only after the processor determines that the I/O device is ready, either by polling its status register or by waiting for an interrupt request.
- A special control unit is provided to manage the transfer, without continuous intervention by the processor. This approach is called *direct memory access*, or DMA.

Registers in DMA controller



DMA controllers in a computer system

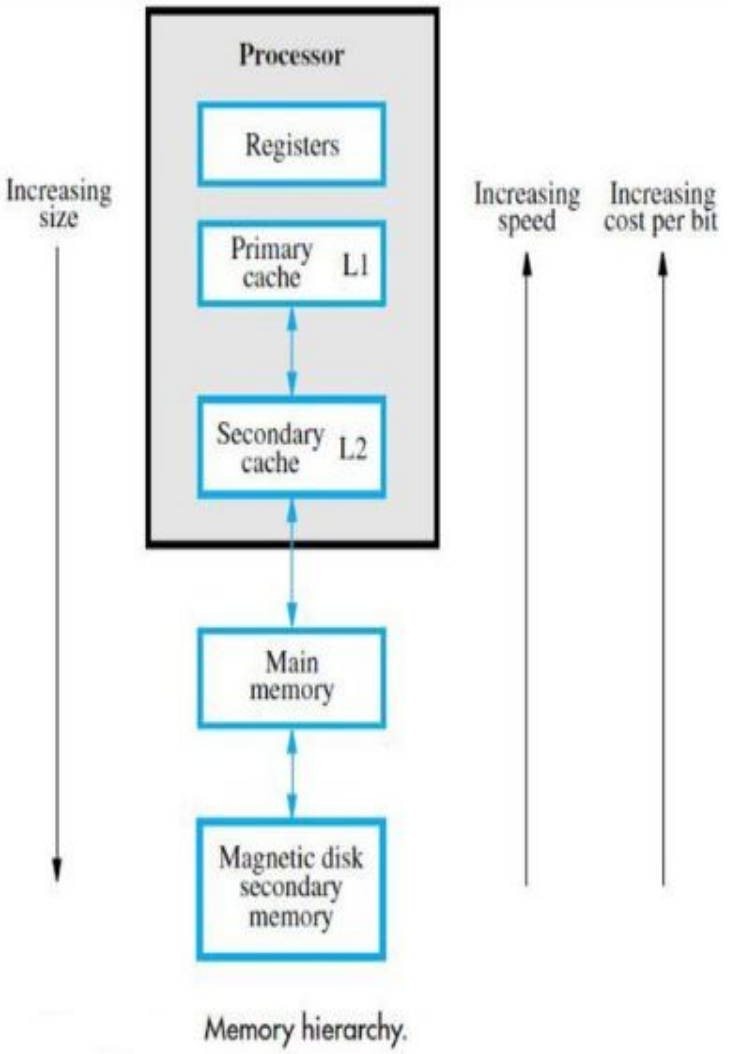


Speed, Size and Cost
Memory hierarchy

- The fastest access is to data held in processor registers. Processor cache, holds copies of the instructions and data stored in a much larger memory that is provided externally.

- A primary cache is always located on the processor chip. This cache is small and its access time is comparable to that of processor registers. The primary cache is referred to as the level 1 (L1) cache.

- A larger, and hence somewhat slower, secondary cache is placed between the primary cache and the rest of the memory. It is referred to as the level 2 (L2) cache.



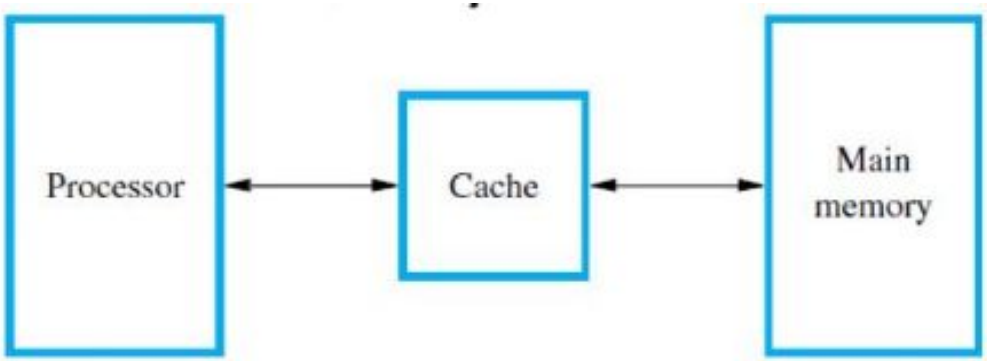
Memory hierarchy.

Cache Memories

- The memory control circuitry is designed to take advantage of the property of locality of reference.
- Temporal locality suggests that whenever an information item, instruction or data, is first needed, this item should be brought into the cache, because it is likely to be needed again soon.
- Spatial locality suggests that instead of fetching just one item from the main memory to the cache, it is useful to fetch several items that are located at adjacent addresses as well.
- The term cache block or cache line refers to a set of contiguous address locations of some size.

Cache Memories
Use of a cache memory

When the processor issues a Read request, the contents of a block of memory words containing the location specified are transferred into the cache.



Use of a cache memory.

Cache Hits

- The processor does not need to know explicitly about the existence of the cache. It simply issues R/W requests using addresses that refer to locations in the memory.

- The cache control circuitry determines whether the requested word currently exists in the cache.

- If it does, the R/W operation is performed on the appropriate cache location. In this case, a read or write hit is said to have occurred.

- The main memory is not involved when there is a cache hit in a Read/Write operation.

Cache Misses

- A Read operation for a word that is not in the cache constitutes a Read miss.
- It causes the block of words containing the requested word to be copied from the main memory into the cache.
- After the entire block is loaded into the cache, the particular word requested is forwarded to the processor.
- Alternatively, this word may be sent to the processor as soon as it is read from the main memory.
- The latter approach, which is called load-through, or early restart, reduces the processor's waiting time somewhat, at the expense of more complex circuitry.

Mapping Functions

- There are several possible methods for determining where memory blocks are placed in the cache.
- Consider a example, cache consisting of 128 blocks of 16 words each, for a total of 2048 (2K) words, and assume that the main memory is addressable by a 16-bit address.
- The main memory has 64K words, which will view as 4K blocks of 16 words each.
- For simplicity, assume that consecutive addresses refer to consecutive words.

Mapping Functions
Direct Mapping

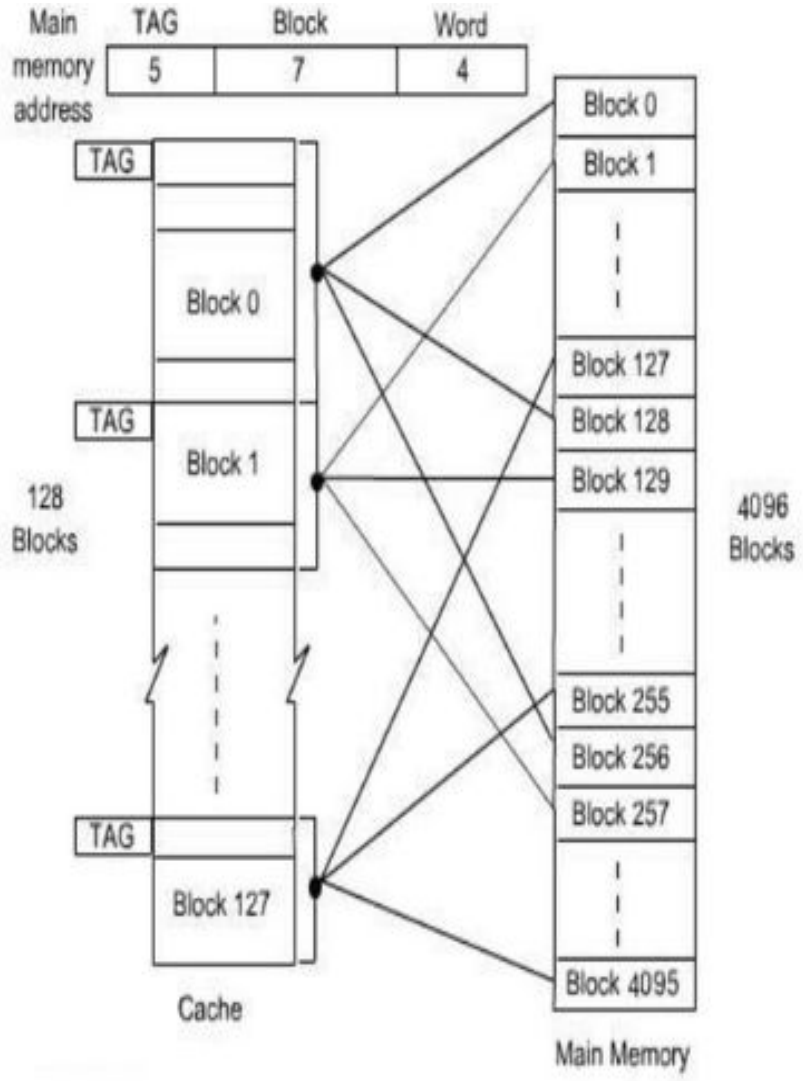
- The simplest way to determine cache locations in which to store memory blocks is the direct-mapping technique. In this technique, block j of the main memory maps onto block j modulo 128 of the cache, as shown in next slide.

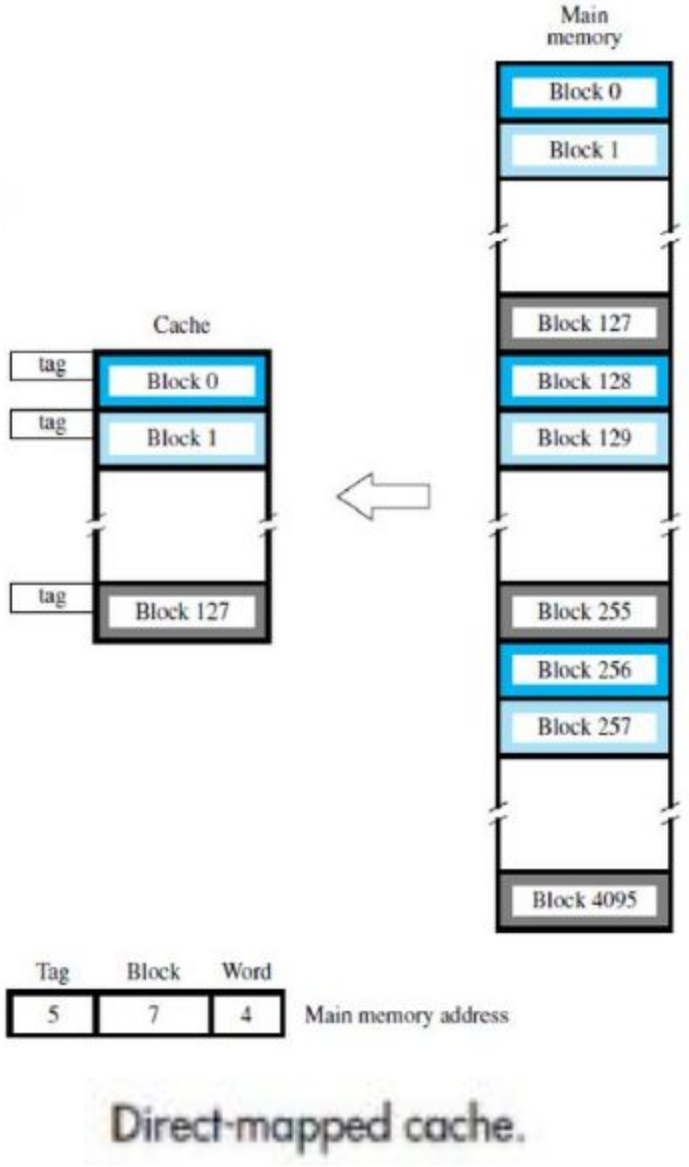
- Thus, whenever one of the main memory blocks 0, 128, 256, is loaded into the cache, it is stored in cache block 0. Blocks 1, 129, 257, are stored in cache block 1, and so on.

- Since more than one memory block is mapped onto a given cache block position, contention may arise for that position even when the cache is not full. For example, instructions of a program may start in block 1 and continue in block 129, possibly after a branch.

- As this program is executed, both of these blocks must be transferred to the block-1 position in the cache. Contention is resolved by allowing the new block to overwrite the currently resident block.

Mapping Functions





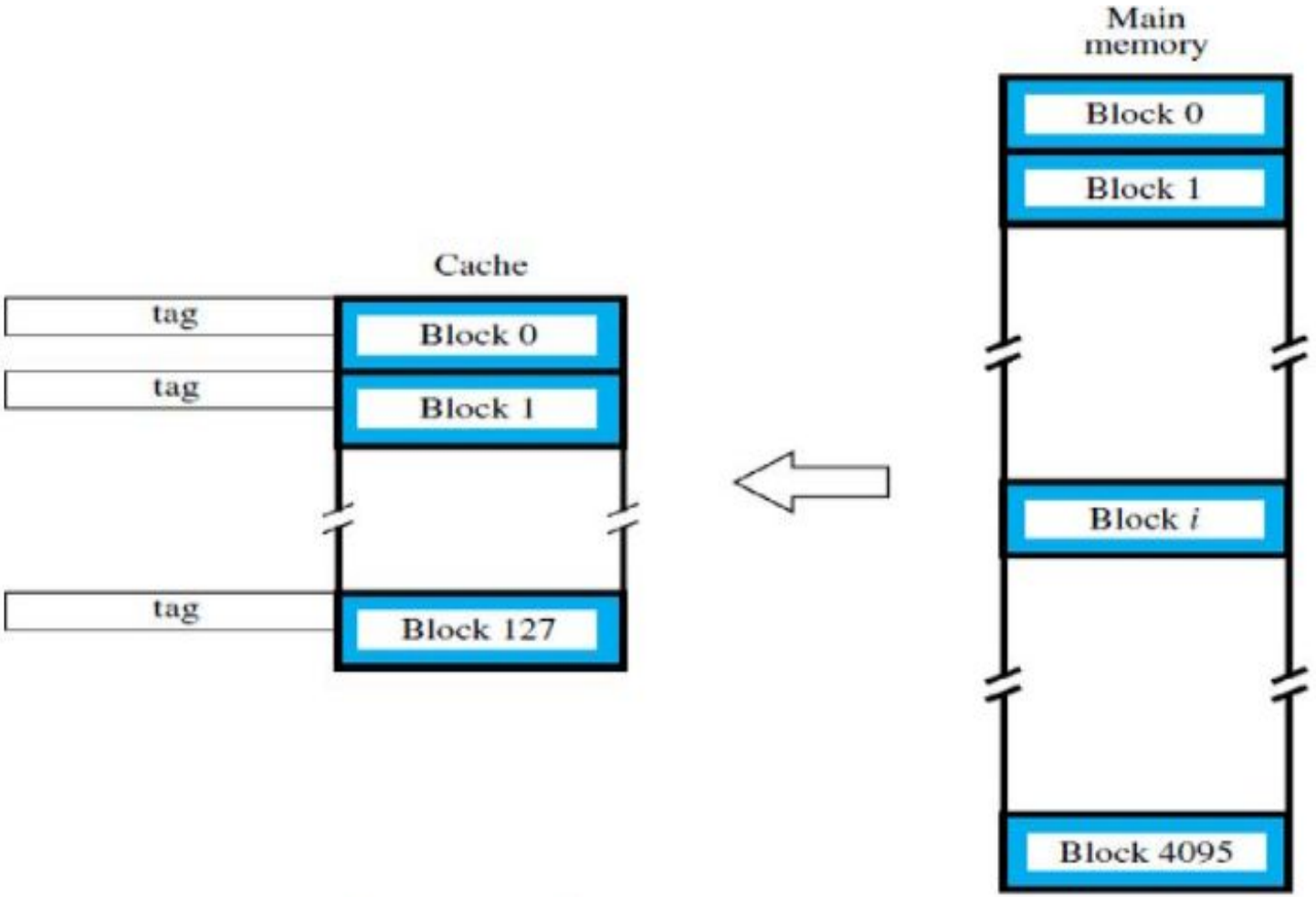
Direct-mapped cache.

Mapping Functions
Associative Mapping

- In which a main memory block can be placed into any cache block position.

- 12 tag bits are required to identify a memory block when it is resident in the cache.

- The tag bits of an address received from the processor are compared to the tag bits of each block of the cache to see if the desired block is present. This is called the associative-mapping technique.



Associative-mapped cache.

Mapping Functions
Set-Associative Mapping

- Another approach is to use a combination of the direct- and associative-mapping techniques.

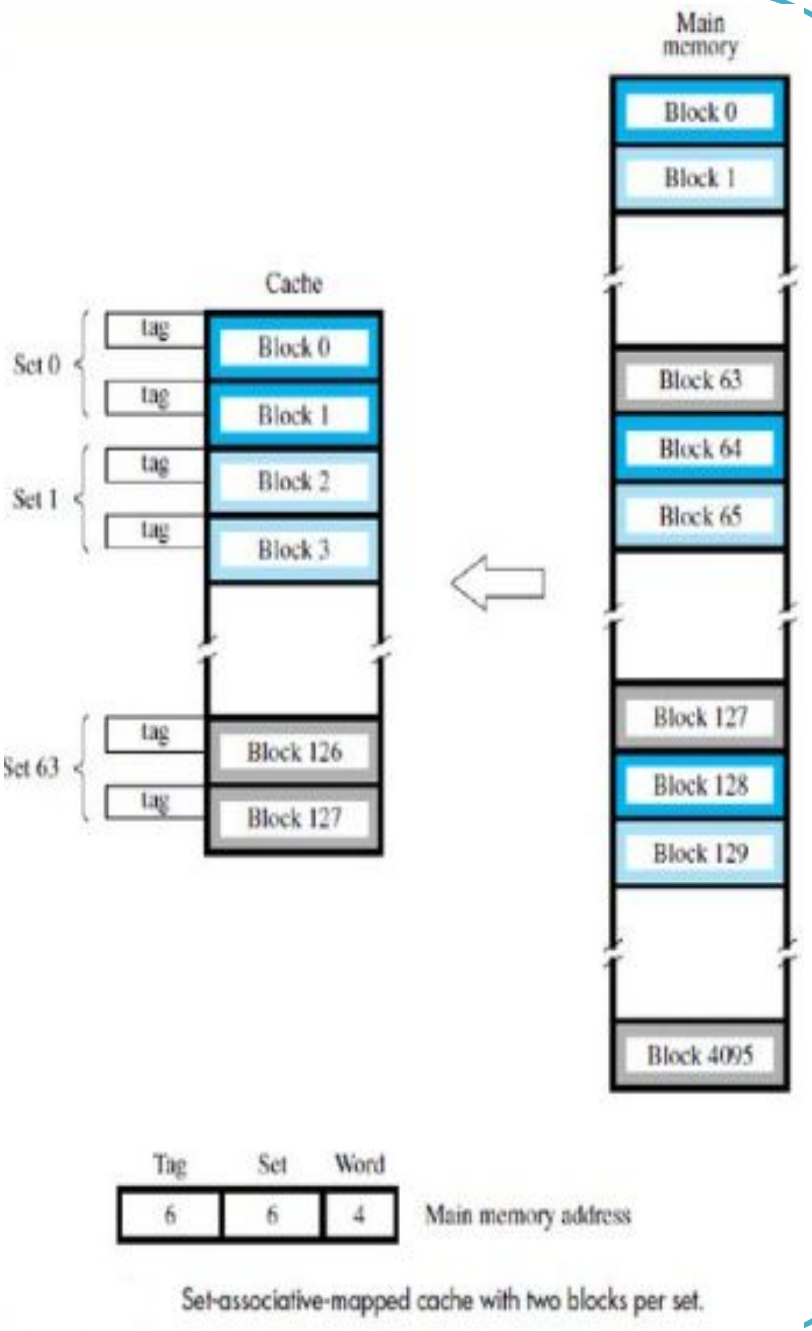
- The blocks of the cache are grouped into sets, and the mapping allows a block of the main memory to reside in any block of a specific set.

- Hence, the contention problem of the direct method is eased by having a few choices for block placement.

- At the same time, the hardware cost is reduced by decreasing the size of the associative search.

Mapping Functions

- Memory blocks 0, 64, 128, , 4032 map into cache set 0, and they can occupy either of the two block positions within this set.
- Having 64 sets means that the 6-bit set field of the address determines which set of the cache might contain the desired block.



Set-associative-mapped cache with two blocks per set.

Cache Replacement Algorithms

- Replacement algorithm determines which block in cache is removed to make room.

- 2 main policies used today

  Least Recently Used (LRU) - The block replaced is the one unused for the longest time
  Random - The block replaced is completely random – a counter-intuitive approach.

Replacement Algorithms

- No choice in Direct mapping because each block only maps to one line!!!
- So it is applicable for other mapping functions
- Hardware implemented algorithm (speed)

- Least Recently used (LRU)
  e.g. in 2 way set associative
  Which of the 2 block is LRU?
- First in first out (FIFO)
  Replace block that has been in cache longest
- Least frequently used
  Replace block which has had fewest hits
- Random

Performance Considerations

- A key design objective of a computer system is to achieve the best possible performance at the lowest possible cost.
  - Price/performance ratio is a common measure of success.

- Performance of a processor depends on:
  - How fast machine instructions can be brought into the processor for execution.
  - How fast the instructions can be executed.

- The main purpose of this hierarchy is to create a memory that the processor sees as having a short access time and a large capacity.
  - Caches improve performance is dependent on how frequently the requested instructions and data are found in the cache.

Performance Considerations

- **Miss Rate**
  - Fraction of memory references not found in cache (misses / accesses) = 1 – hit rate
  - Typical numbers (in percentages):
    - 3-10% for L1
    - Can be quite small (e.g., < 1%) for L2, depending on size, etc.
- **Hit Time**
  - Time to deliver a line in the cache to the processor
    - Includes time to determine whether the line is in the cache
  - Typical numbers:
    - 1-2 clock cycle for L1
    - 5-20 clock cycles for L2
- **Miss Penalty**
  - Additional time required because of a miss
    - typically 50-200 cycles for main memory (Trend: increasing!)

Importance of Hit Ratio

- Given:
  - h = Hit ratio
  - Ta = Average effective memory access time by CPU
  - Tc = Cache access time
  - Tm = Main memory access time

- Effective memory time is:

$$Ta = hTc + (1 - h)Tm$$

- Speedup due to the cache is:

$$Sc = Tm / Ta$$

Example:
Assume main memory access time of 100ns and cache access time of 10ns and there is a hit ratio of .9.

$$Ta = .9(10ns) + (1 - .9)(100ns) = 19ns$$
$$Sc = 100ns / 19ns = 5.26$$

Same as above only hit ratio is now .95 instead:

$$Ta = .95(10ns) + (\ )(100ns) = 14.5ns$$
$$Sc = 100ns / 14.5ns = 6.9$$

Caches on the Processor Chip

Thus, the average access time experienced by the processor in such a system is:

$$tavg = h1C1 + (1 - h1)(h2C2 + (1 - h2)M)$$

Where

h1 is the hit rate in the L1 caches.
h2 is the hit rate in the L2 cache.
C1 is the time to access information in the L1 caches.
C2 is the miss penalty to transfer information from the L2 cache to an L1 cache.
M is the miss penalty to transfer information from the main memory to the L2 cache.

Of all memory references made by the processor, the number of misses in the L2 cache is given by $(1 - h1)(1 - h2)$. If both h1 and h2 are in the 90 percent range, then the number of misses in the L2 cache will be less than one percent of all memory accesses.
This makes the value of M, and in turn the speed of the main memory, less critical.

Write buffer

Write-through:

- Each write operation involves writing to the main memory.
- If the processor has to wait for the write operation to be complete, it slows down the processor.
- Processor does not depend on the results of the write operation.
- Write buffer can be included for temporary storage of write requests.
- Processor places each write request into the buffer and continues execution.
- If a subsequent Read request references data which is still in the write buffer, then this data is referenced in the write buffer.

Write-back:

- Block is written back to the main memory when it is replaced.
- If the processor waits for this write to complete, before reading the new block, it is slowed down.
- Fast write buffer can hold the block to be written, and the new block can be read first.

Prefetching

- New data are brought into the processor when they are first needed.
- Processor has to wait before the data transfer is complete.
- Prefetch the data into the cache before they are actually needed, or a before a Read miss occurs.
- Prefetching can be accomplished through software by including a special instruction in the machine language of the processor.

  Inclusion of prefetch instructions increases the length of the programs.
- Prefetching can also be accomplished using hardware:

  Circuitry that attempts to discover patterns in memory references and then prefetches according to this pattern.

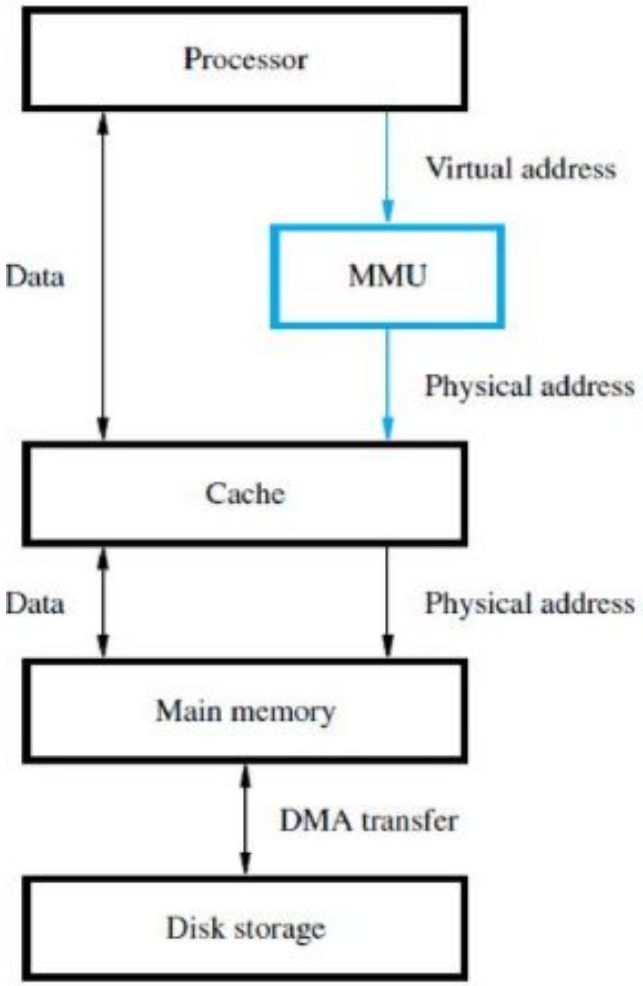
Lockup-Free Cache

- Prefetching scheme does not work if it stops other accesses to the cache until the prefetch is completed.
- A cache of this type is said to be “locked” while it services a miss.Cache structure which supports multiple outstanding misses is called a lockup free cache.
- Since only one miss can be serviced at a time, a lockup free cache must include circuits that keep track of all the outstanding misses.
- Special registers may hold the necessary information about these misses.

CACHE MEMORY	VIRTUAL MEMORY
A data storage device that includes flash memory with an integrated USB interface	A memory management technique that creates an illusion to users of a larger main memory
A storage unit - it is a hardware component	A memory management technique handled by the operating system
CPU takes more time to access the main memory. But storing the data in the cache allows the CPU to access data in a minimum time	Allows the user to execute programs that are large than the capacity of the main memory
Smaller in size	Larger in size
Faster	Slower

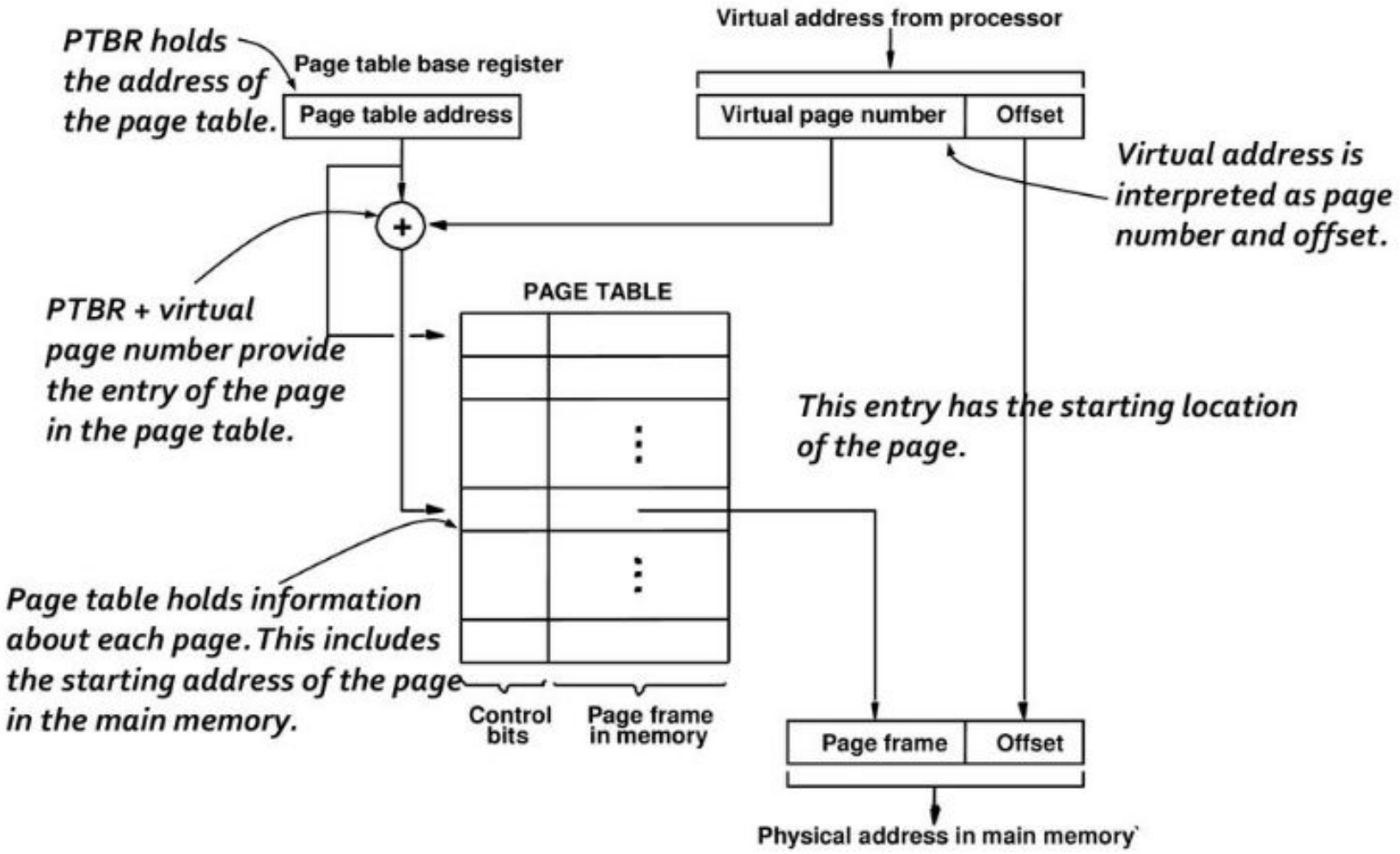
Virtual Memory

- Memory management unit (MMU) translates virtual addresses into physical addresses.
- If the desired data or instructions are in the main memory they are fetched as described previously.
- If the desired data or instructions are not in the main memory, they must be transferred from secondary storage to the main memory.
- MMU causes the operating system to bring the data from the secondary storage into the main memory



Virtual memory organization.

Address translation



Translation Lookaside Buffer

- A small cache called as Translation Lookaside Buffer (TLB) is included in the MMU.
  - TLB holds page table entries of the most recently accessed pages.

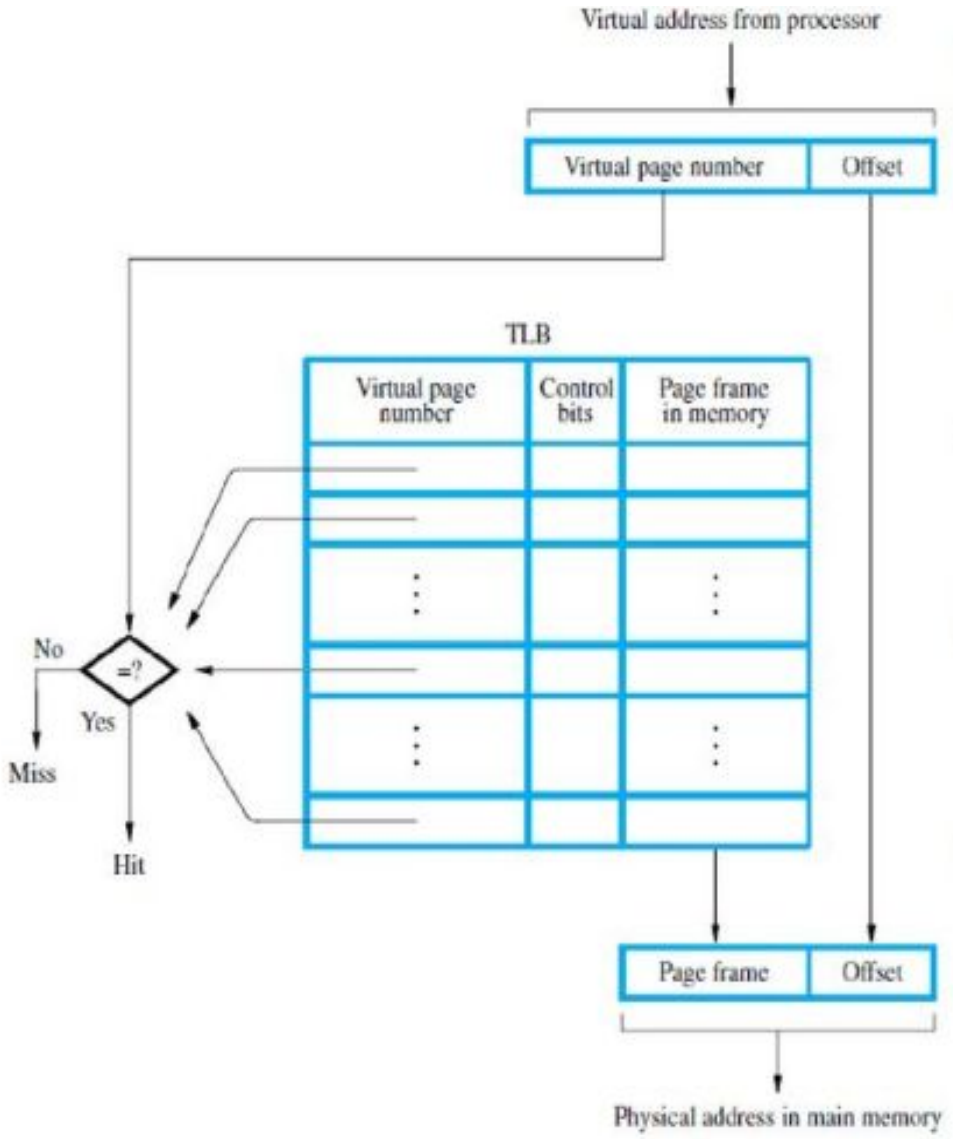
- Recall that cache memory holds most recently accessed blocks from the main memory.
  - Operation of the TLB and page table in the main memory is similar to the operation of the cache and main memory.

- Page table entry for a page includes:
  - Address of the page frame where the page resides in the main memory.
  - Some control bits.

- In addition to the above for each page, TLB must hold the virtual page number for each page.

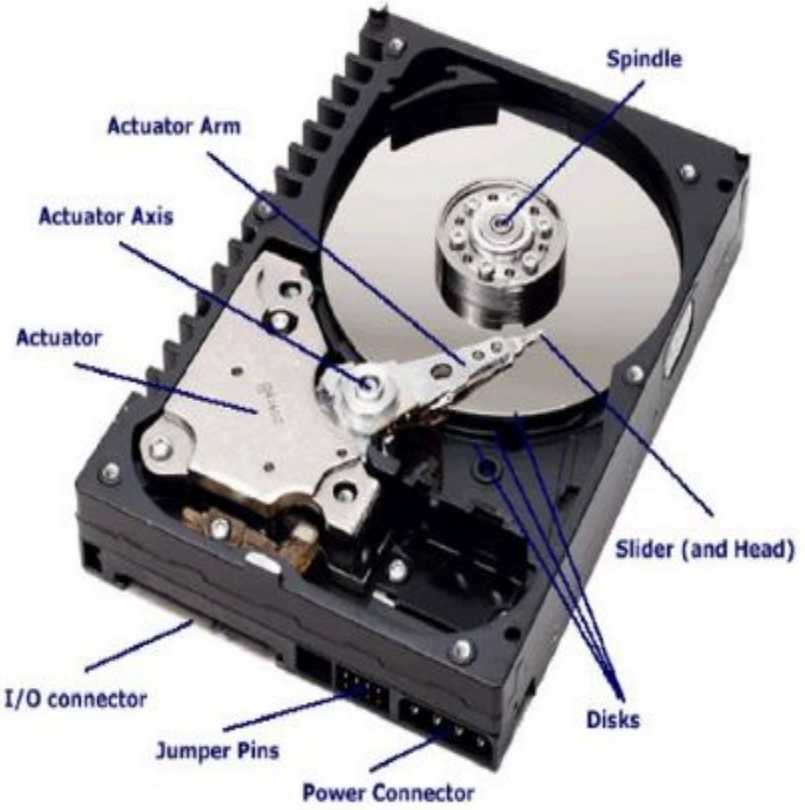
Translation Lookaside Buffer Associative-mapped

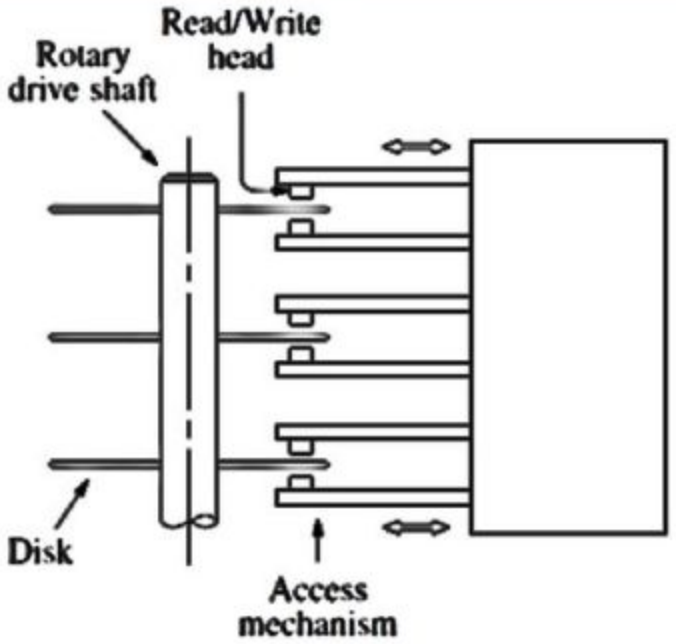
- TLBHigh-order bits of the virtual address generated by the processor select the virtual page.
- These bits are compared to the virtual page numbers in the TLB.
- If there is a match, a hit occurs and the corresponding address of the age frame is read.
- If there is no match, a miss occurs and the page table within the main memory must be consulted.
- Set-associative mapped TLBs are found in commercial processors.



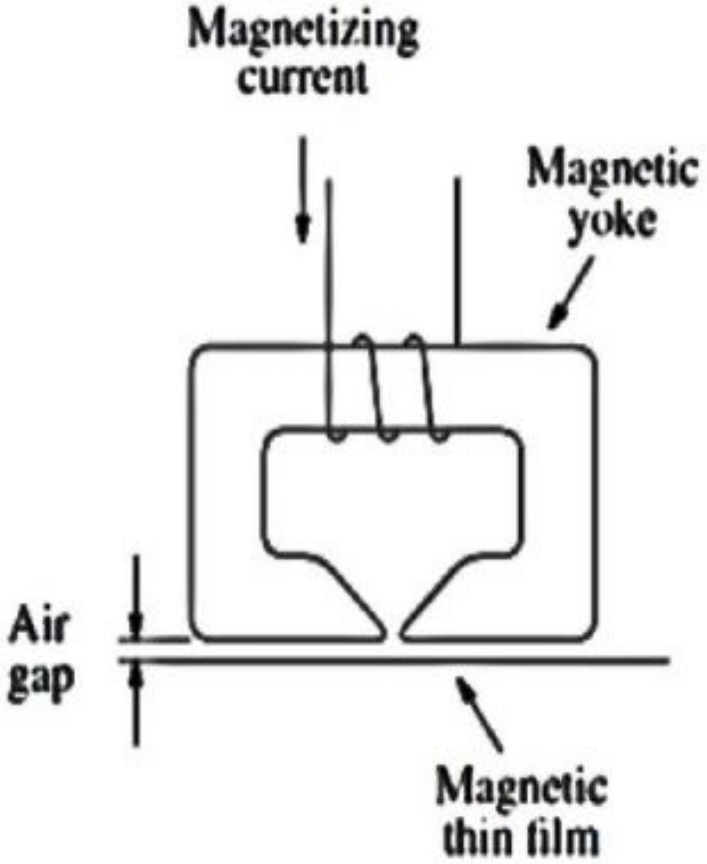
Magnetic disks

- Magnetic-disk system consists of one or more disk platters mounted on a common spindle.
- A thin magnetic film is deposited on each platter, usually on both sides.
- The assembly is placed in a drive that causes it to rotate at a constant speed.
- The magnetized surfaces move in close proximity to read/write heads.
- Data are stored on concentric tracks, and the read/write heads move radially to access different tracks.
- Platter, divided into billions of tiny areas. Each one of those areas can be independently magnetized (to store a 1) or demagnetized (to store a 0).





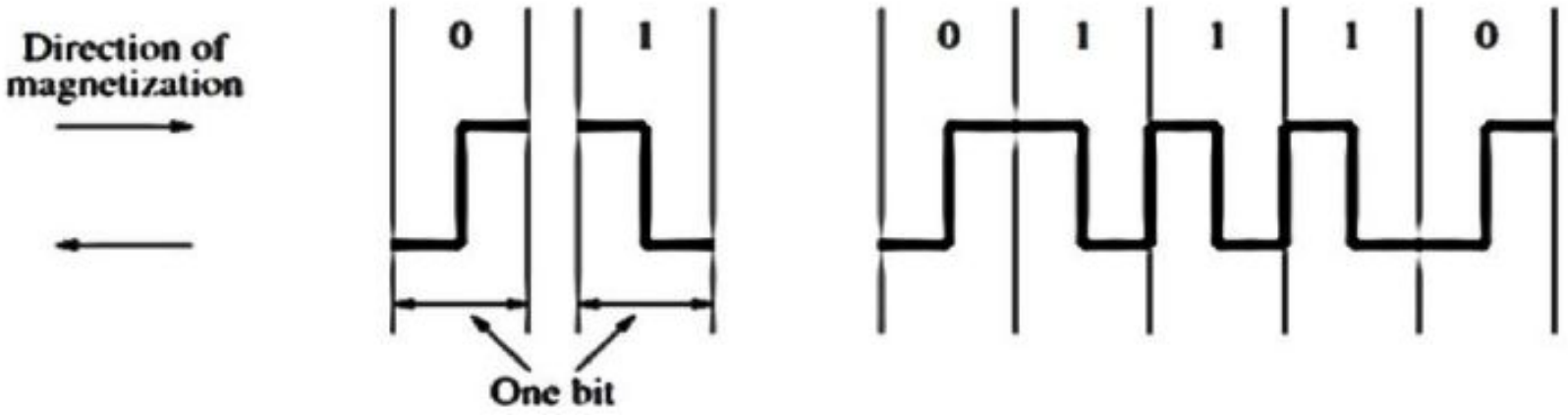
(a) Mechanical structure



(b) Read/Write head detail

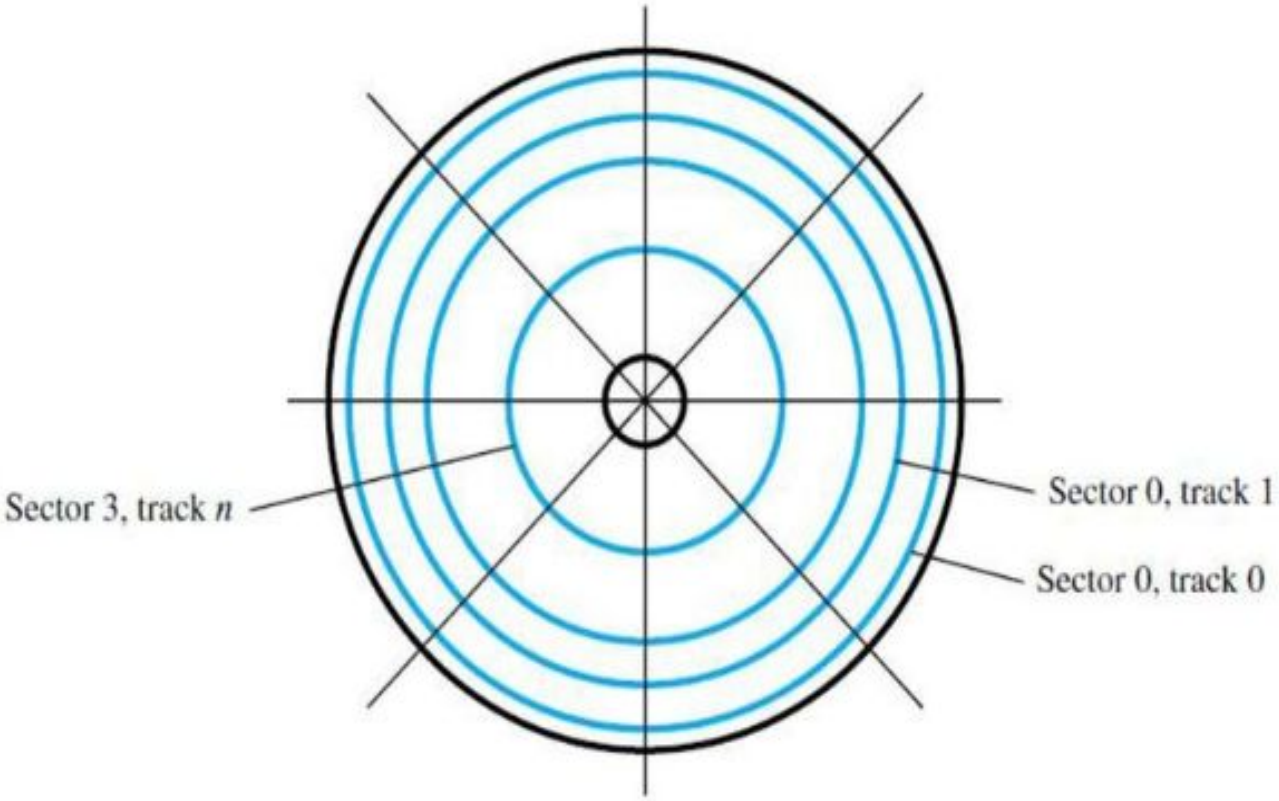
- Each read/write head consists of a magnetic yoke and a magnetizing coil.
- Digital information can be stored on the magnetic film by applying current pulses of suitable polarity to the magnetizing coil.
- This causes the magnetization of the film in the area immediately underneath the head to switch to a direction parallel to the applied field.
- For reading the stored information the magnetic field in the vicinity of the head caused by the movement of the film relative to the yoke induce a voltage in the coil, which now serves as a sense coil.
- The polarity of this voltage is monitored by the control circuitry to determine the state of magnetization of the film.

- Several different techniques have been developed for encoding. One simple scheme is *phase encoding* or *Manchester encoding*.
- Clocking information is provided by the change in magnetization at the midpoint of each bit period.
- The drawback of Manchester encoding is its poor bit-storage density.
- The space required to represent each bit must be large enough to accommodate two changes in magnetization.



(c) Bit representation by phase encoding

Organization and Accessing of Data on a Disk



Organization of one surface of a disk.

Floppy Disks

- Floppy disks are smaller, simpler, and cheaper disk units that consist of a flexible, removable, plastic diskette coated with magnetic material.
- The diskette is enclosed in a plastic jacket, which has an opening where the read/write head can be positioned.
- A hole in the centre of the diskette allows a spindle mechanism in the disk drive to position and rotate the diskette.
- The main feature of floppy disks is their low cost and shipping convenience. However, they have much smaller storage capacities, longer access times, and higher failure rates than hard disks.
- In recent years, they have largely been replaced by CDs, DVDs, and flash cards as portable storage media.

RAID Disk Arrays

- Processor speeds have increased dramatically. At the same time, access times to disk drives are still on the order of milliseconds, because of the limitations of the mechanical motion involved.

- One way to reduce access time is to use multiple disks operating in parallel. In 1988, researchers at the University of California-Berkeley proposed such a storage system. They called it RAID, for Redundant Array of Inexpensive Disks. Since all disks are now inexpensive, the acronym was later reinterpreted as Redundant Array of Independent Disks.

- Using multiple disks makes it cheaper for huge storage, and also possible to improve the reliability of the overall system.

  RAID0 – data striping
  RAID1 – identical copies of data on two disks
  RAID2, 3, 4 – increased reliability
  RAID5 – parity-based error-recovery

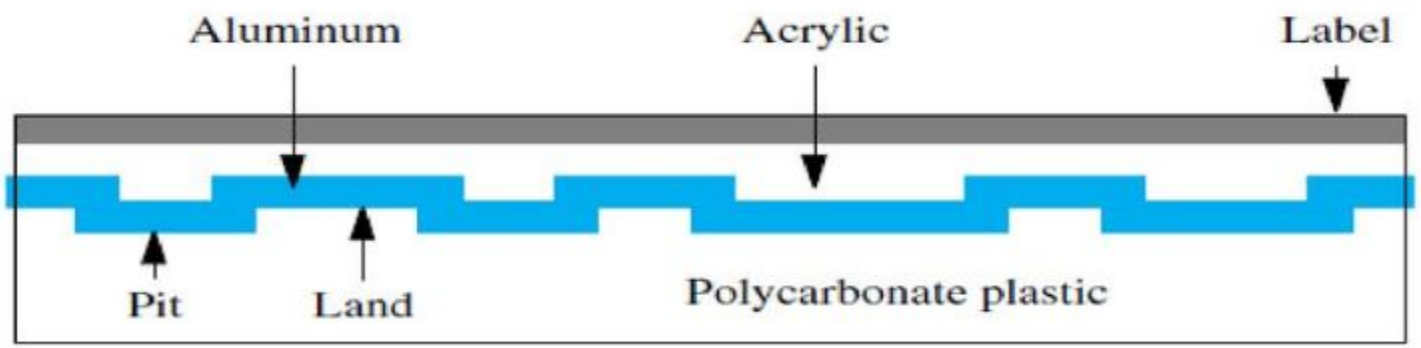
Optical Disks
CD Technology

- The optical technology that is used for CD systems makes use of the laser light focused on a very small spot. A laser beam is directed onto a spinning disk, with tiny indentations arranged to form a long spiral track on its surface.

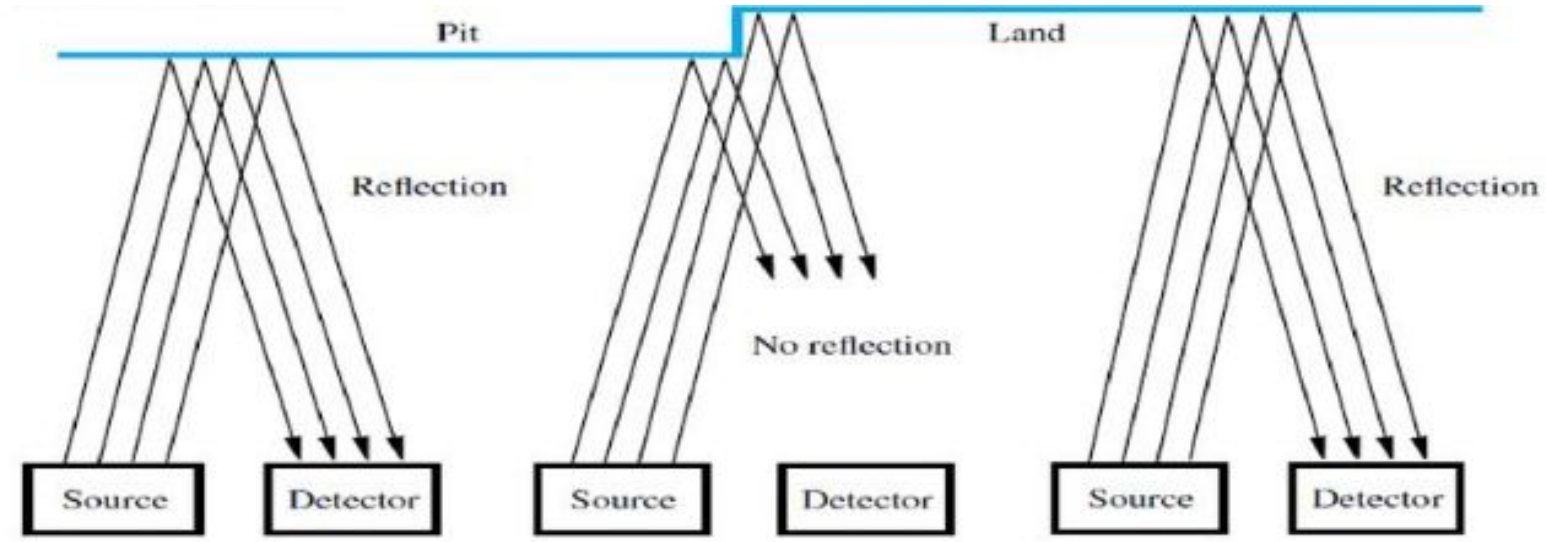
- The indentations reflect the focused beam toward a photodetector, which detects the stored binary patterns. The laser emits a coherent light beam that is sharply focused on the surface of the disk.

- Coherent light consists of synchronized waves that have the same wavelength. If a coherent light beam is combined with another beam of the same kind, and the two beams are in phase, the result is a brighter beam (bright spot).

- If the waves of the two beams are 180 degrees out of phase, they cancel each other (dark spot).Thus, a photodetector can be used to detect the beams.



(a) Cross-section



(b) Transition from pit to land

CD-ROM

- Stored data are organized on CD-ROM tracks in the form of blocks called sectors. There are several different formats for a sector. One format, known as Mode 1, uses byte sectors, 16-byte header to detect the beginning of the sector and addressing information. Followed by 2048 bytes of stored data and at the end of the sector, 288 bytes used for error-correcting scheme.

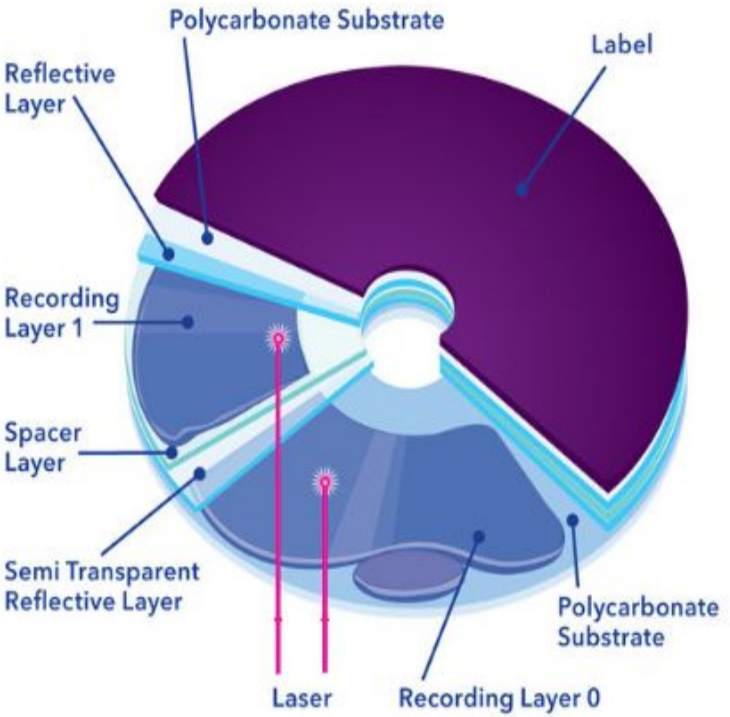
- With the Mode 1 format, a CD-ROM has a storage capacity of about 650 Mbytes. Error detection and correction is done at more than one level.

- Each byte of information stored on a CD is encoded using a 14-bit code that has some error-correcting capability.

- The basic speed of CD-ROM drives is 1X, means 75 sectors per second. This provides a data rate of 153,600 bytes/s (150Kbytes/s), using the Mode 1 format.

DVD (Digital Versatile Disk) Technology

- Its storage capacity is made much larger than that of CDs by several design changes:
- A red-light laser with a wavelength of 635 nm is used instead of the infrared light laser used in CDs, which has a wavelength of 780 nm.
- The shorter wavelength makes it possible to focus the light to a smaller spot.Pits are smaller, having a minimum length of 0.4 micron.
- Tracks are placed closer together; the distance between tracks is 0.74 micron.
- Using these improvements leads to a DVD capacity of 4.7 Gbytes (DVD-5 standard).



Magnetic Tape Systems

- Magnetic-tape recording uses the same principle as magnetic disks. The main difference is that the magnetic film is deposited on a very thin 0.5- or inch wide plastic tape.

- Seven or nine bits (corresponding to one character) are recorded in parallel across the width of the tape, perpendicular to the direction of motion.

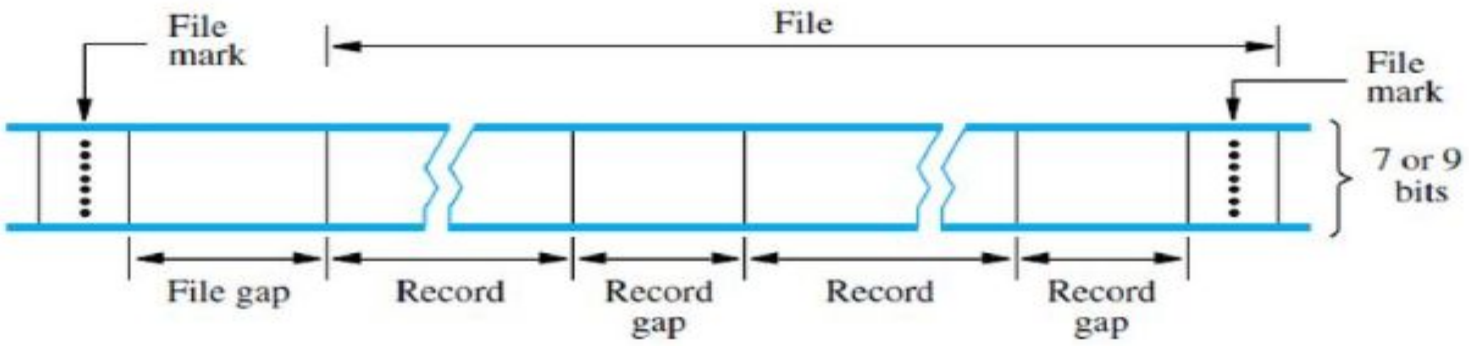
- A separate read/write head is provided for each bit position on the tape, so that all bits of a character can be read or written in parallel.

Magnetic Tape Systems

- Data on the tape are organized in the form of records separated by gaps. Tape motion is stopped only when a record gap is underneath the read/write heads. The record gaps are long enough to allow the tape to attain its normal speed before the beginning of the next record is reached. If a coding scheme used for recording data on the tape, record gaps are identified as areas where there is no change in magnetization.

- This allows record gaps to be detected independently of the recorded data. To help users organize large amounts of data, a group of related records is called a file. The beginning of a file is identified by a file mark. The file mark is a special single- or multiple-character record, usually preceded by a gap longer than the inter-record gap.

- The first record following a file mark can be used as a header or identifier for the file. This allows the user to search a tape containing a large number of files for a particular file.



Organization of data on magnetic tape.