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Course Code: CS
Semester: IV

OPERATING SYSTEMS LABORATORY

Course Objective:

This course will help the learner to explore inter-process communication mechanisms and simulate CPU, file and Disk scheduling algorithms and to implement memory management techniques

1. Creation of a child process using fork system call and communication between parent and child using pipe.
2. Simulation of IPC through shared memory and message queues.
3. Simulation of CPU scheduling algorithms and analyzing their performances.
4. Simulation of thread scheduling approaches.
5. Implementing the solution for Producer-Consumer problem for the bounded and unbounded buffer variants.
6. Implementing the solution for Reader-Writer problem based on reader priority and writer priority approaches.
7. Simulation of Banker's algorithm for Deadlock Avoidance.
8. Simulation of Deadlock Detection.
9. Implementing a solution to resolve the Dining Philosopher's problem.
10. Simulation of memory allocation schemes based on dynamic partitioning with placement algorithms and buddy systems.
11. Simulation of page replacement algorithms.
12. Implementing the address translation mechanism under paging.

COURSE LEARNING OUTCOMES

- Upon successful completion of this course, the learner will be able to
- Create parent and child processes.
- Implement sender-receiver processes that carry out IPC using shared memory and message queue.
- Demonstrate CPU scheduling algorithms and compare their performance.
- Illustrate thread scheduling approaches.
- Implement the solution for classic problems for synchronization using semaphore.
- Analyze the two deadlock solutions.
- Compare the memory partitioning and allocation techniques.