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Course Code: CS E212
Semester: III

COMPUTER ORGANIZATION & ARCHITECTURE

Course Objective:

This course will help the learner to understand the basic digital logic circuits, computer architecture, the memory system and Input / Output organization of a computer system.

UNIT - I **15 Periods**

Basics in Boolean logic and Combinational/Sequential Circuits: Digital Computers - Logic Gates - Boolean Algebra - Map Simplification - Combinational Circuits - Flip-Flop - Sequential Circuits. **Functional blocks of a computer:** CPU, memory, input-output subsystems, control unit. **Data representation:** Signed number representation, fixed and floating point representations, character representation. **Computer arithmetic:** Addition and Subtraction of Signed Numbers - Design of Fast Adders - Multiplication of Unsigned Numbers - Multiplication of Signed Numbers - Fast Multiplication - Integer Division - Floating-Point Numbers and Operations, IEEE 754 format.

UNIT - II **15 Periods**

Instruction set architecture of a CPU: Memory Locations and Addresses - Memory Operations - Instructions and Instruction Sequencing - Addressing Modes - Assembly Language - Stacks - Subroutines - Additional Instructions - CISC Instruction Sets. **Introduction to x86 architecture:** The Intel IA-32 Architecture: Memory Organization - Register Structure - Addressing Modes – Instruction Set – Interrupts and Exceptions.

UNIT - III **15 Periods**

CPU control unit design: Instruction Codes - Computer Registers - Computer Instructions - Timing and Control - Instruction Cycle - Memory-Reference Instructions - Input-Output and Interrupt - Design of Basic Computer - Design of Accumulator Logic. **Microprogrammed Control:** Control Memory - Address Sequencing- Microprogram Example - Design of Control Unit. **Pipelining:** Basic Concept - Pipeline Organization - Pipelining Issues - Data Dependencies - Memory Delays- Branch Delays - Superscalar Operation - Pipelining in CISC Processors. **Parallel Processors:** Hardware Multithreading - Vector (SIMD) Processing - Cache Coherence

UNIT - IV **15 Periods**

Memory system: Basic Concepts - Semiconductor RAM Memories - Read-only Memories - Direct Memory Access - Memory Hierarchy - Cache Memories - Performance Considerations - Virtual Memory - Memory Management Requirements - Secondary Storage. **Basic Input/Output:** Accessing I/O Devices - Interrupts. **Input / Output Organization:** Bus Structure - Bus Operation – Arbitration - Interface Circuits - Interconnection Standards

TEXTBOOKS

1. M. M. Mano, Computer System Architecture, Prentice Hall of India, 3rd Edition, 2007.
2. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann publishers, 5th Edition, 2014.
3. Carl Hamacher, Zvonko Vranesic, Safwat Zaky,Naraig Manjikian**,** Computer Organization and Embedded Systems, McGraw Hill, 5th Edition, 2012.

REFERENCES

1. John P. Hayes, Computer Architecture and Organization, McGraw-Hill, 2nd Edition, 1998.
2. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson India, 11th Edition, 2019.

UNITWISE LEARNING OUTCOMES

Upon successful completion of each unit, the learner will be able to

Unit I	• Describe the background for understanding the digital circuits • Illustrates various data types represented in binary form and presents arithmetic algorithms
Unit II	• Discuss the concepts of machine instructions, addressing techniques, and instruction sequencing and explores the X86 architecture
Unit III	• Presents the organization and design of a basic digital computer and discuss the microprogramming concepts
Unit IV	• Describe the memory hierarchy and explain the operation of cache memory • Explain the techniques that computers use to communicate with input and output devices

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