

BANDGAP REFERENCE CIRCUIT

Contents

Theory

1. Introduction to BGR
2. Need of BGR
3. BGR working Principle
4. CTAT Voltage Generation
5. PTAT Voltage generation
6. Self Biased Cascode Current Mirror
7. Reference Voltage Circuit
8. Startup Circuit
9. Overview of BGR

Lab Report

Saptarshi Ghosh

Introduction to BGR

Bandgap Reference circuit are PVT independent Voltage Reference circuits used in Integrated Circuits. It produces a constant output voltage of 1.2 which is equivalent the energy bandgap of the silicon at 0 Kelvin. Many analog subsystem and digital subsystem require power supply from LDOs. The reference Voltage of the LDOs Vref is provided by this BGR. Components like ADC, DAC, BUCK converters also require Vref. The applications of BGR circuits are:

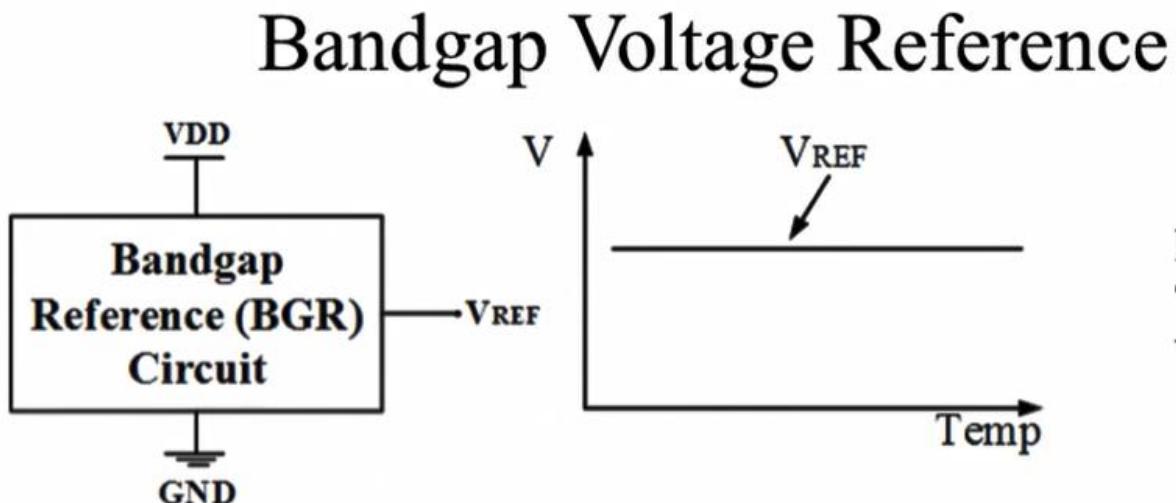
The applications of the BGR circuit are:

- Low Dropout Regulators
- Analog to Digital Converters
- Digital to Analog Converters
- DC to DC Buck converters

Application wise BGR can be categorized as:-

- Low Voltage BGR
- Low Power BGR
- High PSRR and low noise BGR
- Curvature compensated BGR.

The typical diagram of BGR is shown below:-



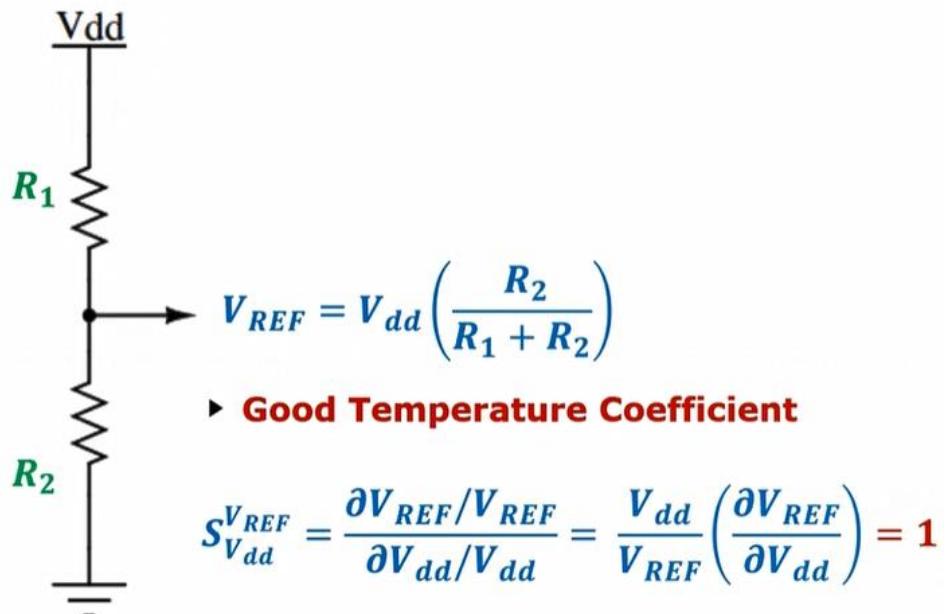
Need of BGR

The Vref circuit can be implemented by

- Voltage divider circuit
- Forward biased PN junction
- Base Emitter Voltage Referenced circuit
- A voltage referenced IC using Zener diode

➤ **Voltage Divider Circuit:**

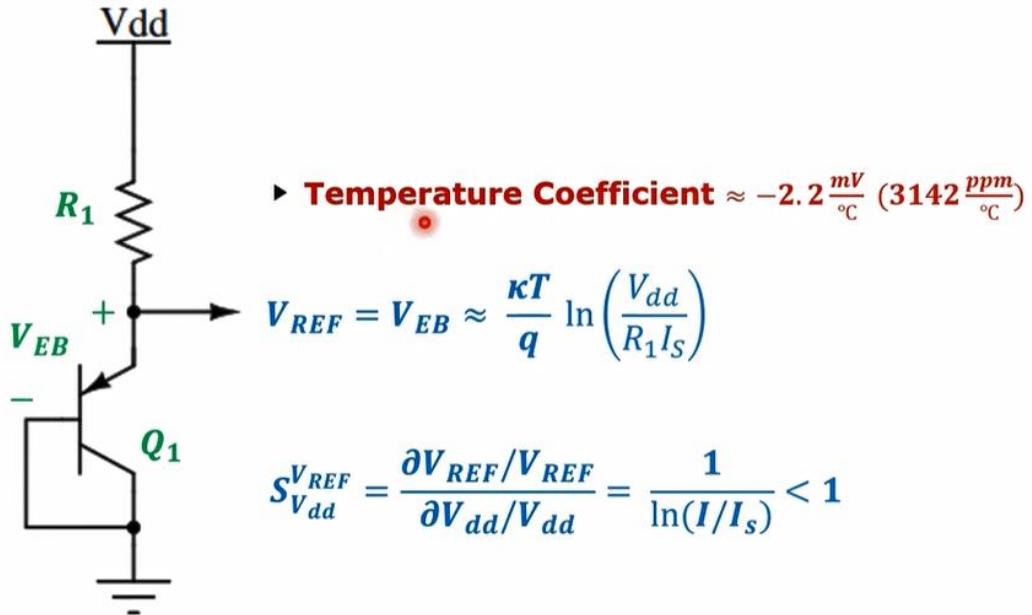
Voltage Divider



The main drawback of this voltage divider circuit is the vref changes with vdd. According to the above equation with change in 10% of vdd vref changes by 10%. It has a good temperature coefficient but very undesirable power supply rejection ratio.

➤ **Forward Biased PN junction**

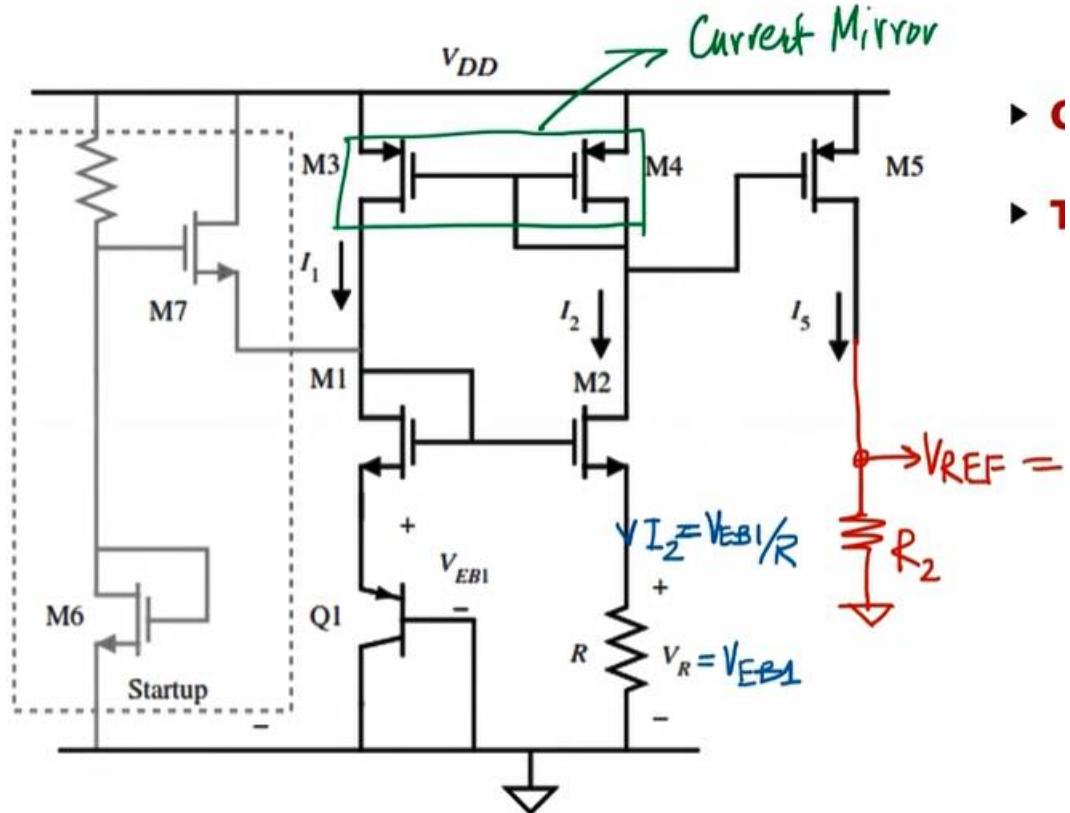
Forward-biased pn Junction



In this circuit the biasing current is more than the saturation current due to which the sensitivity is better than voltage divider but the power supply rejection ratio value is far away from 40-60dB.

Base Emitter Voltage Reference circuit

► Base-Emitter Voltage-Referenced Circuit



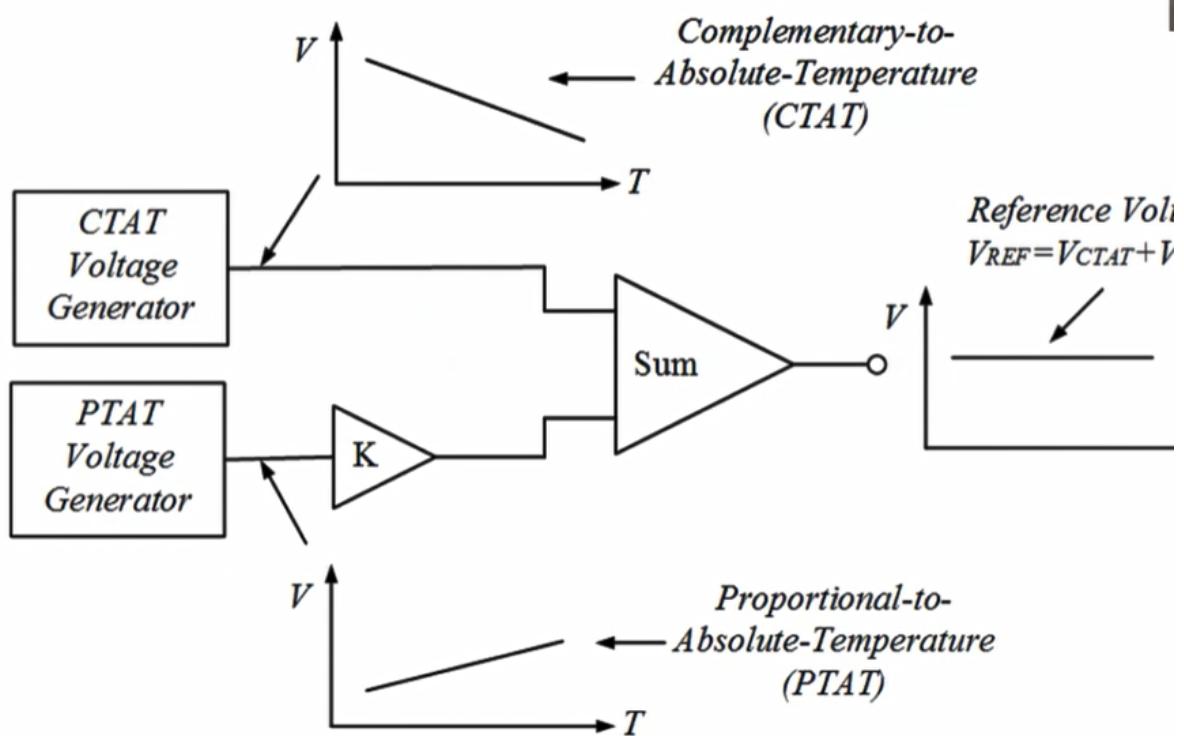
Because of the current mirror the Power supply rejection ratio is good but the temperature coefficient of 2333ppm/degree celcius is dominated by the Q1 BJT.

Voltage Referenced IC using Zener diode.

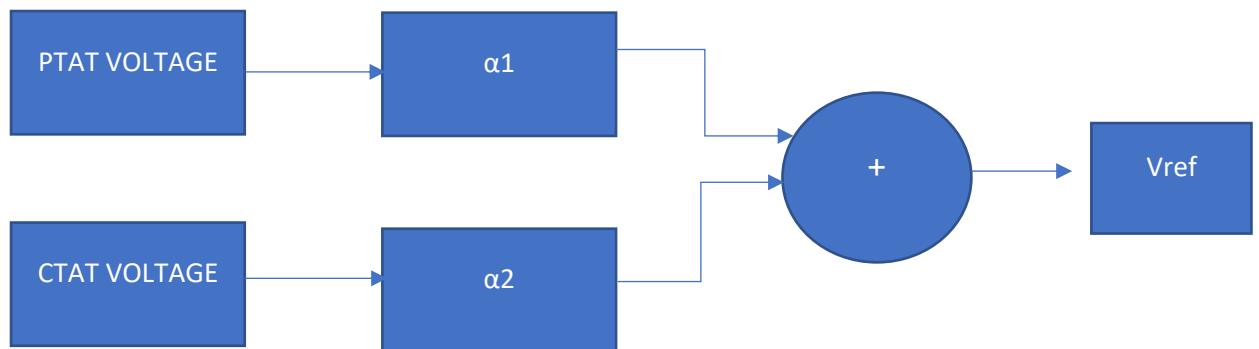
The drawback are that these discrete components and for their connections in the circuit they require additional components like high frequency filtering circuits which are noisy. A low voltage Zener diode is difficult to get in the market.

Hence solution is to implement the BGR which can be integrated in Bulk CMOS, Bi CMOS or Bipolar technologies without the use of any external components

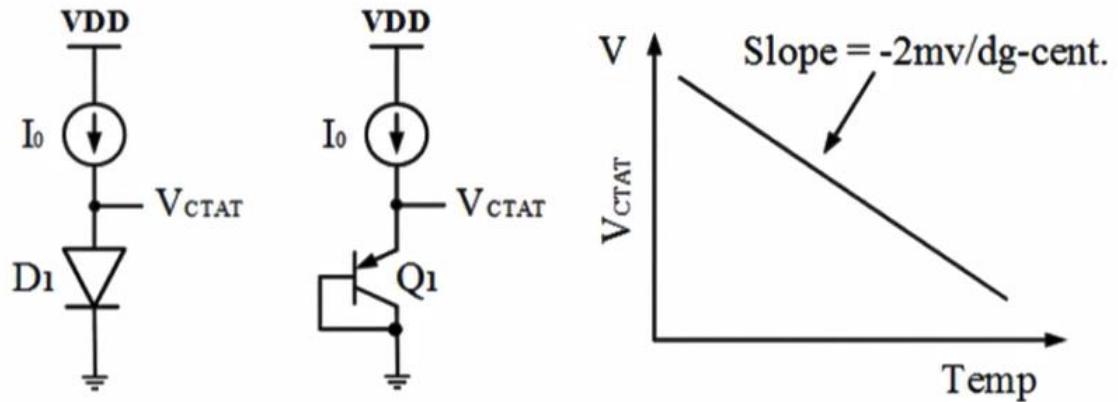
BGR working principle



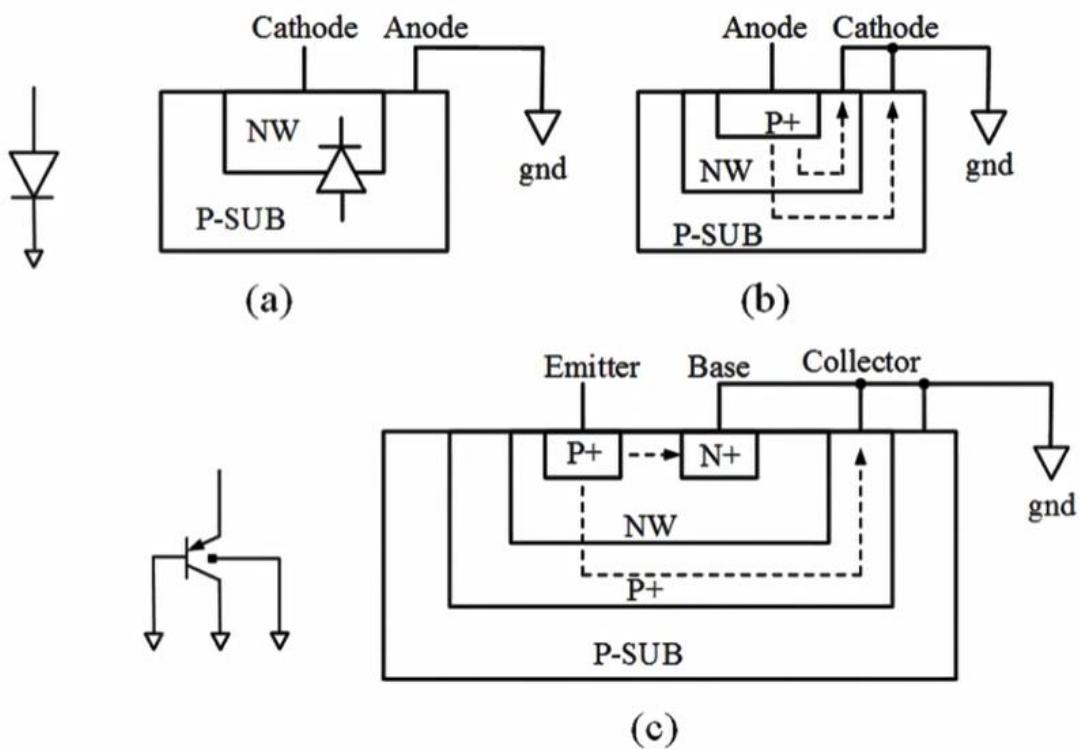
The V_{be} voltage is generated by supplying a constant current through a BJT whose collector and base are shorted. The voltage drops by 2.2mv/degree celcius. Similarly the V_t is generated by supplying two different current densities to the anode of two diodes respectively and difference of that two voltage is taken into account. The voltage produced has a positive slope and is amplified by M times or K times such that all the linear terms should get eliminated and higher order terms should be present and we get a constant voltage at the output. But if the CTAT voltage is more negative such that adding it with amplified value of PTAT voltage we may not get a constat V_{ref} . For that sometimes CTAT voltage value has to be positively amplified such that both the value almost cancels each other and the graph becomes constant as explained in the following diagram:



CTAT Voltage generation



Based on the above circuit the, the constant current is fed through the anode section of the diode. When the current will flow the voltage across the diode will drop by 2.2mv/dg-cent.



According to the first diagram, it is the very basic way to implement a PN junction diode. But in normal circuits the p substrate is always fixed to 0 in a CMOS process. So we cannot use the first topology. According to the second diagram if the P+ implant is present in the nwell which is for the emitter and N+ which will be present for the collector. Now if there is a small base current it will generate huge collector current of value βI_b . This current will go in small amount towards the cathode but huge current it will get pass through the P substrate and effect other implants in it. Hence to avoid this the P+ layer is made inside the Psubstrate such that the huge current which is getting generated should pass through the P+ layer and finally to the collector.

Next with increasing value of transistor unit and value of current the slope will change which will be explained in the lab report.

The calculation of the slope of the graph shown in figure 7 can be deduced from the below calculations.

The diode current can be written as:-

$$I_D = I_S e^{\frac{V_D}{V_t}}$$

The diode voltage from the equation is :-

$$V_D = V_t \ln\left(\frac{I_0}{I_S}\right)$$

The dependancies of I_s and V_t with mobility and temperature can be explained below:-

$$V_t = \frac{kT}{q}$$

$$I_S = A \mu k T n_i^2$$

$$\mu \propto \mu_0 T^m, m = -3/2$$

$$n_i^2 \propto T^3 e^{\left[\frac{-E_g}{kT} \right]}$$

$$I_S = A T^{(4+m)} e^{\left[\frac{-E_g}{kT} \right]}$$

The final equation can be obtained by the below calculation:-

$$\begin{aligned}
 \frac{\partial V_T}{\partial T} &= \frac{V}{T} \quad \text{--- (2)} \\
 V_D &= V_F \ln \frac{I_0}{I_S} \quad \text{--- (1).} \quad (CTAT) \\
 I_S &= T^{-b} \exp \left[\frac{-E_g}{kT} \right] \\
 \text{By } I_S &\propto b T^{(4+m)} \exp \left[\frac{-E_g}{kT} \right] \quad \text{--- (3),} \\
 \frac{\partial I_S}{\partial T} &= b \left[T^{(4+m)} \exp \left[\frac{-E_g}{kT} \right] \times \frac{E_g}{kT^2} + \right. \\
 &\quad \left. T^{(4+m)-1} \exp \left[\frac{-E_g}{kT} \right] \right] \\
 &= b \left[\exp \left[\frac{-E_g}{kT} \right] \left[T^{(4+m)} \frac{E_g}{kT^2} + (4+m) T^{(3+m)} \right] \right] \\
 &= b \left[\exp \left[\frac{-E_g}{kT} \right] T^{(4+m)} \left[\frac{E_g}{kT^2} + \frac{(4+m)}{T} \right] \right] \\
 \frac{\partial I_L}{\partial T} &= I_S \left[\frac{E_g}{kT^2} + \frac{(4+m)}{T} \right] \quad \text{--- (4).} \\
 \text{Now from (1)} \\
 \frac{\partial V_D}{\partial T} &= \frac{\partial V_T}{\partial T} \cdot \ln \frac{I_0}{I_S} + V_T \frac{\partial}{\partial T} \left(\ln \frac{I_0}{I_S} \right) \\
 &= \frac{\partial V_T}{\partial T} \ln \frac{I_0}{I_S} + V_T \cdot \frac{1}{I_S} \cdot \frac{\partial I_S}{\partial T} = \frac{I_0}{I_S} \cdot \frac{\partial I_S}{\partial T} \\
 \frac{\partial V_D}{\partial T} &= \frac{\partial V_T}{\partial T} \cdot \ln \left(\frac{I_0}{I_S} \right) - V_T \cdot \frac{1}{I_S} \cdot \frac{\partial I_S}{\partial T} \\
 &= \frac{V}{T} \ln \frac{I_0}{I_S} - \frac{V_T}{I_S} \left[I_S \left(\frac{(4+m)}{T} \right) + \frac{E_g}{kT} \right]
 \end{aligned}$$

$$\frac{\partial V_D}{\partial T} = \frac{V_T}{T} \ln \frac{V_D}{V_t} - \frac{V_t}{T} (4+m) - V_T \frac{Eg}{kT^2}$$

$$\frac{\partial V_D}{\partial T} = \frac{V_D}{T} - \frac{V_t}{T} (4+m) - \frac{kT}{q} \frac{Eg}{kT^2}$$

$$\frac{\partial V_D}{\partial T} = \frac{V_D}{T} - \frac{V_t}{T} (4+m) - \frac{Eg}{qT}$$

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (4+m)V_t - Eg/q}{T}$$

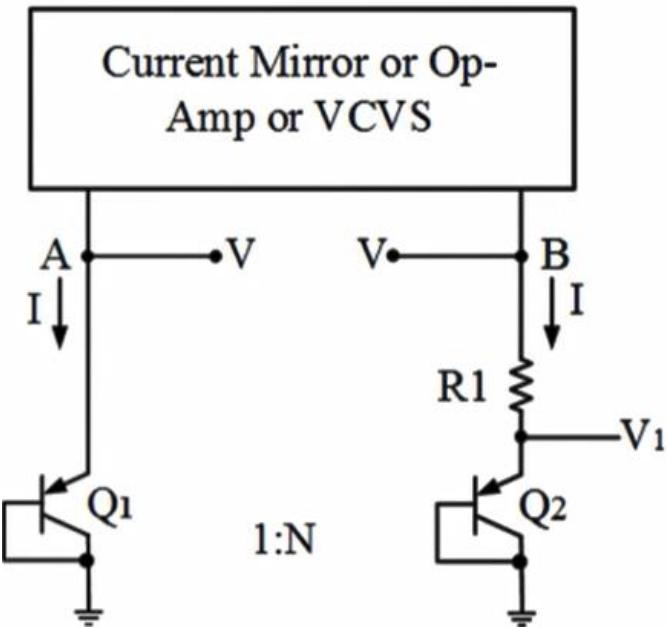
So the final slope is :-

$$\frac{dV}{dT} = \frac{V_D - (4+m)V_t - \frac{Eg}{q}}{T}$$

Putting the values we will get

$$\frac{dV}{dT} = \frac{0.7 - (4 - 1.5) * 0.026 - 1.2}{300} = -1.88mv/\deg k$$

PTAT Voltage generation



$$V = V_t \ln \frac{I}{I_s} \quad \text{and} \quad V_1 = V_t \ln \frac{I/N}{I_s}$$

According to the above circuit the node voltages at A and B are same. This is done by self bias current mirror ora VCVS which will be explained. From the equation the value of $\ln(I/I_s)$ is a strong quantity than V_t and hence the V value is CTAT in nature. The V_t is directly proportional to the temperature by the following equation:-

$$V_t = PTAT$$

$$V_t = \frac{kT}{q},$$

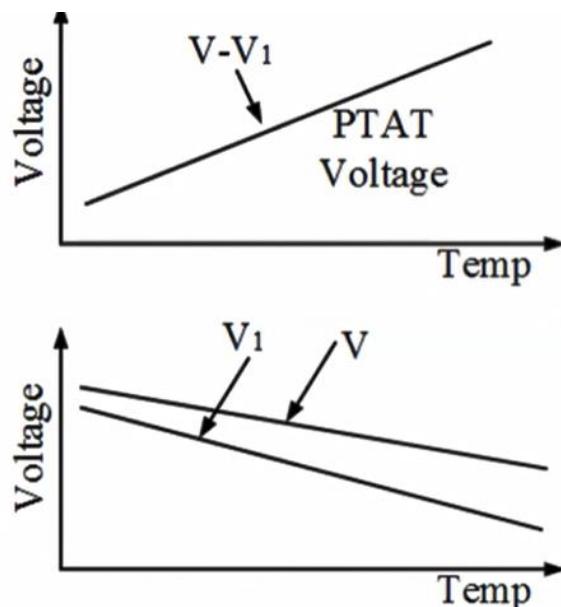
If we differentiate we will get the slope of the graph:-

$$\frac{d(V_t)}{dT} = \frac{k}{q} = 85 \mu V / \text{Deg Cent}$$

The calculation will be generally done by subtracting V_1 from V . V is less sloppy or less negative while V_1 is more sloppy as the current will flow is less. It will depend upon number of BJTs we are connecting. This will be clear by the following equation and the graph.

$$V - V_1 = V_t \ln(N)$$

$$V_t = \text{PTAT} \text{ and } \ln(N) = \text{constant}$$



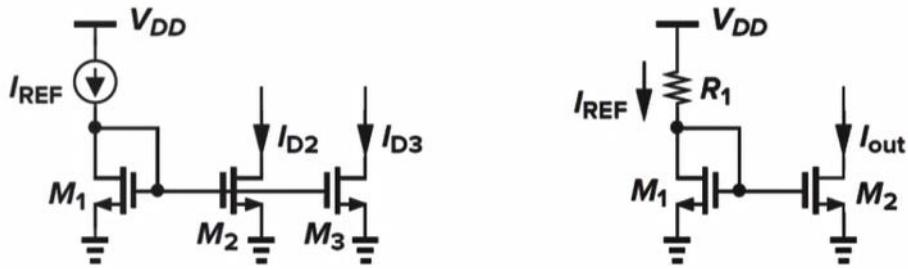
The design of R_1 is done as taking the current into consideration. The current equation $Vt \ln(N)$

$$R_1 = Vt \ln(N) / I$$

If the Number of BJTs are more then current will be divided and hence resistance value will be more. Less number of BJTs will have less value of resistance and will consume less area

Self Biased cascode Current Mirror

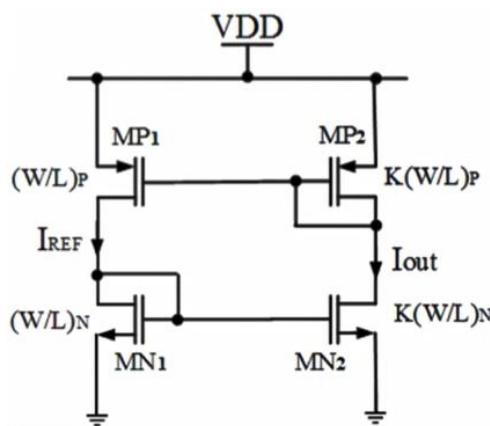
The main objective of the circuit is to produce a stable voltage at both the nodes which was explained in the voltage generation phase. The voltage should be independent of PVT. First topology which was tried to realise this circuit was :-



The first figure will produce I_{D2} and I_{D3} which will be equal to I_{ref} . But realising the I_{ref} with a BGR circuit will be too complicated. So the topology in figure can be used but the the value of I_{out} will vary greatly with V_{DD} according to the equation

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_m 1} \cdot \frac{(W/L)_2}{(W/L)_1}$$

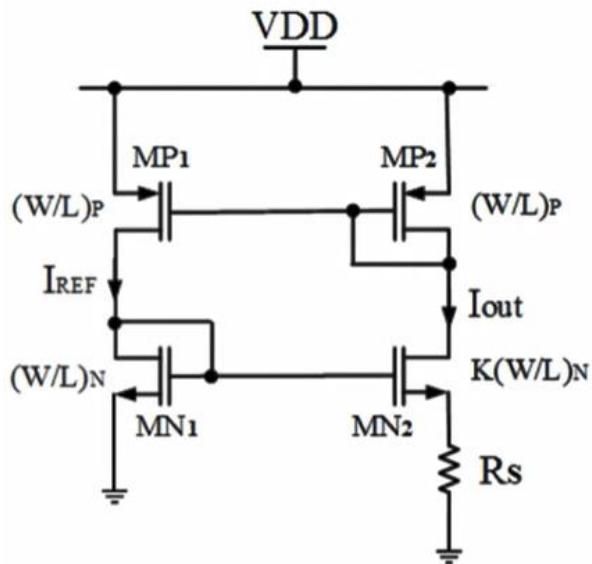
A topology should be used such that I_{out} and I_{ref} are independent to each other.



The above circuit with diode connected MN1 and MP2 will generate I_{out} and I_{ref} which will almost independent of VDD. I_{ref} will be bootstrapped to I_{out} . The governing equation is :-

$$I_{out} = K I_{ref}$$

The current uniquely can be generated from the following circuit:-

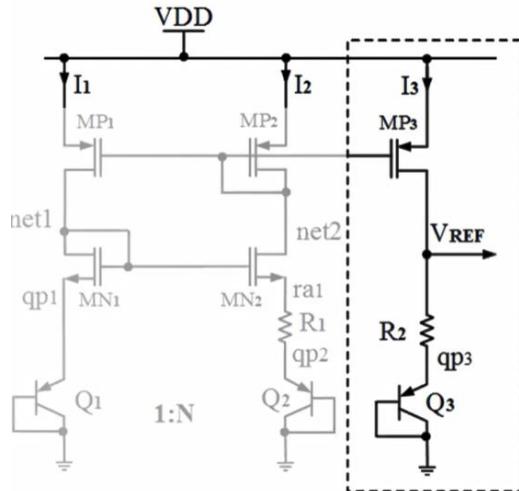


If we connect a net between MN_1 and short the output resistance we can calculate GM and shorting the input voltage and connecting a voltage source at the output we can calculate R_{out} by that way the gain of the circuit will be less than 1. The circuit will have voltage headroom issue due to which we will use LVT transistors during the lab. The governing is :-

$$I_{out} = \frac{2}{\mu_n C_{ox} (W/L)_N} \cdot \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}} \right)^2$$

Reference Branch Circuit

The transistor MP3 of the above diagram will copy the current I2. The Voltage across the BJT is Vq3 will be more sloppy and is CTAT in nature. The design of R2 is done such a way that VPTAT – VCTAT voltage will cancel each other and will generate almost constant reference voltage. This can be explained based on the below figure:-



The dependency of R2 over R1 is by a constant factor α . ($R_2 = \alpha R_1$)

The below equation is written as low temperature coefficient of Vref should be 0

$$\frac{dV_{R2}}{dT} + \frac{dV_{Q3}}{dT} = 0$$

$$\frac{d\alpha * V_{R1}}{dT} + \frac{dV_{Q3}}{dT} = 0$$

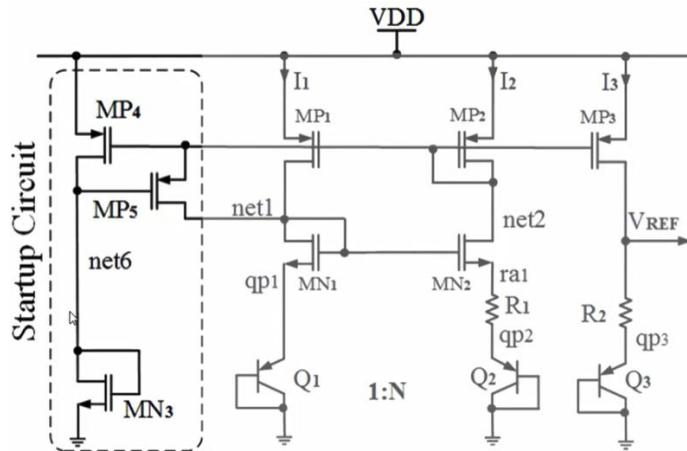
$$\frac{d(\alpha * V_t \ln N)}{dT} + \frac{dV_{Q3}}{dT} = 0$$

$$(\alpha * \ln N) \frac{dV_t}{dT} + \frac{dV_{Q3}}{dT} = 0$$

$$\frac{dV_{Q3}}{dT} = -1.6 \text{ mV/deg cent.}$$

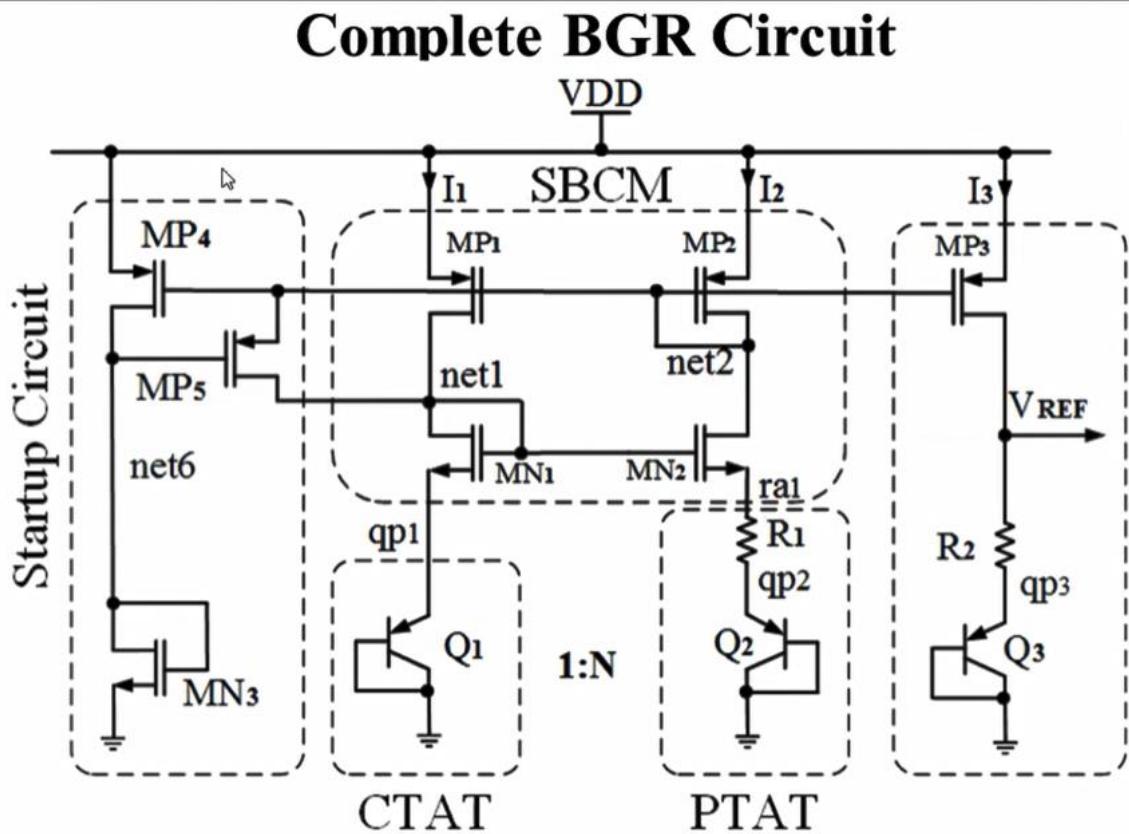
$$\frac{dV_t}{dT} = 85 \mu\text{V/deg cent.}$$

Startup Circuit



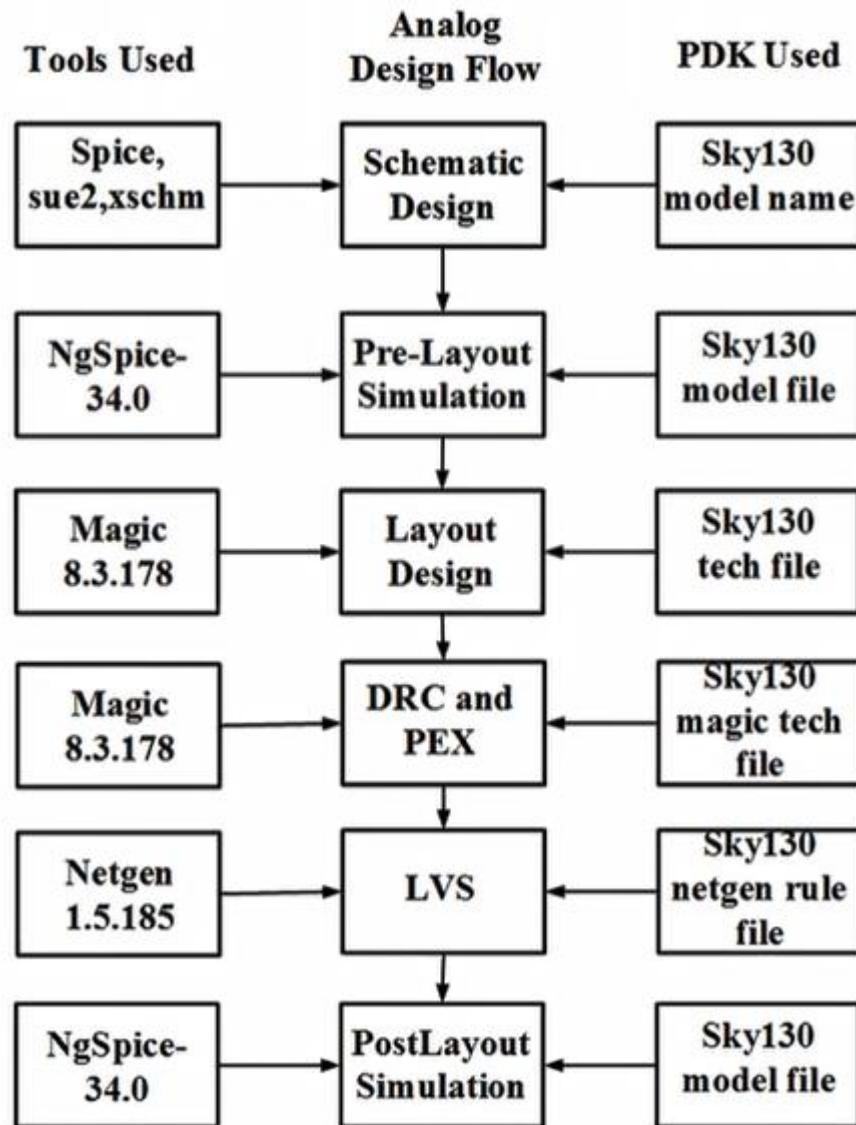
The requirement of the startup circuit is to disturb the stable point of the self bias cascode circuit. Since the lambda value is considered 0 the current is independent of supply and that is the zero current mode or degenerate bias point. When the net2 voltage will be greater than V_t of MP5 the current will flow through MP5 and slowly will through MN2, MP2 MP1 and will reach to desired point from degenerate bias point. When it will reach to stable point ,the voltage at source of MP5 will be less than gate of MP5 and hence the transistor will get not allow any current and the circuit will get isolated but minimal will flow through the branch.

Complete BGR circuit



Lab Report

The basic analog flow which was implemented to realise the BGR :



As a first step the models, tech and libraries were taken into my a directory named `cad_vsd` by using git clone command. A separate work directory was created where all the `.mag` files were taken.

The first is to get the design specification which is:-

- Supply voltage = 1.8V
- Temperature: -40 to 125 Deg Cent.
- Power Consumption < 60uW
- Off current < 2uA
- Start-up time < 2us
- Tempco. Of Vref < 50 ppm

The device specifications which we are using :-

	NFET (MOSFET)		PNP (BJT)
MOSFET	Type	LVT	BJT
	Voltage	1.8V	
	Thres. Voltage	~ 0.4V	
	Model Name	Sky130_fd_pr_nfet_01v8_lvt	

	RPOLYH (RESISTOR)
RESISTOR	Sheet Resistance
	~ 350 Ohm
	Tempoco.
	2.5 Ohm/Deg Cent.
	Bin width
	0.35u, 0.69u, 1.41u, 2.85u and 5.73u
	Model Name
	Sky130_fd_pr_res_high_po

The main steps which are followed while making the circuit:

Step-1: Calculation of Current

- Max. power Consumption < 60uW
- Max Total Current = $60 \text{ uW} / 1.8\text{V} = 33.33\text{uA}$
- So, we have chosen 10uA/branch, ($3 * 10 = 30\text{uA}$)
- Start-up current 1-2 uA

Step-2: Choosing Number of BJT in parallel in Branch2

- Less number of BJT: require less resistance value but matching hampers
- More number of BJT: requires higher resistance value but gives good matching
- So a moderate number have chosen (8 BJT) for better layout matching and moderate resistance value

Step-3: Calculation of R1

- $R1 = Vt * \ln(8) / I = 26 \text{ mV} * \ln(8) / 10.7\text{uA} = 5 \text{ KOhm}$
- R1 size: W=1.41um, L=7.8um, Unit rer value: 2k Ohm
- Number of resistance needed: 2 in series and 2 in parallel ($2+2+(2||2)$)

Step-4: Calculation of R2

- Current through ref branch: $I_3 = I_2 = V_t \ln(8) / R_1$
- Voltage across R2: $R_2 * I_3 = R_2 / R_1 (V_t \ln(8))$
- Slope of VR2 = $R_2 / R_1 (\ln(8) * 115\text{uV}) / \text{Deg Cent.}$
- Slope of VQ3 = $-1.6\text{mV}/\text{Deg cent}$
- Adding both and equating to zero, R2 will be around 33k Ohm
- Number of resistance needed: 16 in series and 2 in parallel ($2+2\dots+2+(2||2)$)

Step-5: PMOS design in SBCM

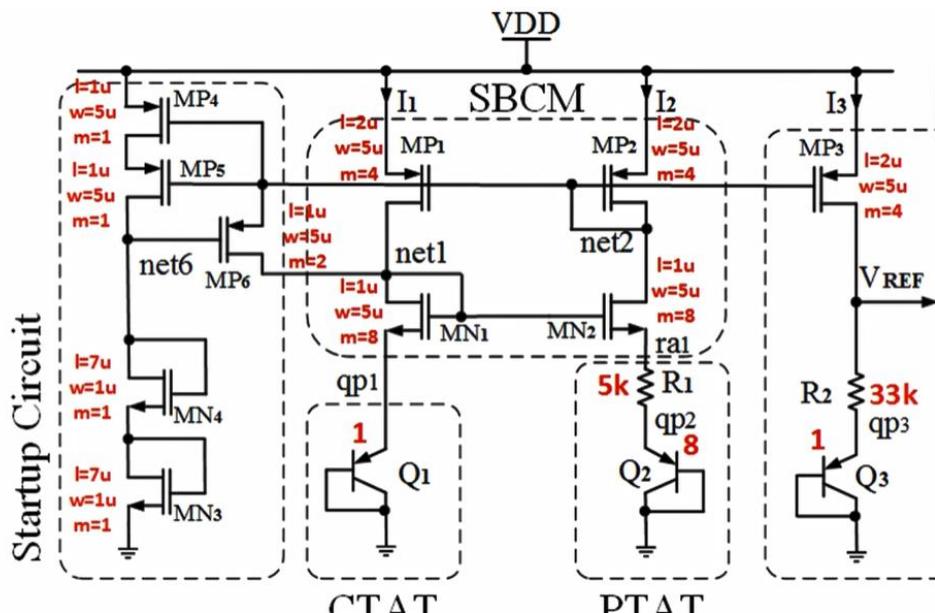
- Make both the MP1 and MP2 well in Saturation
- To reduce channel length modulation used $L=2\mu\text{m}$
- Finally the size is $L=2\mu\text{m}$, $W=5\mu\text{m}$ and $M=4$

STEP -6

Step-5: NMOS design in SBCM

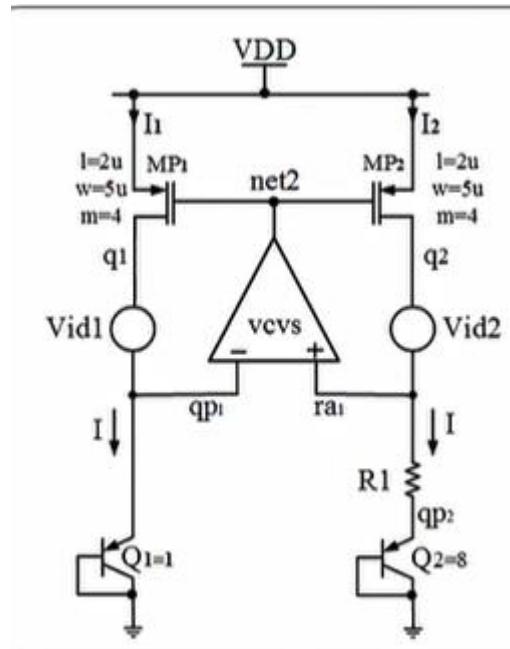
- Make both the MN1 and MN2 either in Saturation or in deep sub-threshold
- We have made it in deep sub-threshold
- To reduce channel length modulation used $L=1\mu\text{m}$
- Finally the size is $L=1\mu\text{m}$, $W=5\mu\text{m}$ and $M=8$

Final BGR circuit



Implementation of the circuit

The circuit under consideration



CTAT Voltage generation

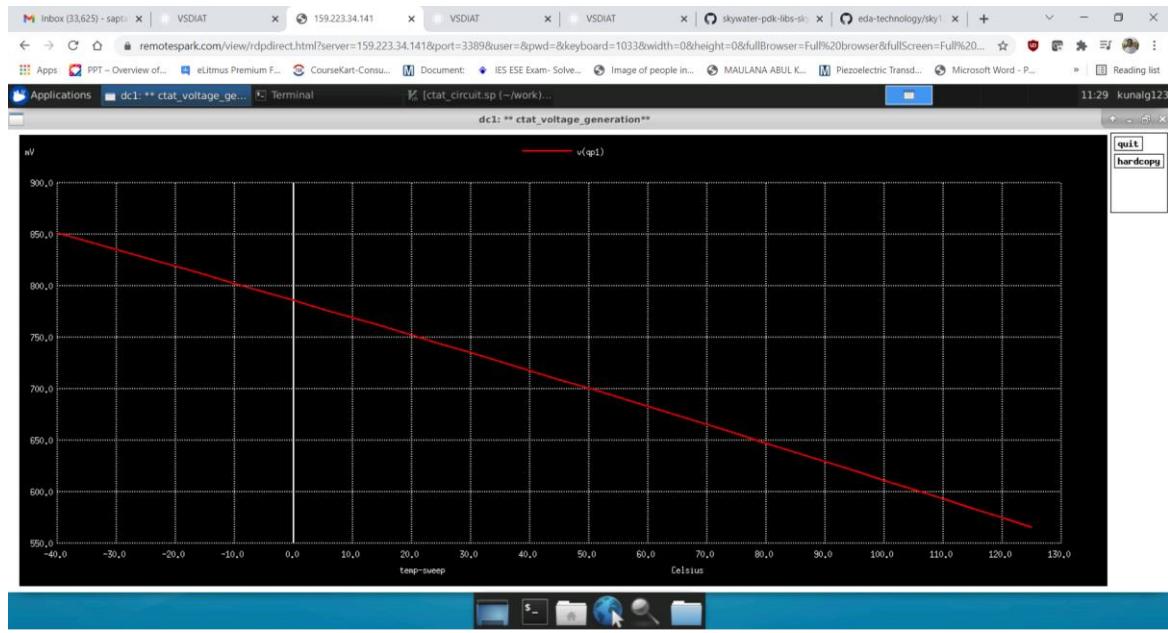
A CTAT voltage generation file was made based on the above circuit. The simulations were done for tree conditions.

1. By keeping the transistor unit to 1
2. By increasing the transistor unit
3. By increasing current

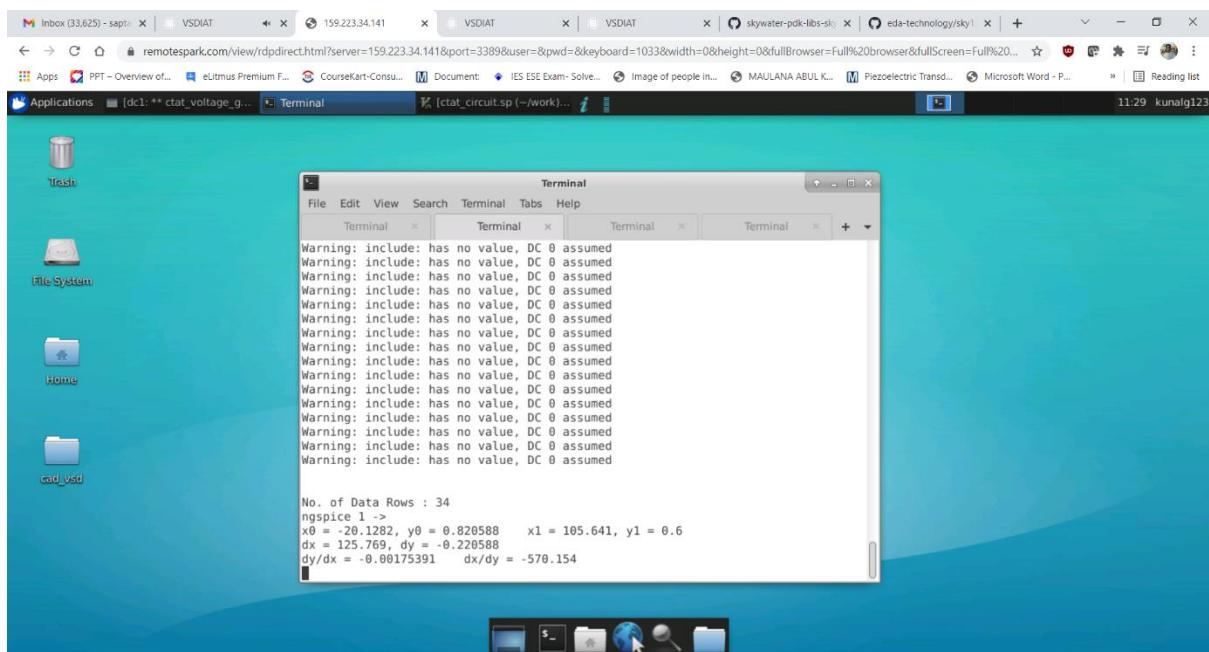
The command used to plot was

ngspice filename.sp

The graphs which were plotted are:-



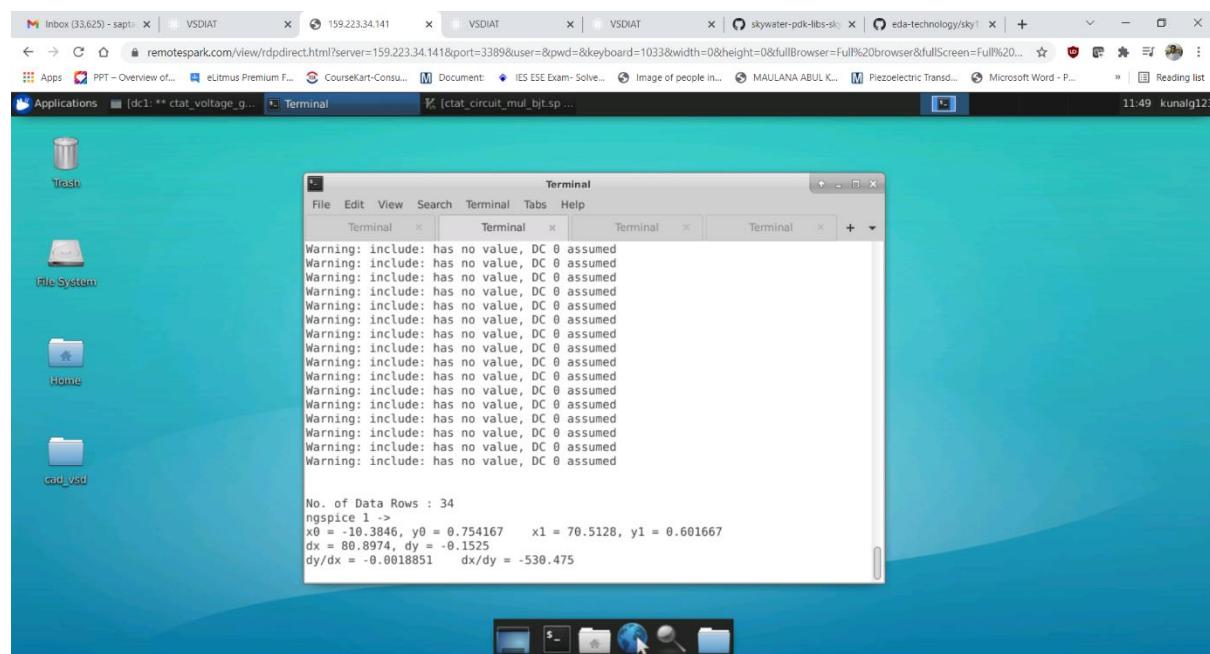
With one transistor the CTAT voltage graph



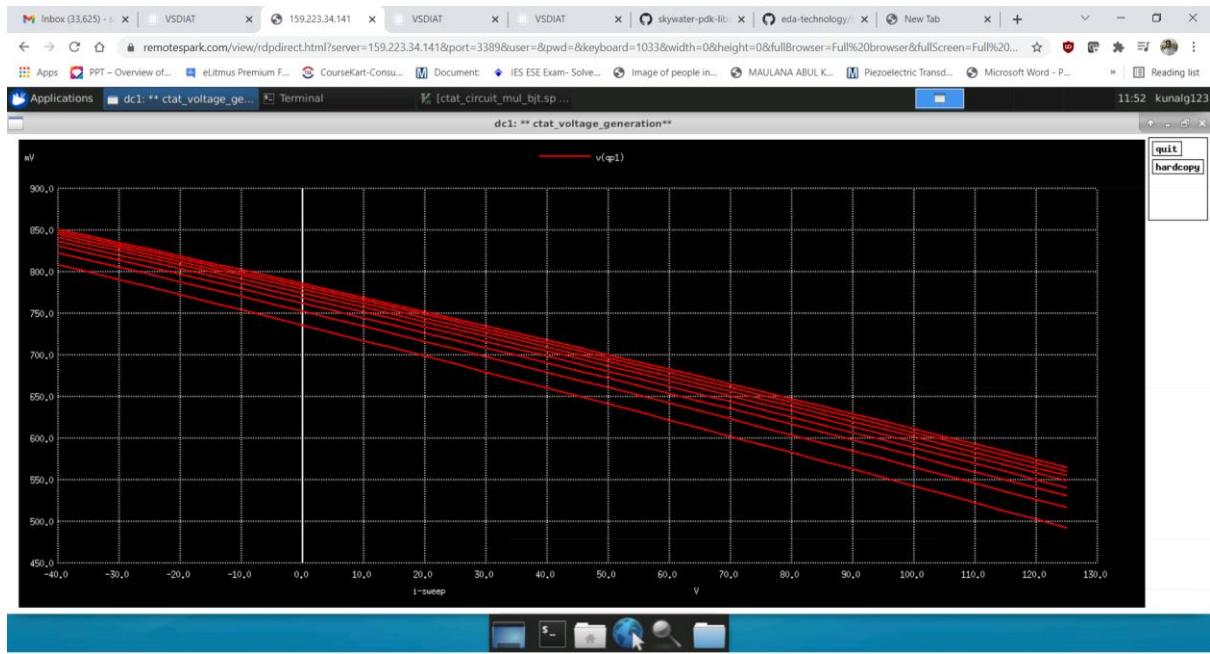
The slope of the previous graph



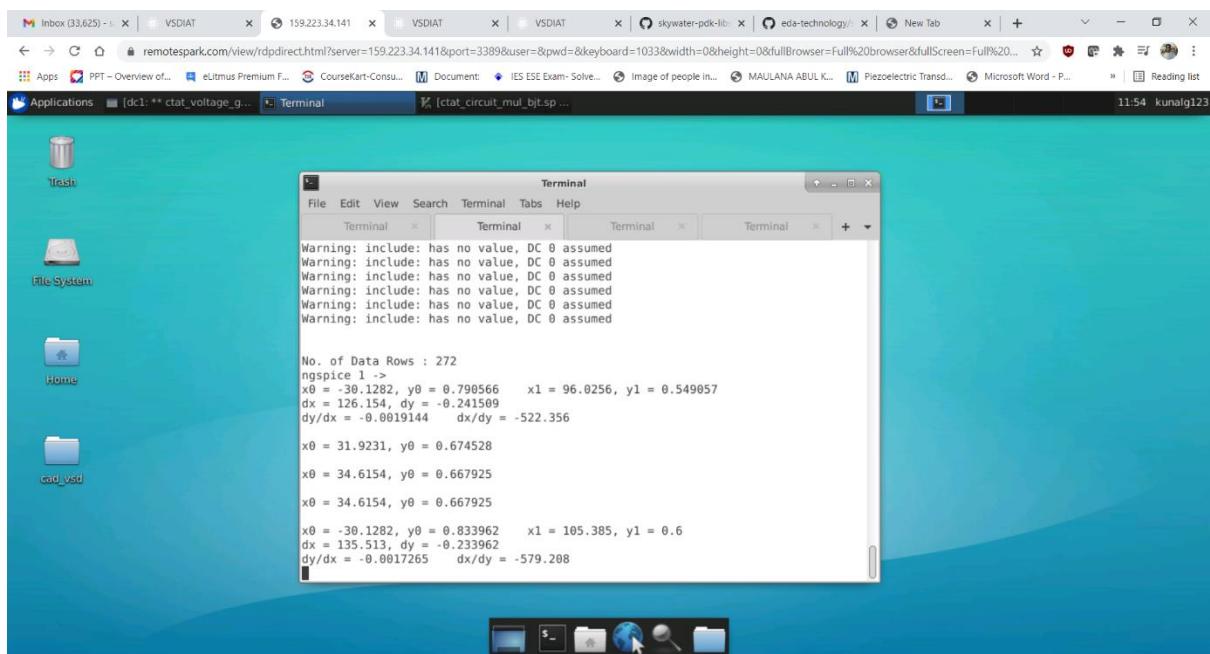
This graph is for multiple BJTs(8)



Since the BJTs are getting increased value of current will get divided and hence the slop of the graph will be more negative.

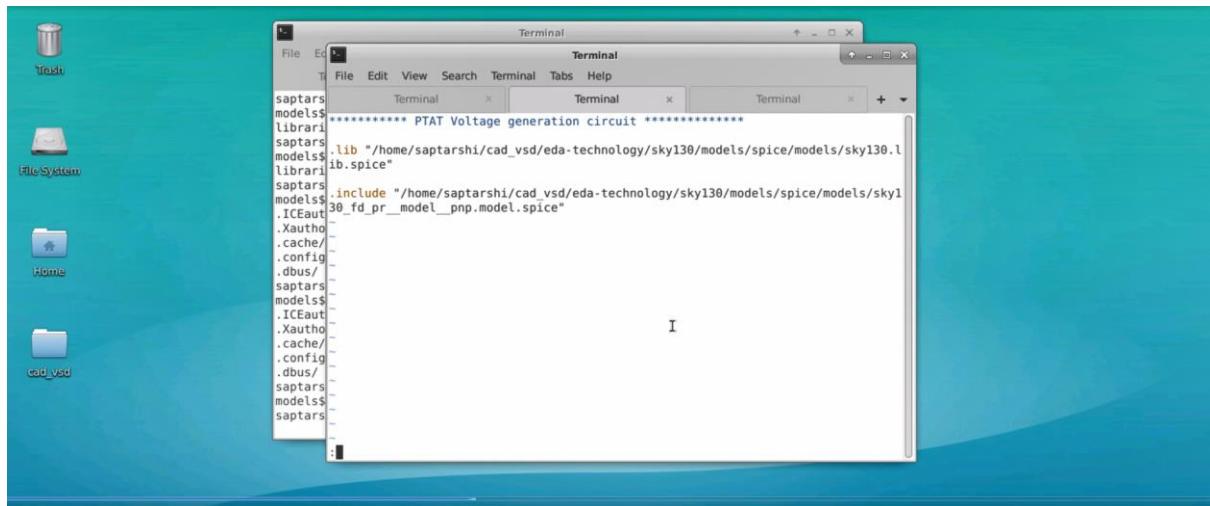


This graph is by varying the current from 1.25 to 10uA with step size of 1.25uA

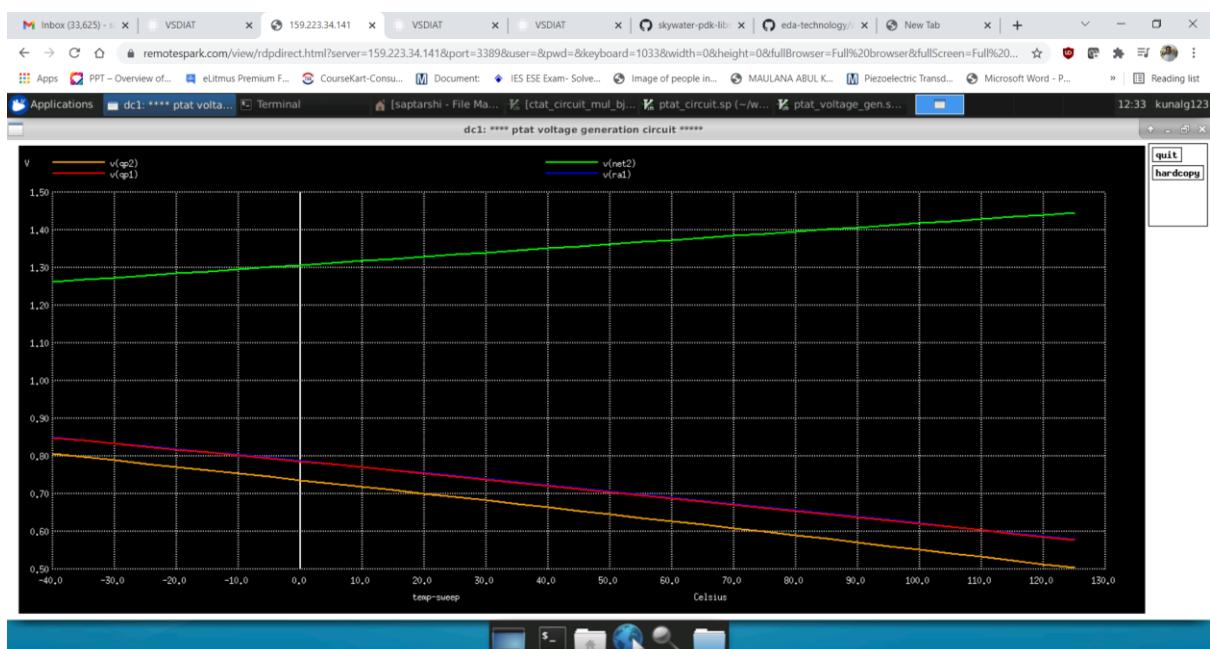


The value -0.0019144 is for 1.25uA and -0.0017265 is for 10uA

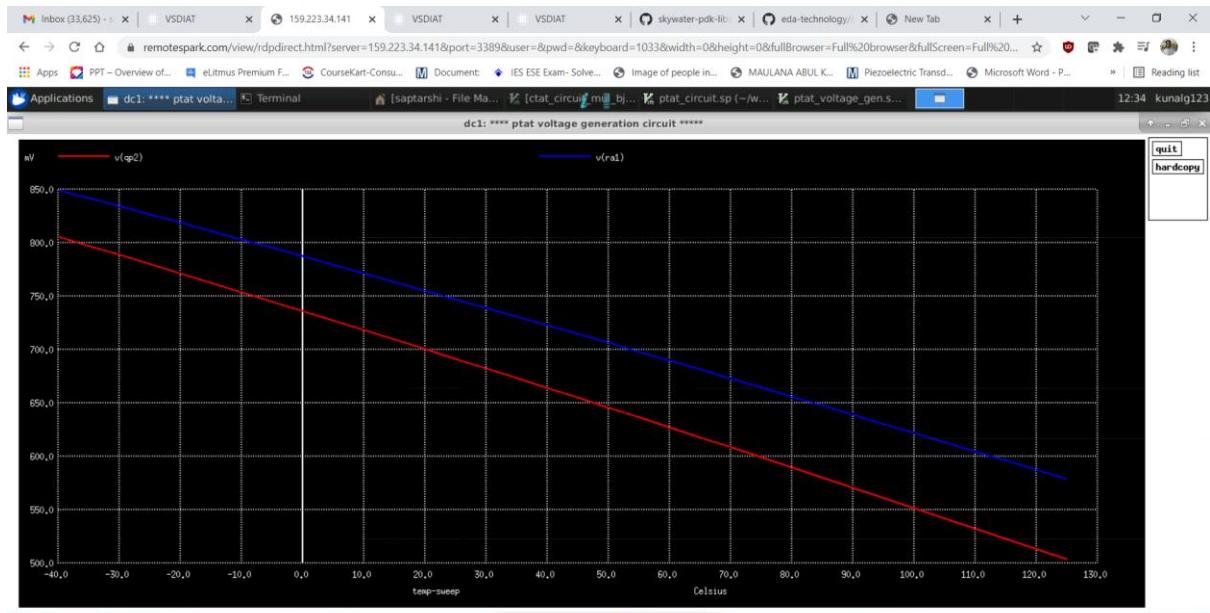
PTAT Voltage Generation



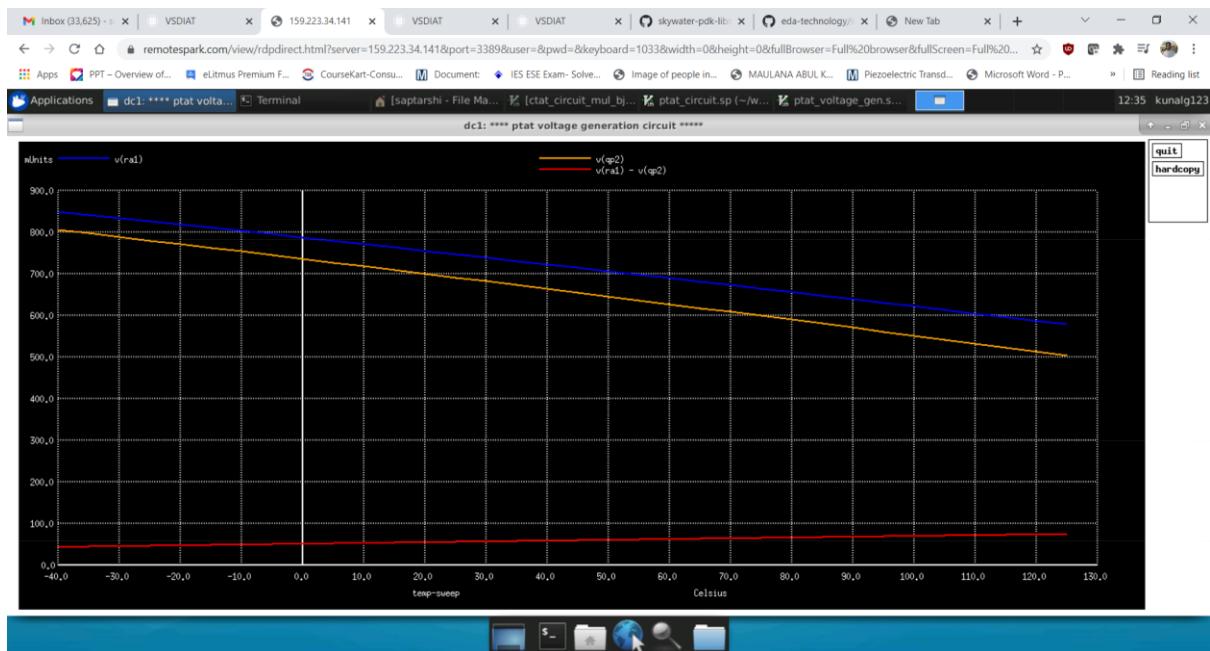
The above model files were used for simulations for both CTAT and PTAT.



The voltage at qp1,qp2,net2 and ra1



The main intention is to subtract the $V(ra1)$ and $v(qp2)$ to get the PTAT voltage



As can be seen the red curve is constant with temperature

```

.control
run
plot v(qp1) v(ral1) v(qp2) v(net2)
plot vid1#branch vid2#branch
.endc
.end

```

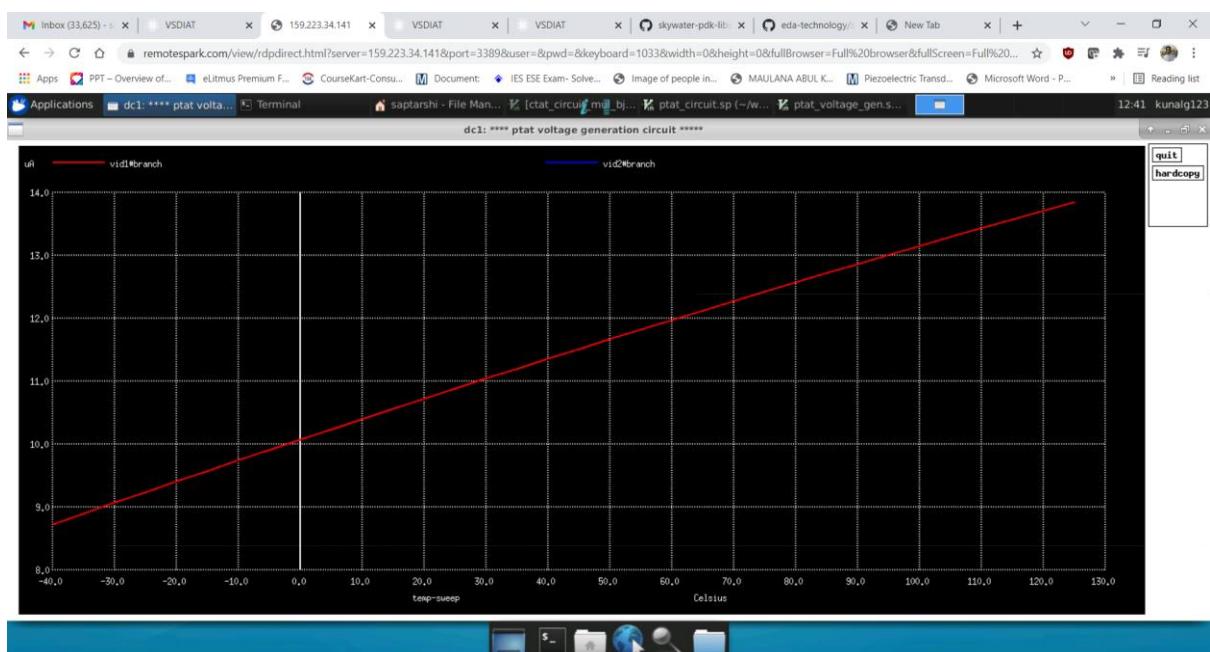
No. of Data Rows : 34

```

ngspice 1 -> plot v(qp2) v(ral1)
Error: no such vector qral1
ngspice 1 -> plot v(qp2) v(ral1)
ngspice 1 -> plot v(qp2) - v(ral1)
ngspice 1 -> plot v(ral1) - v(qp2)
ngspice 1 -> plot v(ral1) - v(qp2) v(ral1) v(qp2)
ngspice 1 ->

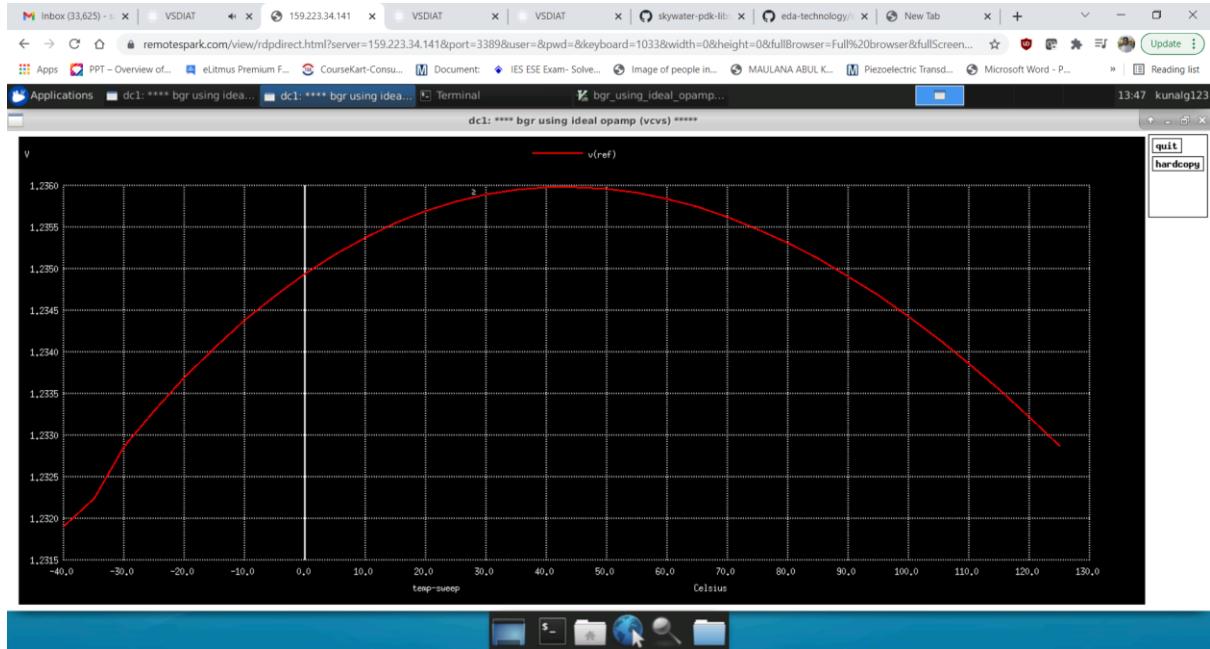
```

The expression required to obtain the above graphs



The current in two branches are same as expected.

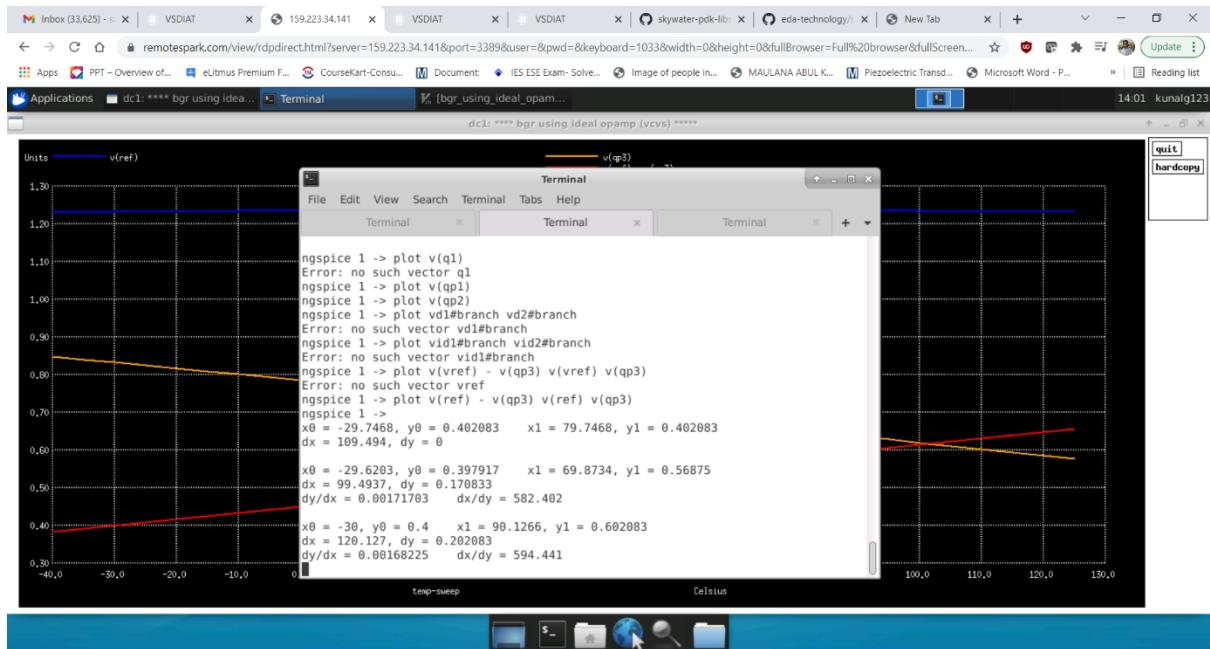
BGR circuit using VCVS as OPAMP



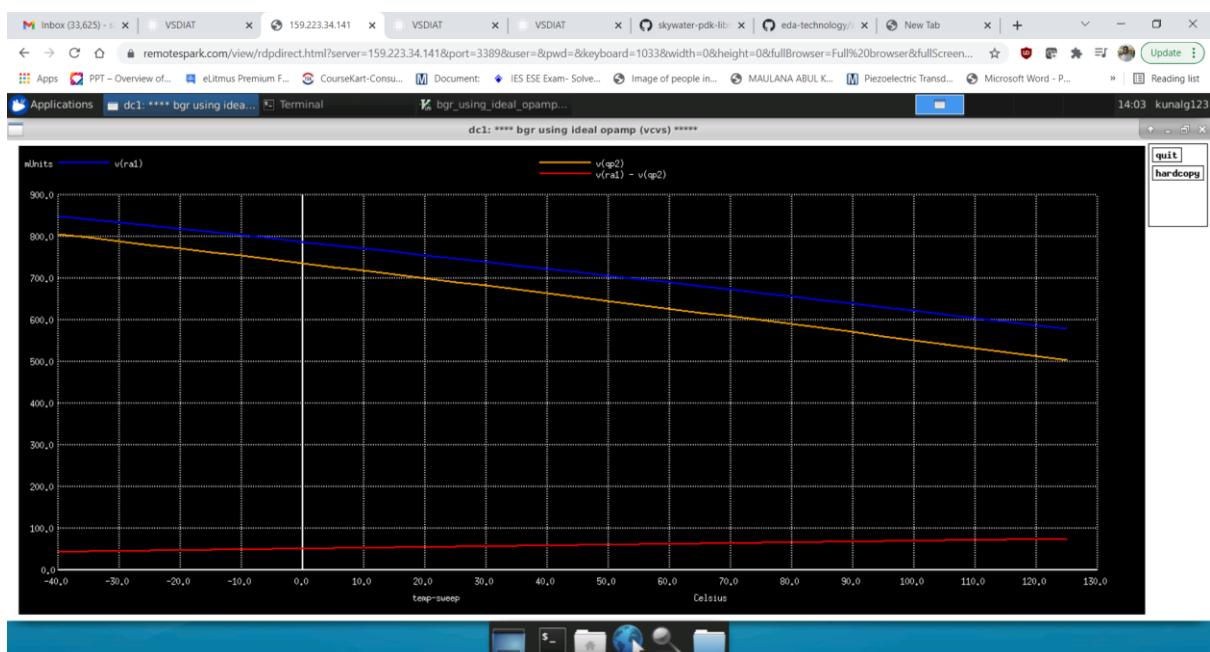
This is the umbrella curve for Vreference. The ppm can be calculated to 30-35 which is acceptable by $(V_{max} - V_{min})/V_{nominal}/T_{nominal} * 10^6$ ppm



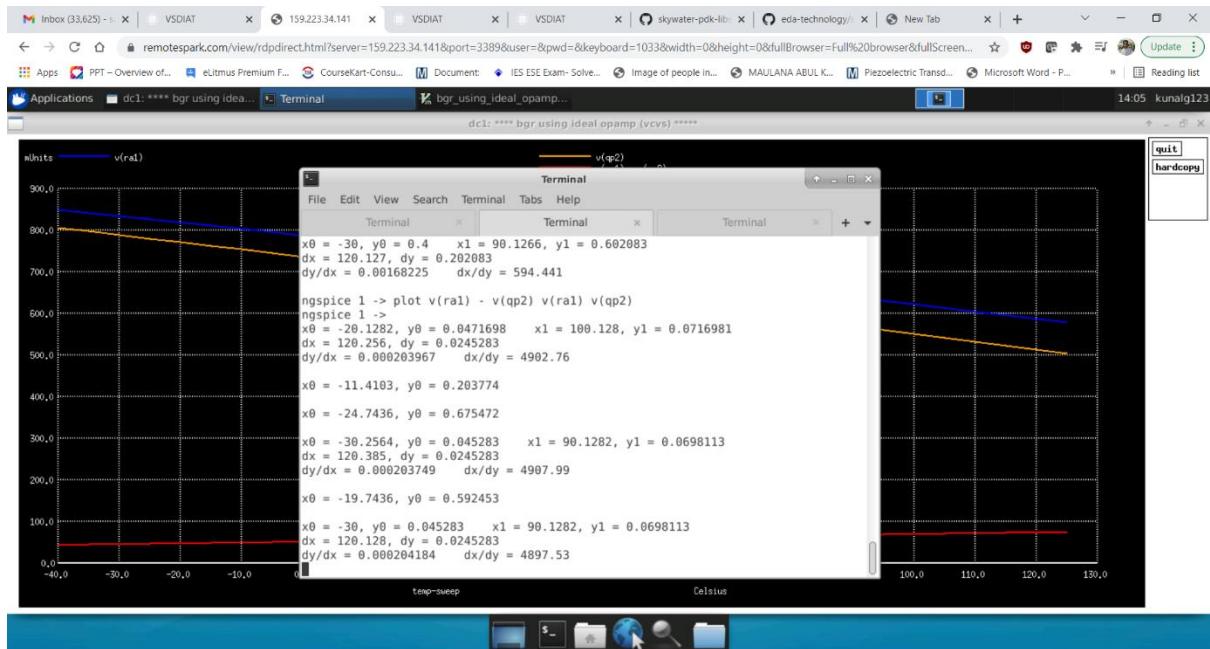
The above graph is the actual PTAT voltage which is calculated by $V_{ref} - V_{qp3}$



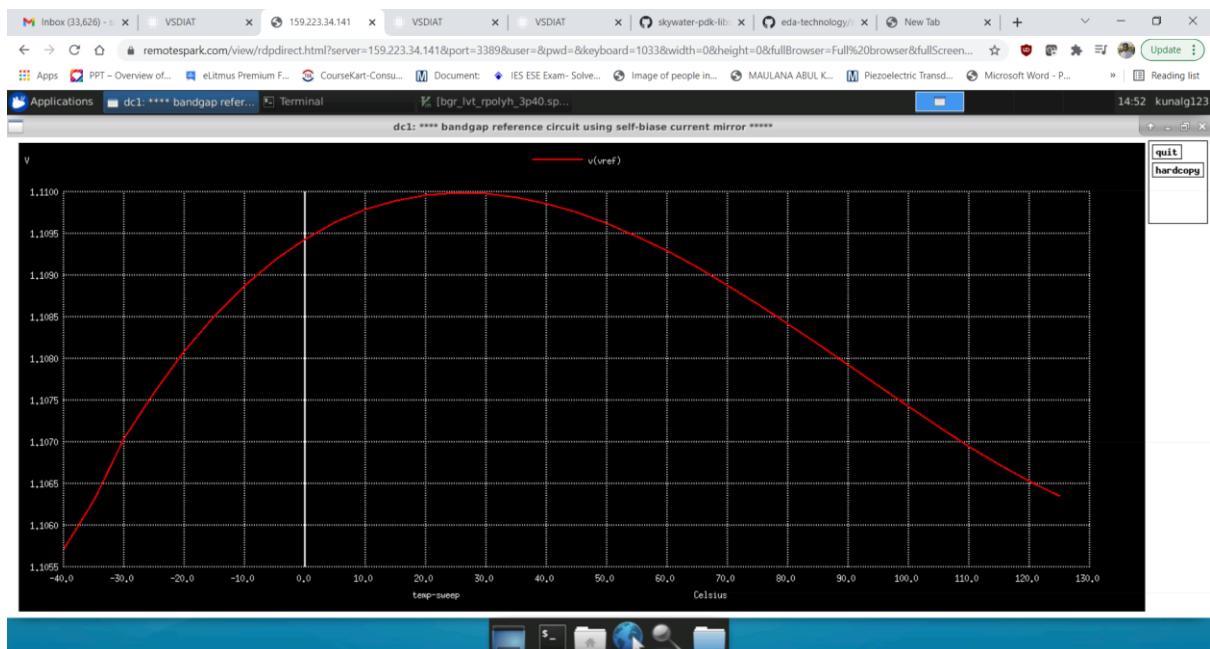
The slope of the above graph is 0.0016825



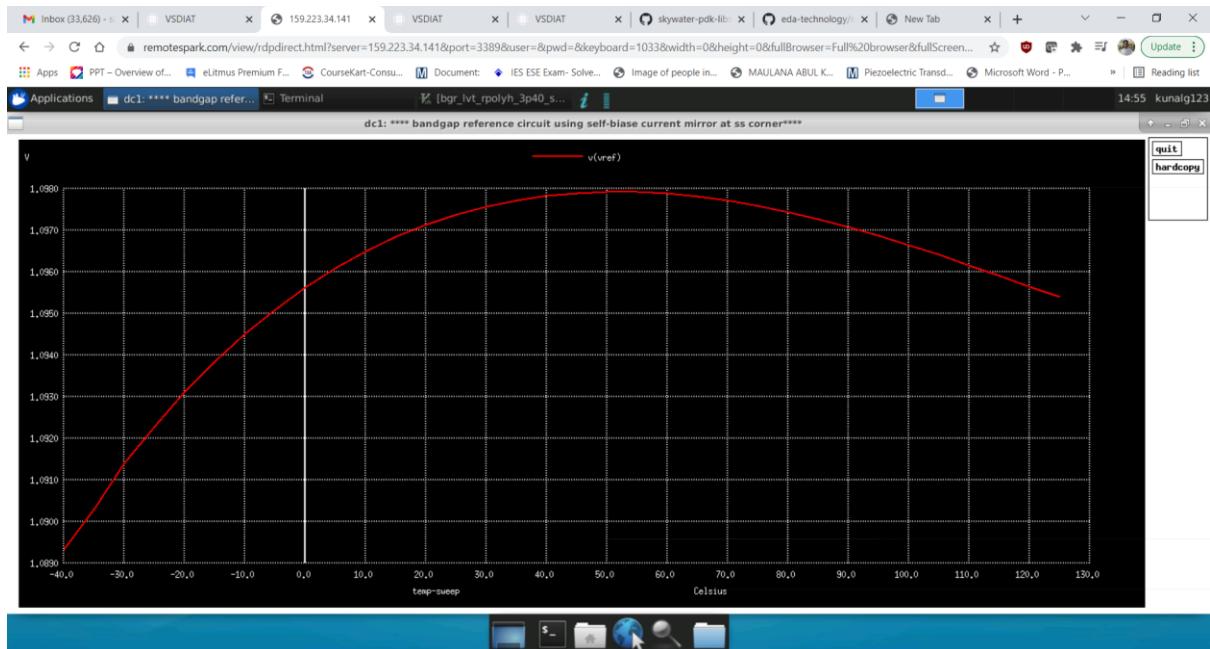
This is the voltage calculation of around R1. R1 is pf 2 resistor in series and two resistor in parallel while R2 is realized by 22 resistor in series and two resistor in parallel.



The slope of the graph is 0.000204 which is almost 1/9 times of the slope of R2.



Dc simulations for tt corner



DC simulations for ss corner

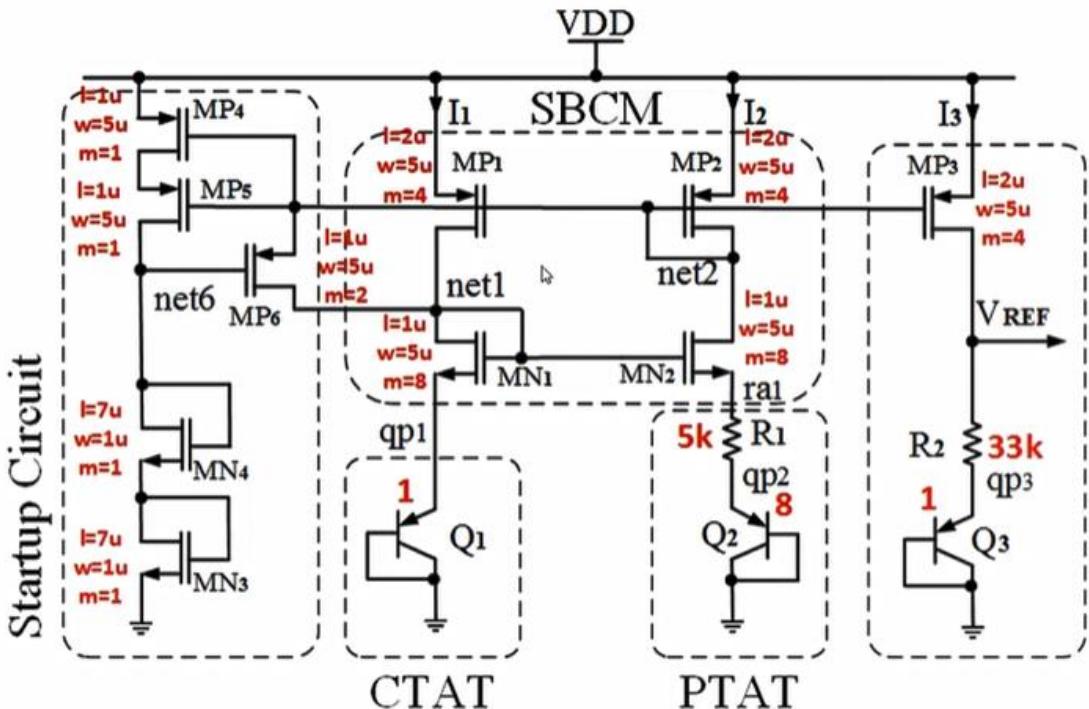


DC simulations for ff corner

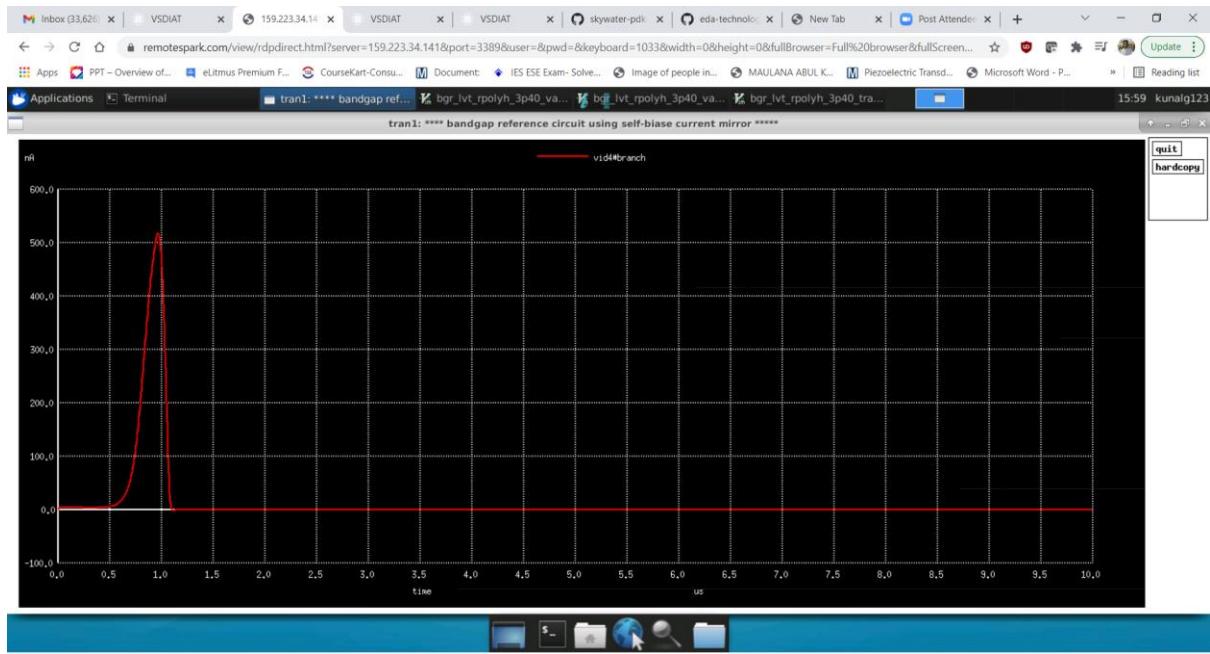


Transient simulations

Startup circuit simulations



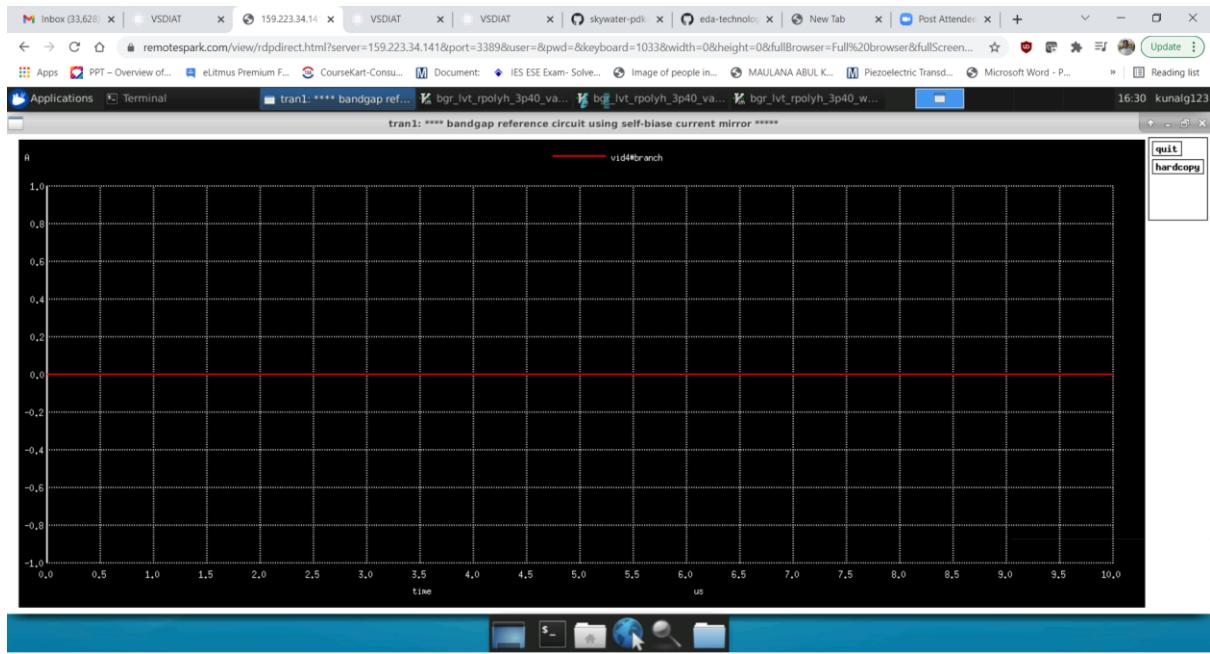
This graph corresponds to just after startup circuit point where the voltage difference between net2 and net6 is more than 0.5 and current start flowing. So initially net2 is following vdd but just after 1.6 it is going down. Similarly net1 voltage also almost following vdd but just after 1.6 the node voltage is increasing. Also from the graph it is clear that at 1.6 the Vref is constant.



This is the graph when MP6 just starts to allow the flow of current to shift the self bias current mirror circuit from zero current mode to the desired mode.



When the MP6 transistor is commented out in the sp file that means the startup circuit went to isolation phase, the net2 voltage is almost equivalent to vdd and net1 which is very low.



Since the transistor went off the current in that branch is 0.

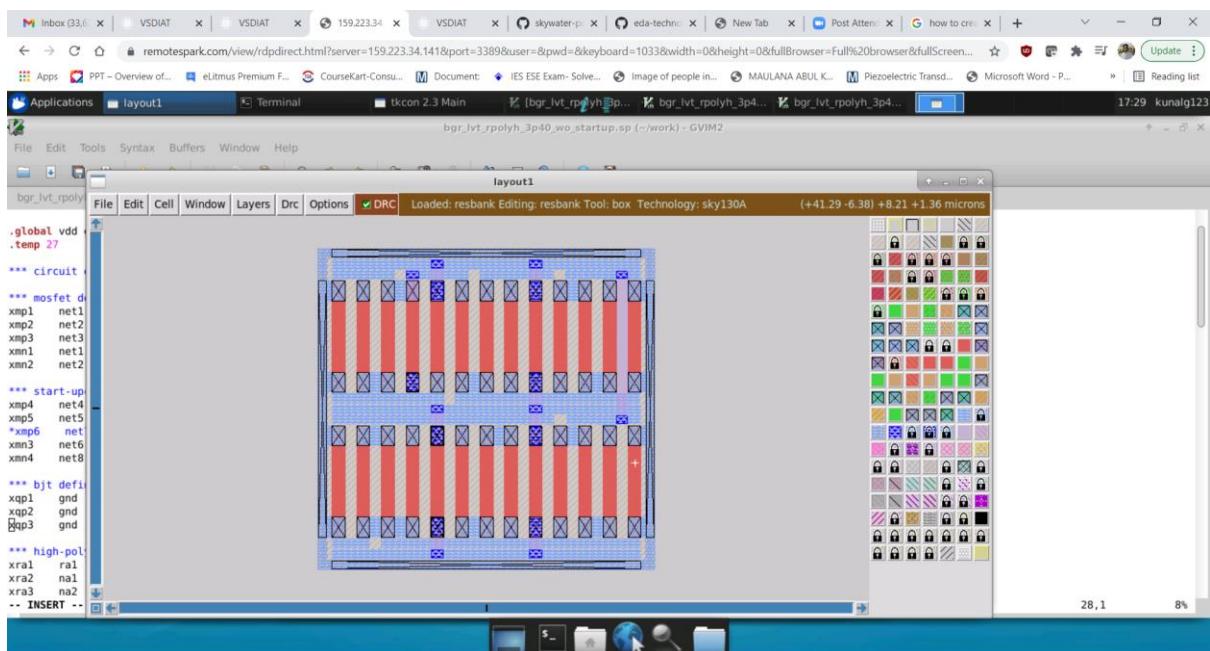


After isolation the value of the current through the start up circuit is very minimal.

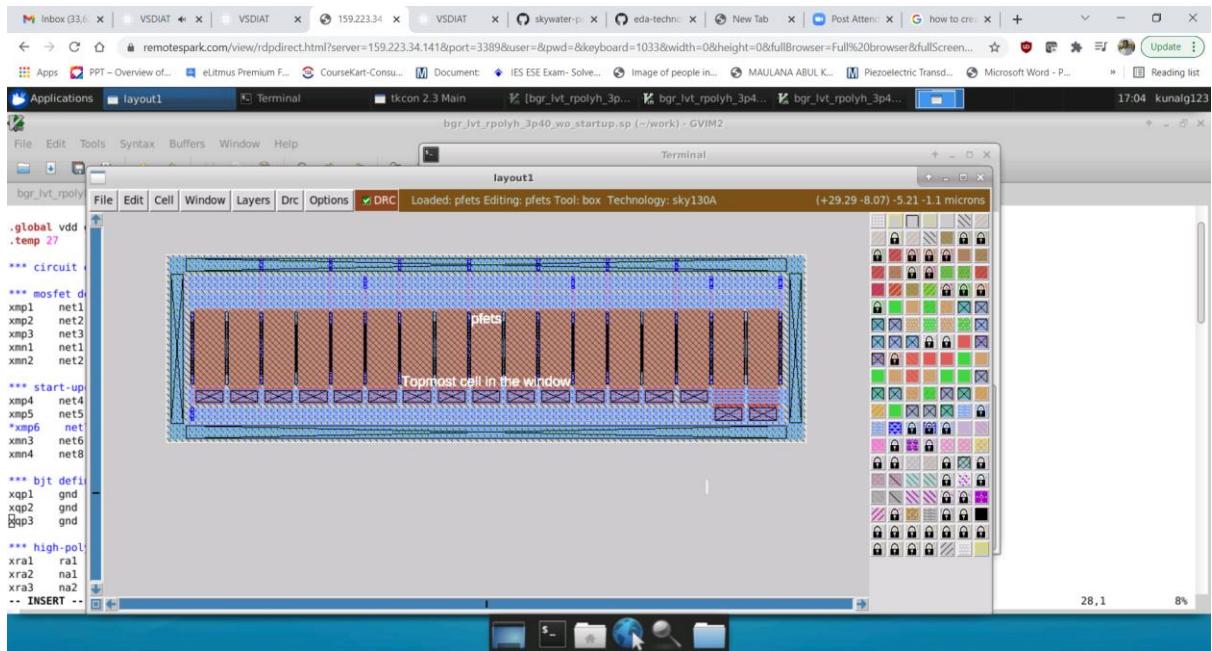
Layout

```
bgr_lvt_rpolyh_3p40_v... bgr_lvt_rpolyh_3p40_v... bgr_lvt_rpolyh_3p40_w... bgr_lvt_rpolyh_3p40_wo_startup.sp (-/work) - GVIM2
File Edit Tools Syntax Buffers Window Help
bgr_lvt_rpolyh_3p40_transient.sp bgr_lvt_rpolyh_3p40_wo_startup.sp
.global vdd gnd
.temp 27
*** circuit definition ***
*** mosfet definitions self-biased current mirror and output branch ***
xmp1 net1 net2 vdd vdd sky130_fd_pr_pfet_01v8_l1
xmp2 net2 net2 vdd vdd sky130_fd_pr_pfet_01v8_l1
xmp3 net2 vdd vdd sky130_fd_pr_pfet_01v8_l1
xmn1 net1 q1 gnd sky130_fd_pr_nfet_01v8_l1
xmn2 net2 net1 q2 gnd sky130_fd_pr_nfet_01v8_l1
*** start-upcircuit ***
xmp4 net4 net2 vdd vdd sky130_fd_pr_pfet_01v8_l1
xmp5 net5 net2 net4 vdd sky130_fd_pr_pfet_01v8_l1
*xmp6 net7 net6 net2 vdd sky130_fd_pr_pfet_01v8_l1
xmn3 net6 net8 gnd sky130_fd_pr_nfet_01v8_l1
xmn4 net8 net8 gnd sky130_fd_pr_nfet_01v8_l1
*** pjt definition ***
xqp1 gnd gnd qp1 vdd sky130_fd_pr_pnp_05v5_W3
xqp2 gnd gnd qp2 vdd sky130_fd_pr_pnp_05v5_W3
xqp3 gnd gnd qp3 vdd sky130_fd_pr_pnp_05v5_W3
*** high-poly resistance definition ***
xra1 ral nal vdd sky130_fd_pr_res_high_po_lp41 w=1.41 l=7.8
xra2 nal na2 vdd sky130_fd_pr_res_high_po_lp41 w=1.41 l=7.8
xra3 na2 qp2 vdd sky130_fd_pr_res_high_po_lp41 w=1.41 l=7.8
-- INSERT --
```

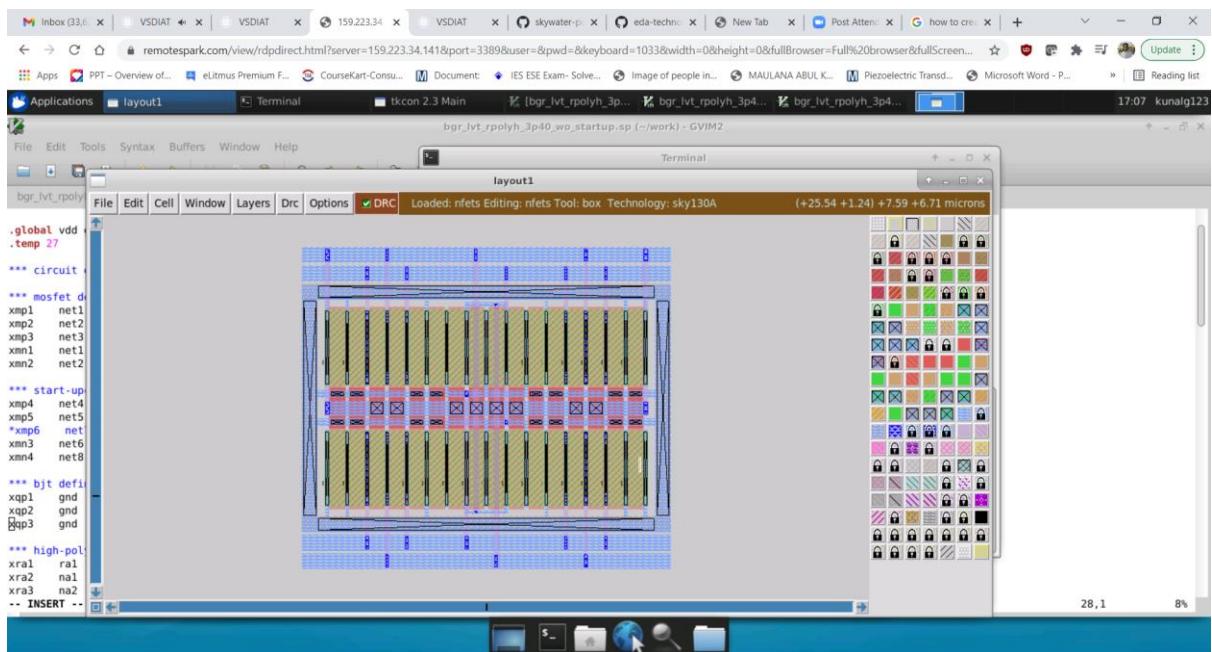
Layout was done using the MAGIC tool and model file was sky130A.tech



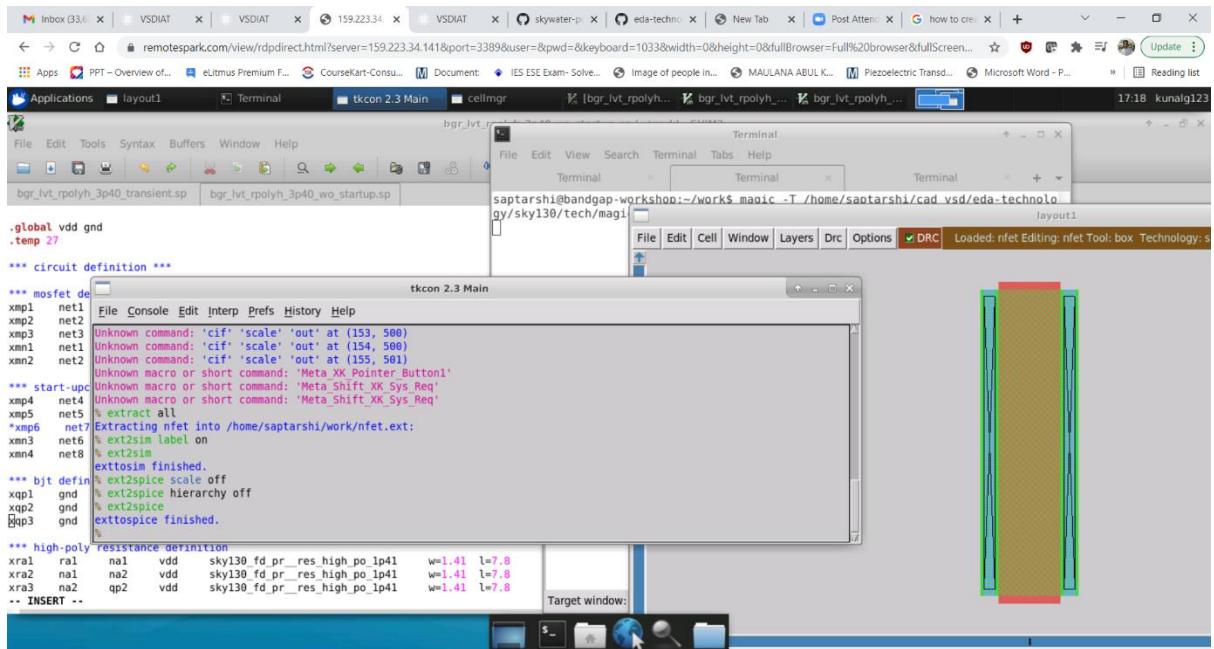
Resistor



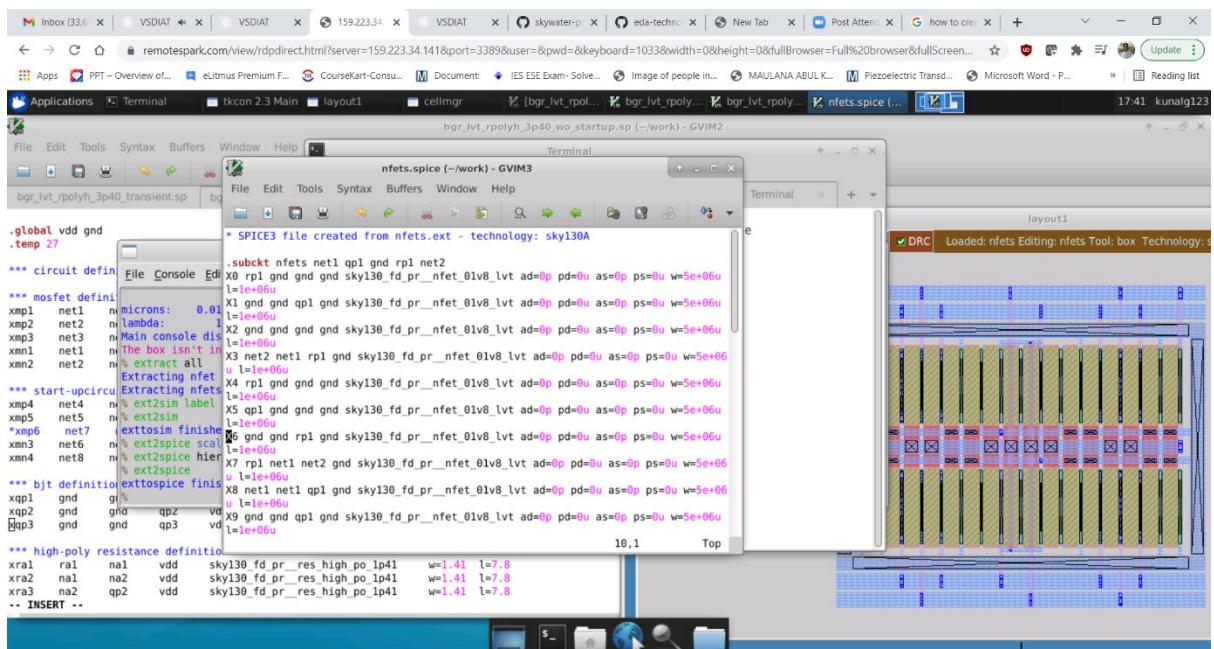
PFETS



NFETS



Extraction was done to .spice using the above commands



The parasitic file which got generated. For each and every component parasitics were extracted.

Further lvs was carried using netgen tool by using the netlist of the top file and the spice parasitic extracted file and the vreference should as shown in above graph. Unfortunately due to lack of time that simulation is not carried out.

Acknowledgements

Kunal Ghosh

Santunu Sarangi