SAPTASHWA BHATTACHARJEE

B.Tech in E&ECE @ IIT Kharagpur (4th Year)

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RESEARCH INTERESTS

ML Accelerators, In-Memory Computing, Neuromorphic Circuits, Analog/RF & Mixed-Signal Design

SUMMARY

Currently pursuing a bachelor of technology in Electronics & Electrical Communication Engineering at IIT Kharagpur. Expertise lies in *Analog/Mixed-Signal Design* and *In-Memory Computing*, developed through rigorous coursework, projects, and online certifications. Prior research experience in circuit design for ML accelerator in N5 (*FinFET technology*) in association with DxCorr Design Inc., USA. Interned at *École de Technologie Supérieure Montréal* and conducted research on the design of Impulse-Radio Ultra-Wideband non-coherent receiver. A proud recipient of ISRO's *Undergraduate Research Fellowship* for tape-out of a radiation-hardened VCO for space applications. Aspiring PhD candidate to carry out research on computationally efficient artificial intelligence through processing-in-memory, energy-efficient training and inference, and exploration of beyond-CMOS devices.

EDUCATION

IIT Kharagpur; West Bengal, India **2021-2025(Expected)**
B.Tech. in Electronics & Electrical Communication Engineering
GPA: 9.45/10.00
Thesis(Ongoing): Circuits for Deep Learning Accelerators | *Supervisor:* Prof. Mrigank Sharad, IIT Kharagpur

B.D.M.International; West Bengal, India **2021**
All India Senior School Certificate Examination (10+2)
GPA: 97.4%

B.D.M.International; West Bengal, India **2019**
All India Secondary School Examination (10)
GPA: 97%

HONORS & AWARDS

1. **Mitacs Globalink Research Internship** 2024 for a fully funded research internship at the *École de Technologie Supérieure - ÉTS Montréal*.
2. **DAAD WISE Scholarship** 2024 for a fully funded research internship at the *Technical University of Munich*.
3. **Undergraduate Research Fellowship** by SAC, ISRO, Ahmedabad: For full chip tape-out.
4. Kishore Vaigyanik Protsahan Yojana **(KVPY)** Fellowship 2020 awarded by the Indian Institute of Science(IISc).
5. Jagadis Bose National Science Talent Search **(JBNSTS)** Senior Scholarship 2021 by Govt. of West Bengal.
6. Secured a General Merit Rank of 8 in the West Bengal Joint Entrance Examination **(WBJEE)** 2021.

PROFESSIONAL EXPERIENCE

DXCorr Design Inc, *Project Intern*, USA (Remote-collaboration) **Jan 2024 - April 2024; Aug 2024 - Present**

- Topic: *Circuits for Deep Learning Accelerators*
- Supervisor: *Prof. Mrigank Sharad, IIT Kharagpur*

École de Technologie Supérieure, *Research Intern*, Montréal, Canada **May 2024 - July 2024**

- Topic: *Ultra-wideband Wireless Integrated Circuits for Ultra-low Power Communications*
- Supervisor: *Prof. Frederic Nabki, Dept. of EE, ÉTS Montréal*
- Laboratory: *LaCIME – communications et microélectronique*
- *Award:* Mitacs Globalink Research Internship

Indian Space Research Organization, *Research Fellow*, SAC Ahmedabad, India **June 2023 - Dec 2023**

- Project Topic: *Design of RHBD (Radiation-Hardened-By-Design) Cross-coupled Quadrature VCO*
- Coordinator: *Dr. Harishankar Gupta, Head, VLSI Design Lab, SAC, ISRO, Ahmedabad*
- Supervisor: *Prof. Mrigank Sharad, IIT Kharagpur*
- *Award:* Undergraduate Research Fellowship

PROJECTS

Circuits for Deep Learning Accelerators **Jan 2024 - April 2024; Aug 2024 - Present**

- Supervisor: *Prof. Mrigank Sharad, IIT Kharagpur*
- Laboratory: *Remote collaboration with DxCorr Design Inc.*
- Proposed a novel current subtraction-based IMC scheme to accommodate negative weights in the SRAM crossbar.
- Currently working on a Pulse mode IMC with a calibration loop for robust computation across all corners, enhancing MAC accuracy. Implementing binary weighted capacitor-based voltage summation to reduce the number of ADCs in the peripherals, thereby reducing power consumption.
- Wrote Verilog-A module to model a random voltage generator to determine the input combination corresponding to worst-case accuracy(to be taken care of during model training). Finding the ideal number of columns to be capacitively coupled, keeping the MAC accuracy in mind. Running Monte-Carlo simulations to capture the effect of device mismatch and process variations on MAC accuracy. Interfacing ADC with the output of capacitive summation.
- The entire work is being done in TSMC 5nm (FinFET) technology node, one of the most advanced nodes at present.
- Ongoing as *Bachelor's Thesis-I*: **Thesis Slides**

Ultra-wideband Wireless Integrated Circuits for Ultra-low Power Communications **May 2024 - July 2024**

- Supervisor: *Prof. Frederic Nabki*
- Laboratory: *LaCIME – communications et microélectronique, École de Technologie Supérieure Montréal*
- Collaborator(s): Ali Poursaadati Zinjanab & Nabki F.
- Literature survey of Impulse Radio-Ultra Wideband communication to understand its spectrum, communication protocol, and modulation schemes. Comparison of existing non-coherent receivers to realize the PLL-based solution of the synchronization issue. Proposed a novel ultra-low power non-coherent wake-up receiver based on an energy collection-based approach that employs a CDR to recover the TX clock. Designed an ultra-low power Gilbert cell-based squarer and time-interleaved integrator as a part of the Analog Front End in TSMC 180nm technology node. Tried to implement in-band blocker rejection using N-path harmonic rejection filters.
- Detailed design & implementation: **Project Report**

Design of RHBD Cross-coupled Quadrature VCO Design **June 2023 - Dec 2023**

- Supervisor: Prof. Mrigank Sharad, IIT Kharagpur & Dr. Harishankar Gupta, ISRO
- Laboratory: *Advanced-VLSI Lab (AVLSI), IIT Kharagpur*
- Collaborator(s): Haldar A., Samudralwar S., Gupta H., & Sharad M.
- Implemented various schemes to obtain an oscillation frequency range of 300MHz to 850MHz for a range of control voltage from 0 to 1.8V in SCL 180nm technology. Observed the effect of Single Event Transients and Upsets on various VCO parameters like frequency, jitter, etc. Ensured radiation hardening by splitting each stage into 20 layers. Designed the entire layout of the VCO in Cadence Virtuoso Layout Suite. Carried out post-layout simulation to observe the degradation in performance. Integrated pads with the core layout to make the design ready for tape-out.
- Detailed design & implementation: **Project Report**

Design of 7-bit Frequency Counter type ADC **Dec 2022 - April 2023**

- Supervisor: *Prof. Mrigank Sharad, IIT Kharagpur*
- Laboratory: *Advanced-VLSI Lab (AVLSI), IIT Kharagpur*

- Designed a Cascoded 2 Stage Op-Amp with an open loop gain of approx. 10,000. Used the Op-Amp in a closed loop (capacitive feedback) as the front-end amplifier, with a gain of 100 and bandwidth of 200 KHz. Designed a linear voltage-to-current converter to convert Op Amp output into proportional current. Implemented Current Controlled Oscillator (CCO) using current-starved inverter configuration and obtained linear characteristics up to 135 MHz frequency range. Used a Comparator to convert CCO output to a full swing rectangular waveform. Designed Counter and Register to count the number of pulses in one sampling period and achieved 7-bit resolution. Simulated the complete design in LTspice using 180 nm Predictive Technology Model (PTM).

COURSEWORK INFORMATION

Courses at IIT Kharagpur: Semiconductor Devices***** | Network Theory***** | Analog Electronic Circuits***** | Digital Electronic Circuits***** | VLSI Engineering***** | Computer Architecture***** | Architectural Design of ICs# | Analog Signal Processing# | Electromagnetic Engineering | RF & Microwave Engineering***** | Mixed Signal & RF Design | VLSI Interconnects# | Signals & Systems | Digital Signal Processing - I***** | Digital Signal Processing - II | Communication - I(Analog Communication)***** | Communication - II(Digital Communication)***** | Introduction to Wireless Communications | Satellite Communication# | Systems & Control | Probability & Statistics | Linear Algebra and Optimization Models | Algorithms***** |

*Courses marked with * have a laboratory component* *Courses marked with # are ongoing*

Online Certifications:
1. Supervised Machine Learning: Regression and Classification by Andre Ng, Coursera (DeepLearning.AI) *(Ongoing)*
2. Neural Networks & Deep-Learning by Andrew Ng, Coursera (DeepLearning.AI) *(Ongoing)*

TECHNICAL SKILLS

- In-Memory Computing (IMC) and Deep-Learning (DL).
- Analog/RF & Mixed-Signal Circuit Design.
- Transceiver design for wireless communication.
- *Technical Tools:* Cadence Virtuoso, LtSpice, MATLAB/Simulink, Ansys HFSS, Silvaco Atlas.
- *Programming Languages*: C, Python, Verilog/ Verilog A.

CAMPUS ACTIVITIES

Mechatronics team member | Swarm Robotics | IIT Kharagpur **Aug 2022 - July 2023**

- Supervisor: *Prof. Pallab Dasgupta, Dept. of CSE, IIT Kharagpur*
- Laboratory: *Swarm Robotics Lab, IIT Kharagpur*
- Participation as a team in the International Conference on Unmanned Aircraft Systems(ICUAS) 2023. Contributed to the design of control schemes such as PID control of the motor and Optimal control of the state of the bot.

First year trainee | TeamKART | IIT Kharagpur **Jan 2022 - Aug 2022**

- Supervisor: *Prof. C S Kumar, Dept of ME, IIT Kharagpur*
- Laboratory: *TeamKART Bay, IIT Kharagpur*
- TeamKART: official formula student team of IIT Kharagpur. Performed in-depth analysis of Battery Management System (**BMS**). Prepared Failure Mode and Effect Analysis (**FMEA**) of the team's future project: **Electric Vehicle**.

POSITIONS OF RESPONSIBILITY

Secretary | E&ECE Department Society | IIT Kharagpur **Oct 2022 - Sept 2023**

- Assisted with initiating a blog series, Corepedia, which aims to guide students through core internship preparation. Acted as the first point of contact for department students.

EXTRA CURRICULAR ACTIVITIES

National Sports Organization (NSO), Health & Fitness | IIT Kharagpur, India **2021-23**
Active participation in **Table Tennis** at IIT Kharagpur