SAPTASHWA BHATTACHARJEE

3rd Year Undergraduate
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

E-mail: saptashwab@kgpian.iitkgp.ac.in
Website : saptashwab.com
Phone : +91-9330087770

Education

Year	Degree/Certificate	Institute	CPI/%
2021 - Present	B.Tech	Indian Institute of Technology, Kharagpur	9.49/10
2021	AISSCE(XII)	B.D.M.International, Kolkata	97.4%
2019	AISCE(X)	B.D.M.International, Kolkata	97%

Research Interests

- Analog circuits design
- VLSI design
- Bioelectronics
- Cryo-CMOS for Quantum Computing Applications

Research Background

Cryogenic All Digital Phase Locked Loop for Quantum Computing Applications
Guide: Dr. Vishnu Paramasivam & Dr. Do Anh Tuan, Institute of Microelectronics, Singapore (*Nov 2023 - Present*)

- It is an All Digital PLL that contains Time to Digital Converter**(TDC)**, **Digital Filer**, and Digital Controlled Oscillator**(DCO)**.
- The modules are being modeled using system verilog to create an architectural design.
- The PLL will operate at **4 Kelvin**. So, power consumption is a critical parameter since leakage cannot be tolerated.
- Its tunability and output frequencies will be used as the local oscillator for an upconverter. The central frequency is **6GHz**.
- The layout will be designed either in **40nm UMC** or **60nm TSMC** technology node depending upon the relative performance.

Novel Cross Coupled Quadrature VCO for ISRO SERDES Module
Guide: Prof. Mrigank Sharad, Indian Institute of Technology, Kharagpur (*May 2023 - Nov 2023*)

- Implemented various schemes to obtain an oscillation frequency range of **500MHz to 1.5GHz** for a range of control voltage from **0 to 1.8V** in **180nm CMOS** technology.
- Parameters such as **jitter** and **phase noise** across all the corners were noted during simulation at various temperatures.
- Ensured **radiation hardening** by splitting each stage into 20 layers to tackle Single Effect Transient and Upset.
- Designed the entire layout of the VCO and checked **DRC** and **LVS** in Cadence Virtuoso Layout Suite.
- Carried out **post-layout simulation** after parasitic extraction and observed the degradation in performance.
- **Input and Ouput Pads** were then integrated with the core layout to make the design ready for fabrication.

Design of 7 bit Frequency Counter type ADC
Guide: Prof. Mrigank Sharad, Indian Institute of Technology, Kharagpur (*Dec 2022 - April 2023*)

- Designed a two stage **OP-AMP** with an open loop gain of **10,000** and a closed loop gain of **100** with capacitive feedback.
- Connected the OP-AMP output to **Voltage to Current Converter** which was then fed into a Current Controlled Oscillator.
- **Current starved oscillator** was implemented. Linear plot of frequency vs current was achieved up to **135 MHz**.
- **Comparator** was coupled to obtain rectangular waveform with full swing from **0 to 1.8V**.
- **7 bit Counter** was used to count the number of pulse occurrence in a specific time period, obtaining digital output depending on the frequency, which in turn depends upon the voltage of the input.
- Entire design was done using **180nm** technology MOSFET Predictive Technology Model**(PTM)**.

The 2023 International Conference on Unmanned Aircraft Systems (*Feb 2023 - April 2023*)

- Performed successful inspection of a factory and detect defects in the infrastructure.
- Navigated the unknown area safely as a part of the Exploration subroutine. Simulation was done in **ROS- Gazebo** environment. It involved **SLAM, Visual Odometry.**
- **Perception:** Detect and classified defects. Data set was provided by the organizers.
- **Pose Estimation:** The ability of the UAV to estimate its pose in a **GNSS denied environment** using onboard sensor data.
- The estimated pose was then compared with very accurate motion tracking system from **CATEC indoor test bed.**

Technical Skills

Programming Languages: C, Python, Verilog, HTML, CSS, JavaScript, AVR C
Softwares: Cadence Virtuoso, Cadence Layout Suite, Synopsys, Ansys HFSS, MATLAB, Simulink, Tina TI, LT Spice, Atmel Studio

Coursework Information

Semiconductor Devices*	Network Theory*
Analog Electronic Circuits*	Digital Electronic Circuits*
Electromagnetic Engineering	RF and Microwave Engineering*#
Signals and Systems	Digital Signal Processing*#
Analog Communication*#	Introduction to Wireless Communication#
Systems and Control	Algorithms#
Probability and Statistics	Linear Algebra and Optimization
Advanced Calculus	Linear Algebra, Numerical and Complex Analysis

Courses marked with * also have a lab component.

Courses marked with # are ongoing and will be completed by 3rd week of November 2023.

Academic Achievements

- Secured an **All India Rank of 1081** in **JEE Advanced 2021** and was among the **top 0.627%** of the **142k** applicants.
- Secured an **All India Rank of 890** in **JEE Mains 2021** and was among the **top 0.09%** out of **1.3 million** applicants.
- Secured an **All India Rank of 624** in **KVPY SX 2020** conducted by Indian Institute of Science(IISc) among **150k+** candidates.
- Secured an **All India Rank of 8** in West Bengal Join Entrance Examination **(WBJEE) 2021** among **65170** candidates.
- Recipient of **Jagadis Bose National Science Talent Search Senior Scholarship 2021**.
- Qualified **Pre-Regional Mathematics Olympiad 2018** among 10k+ students organized by Homi Bhabha Centre for Science Education.

Campus Activities

Mechatronics Team Member, Swarm Robotics, Indian Institute of Technology, Kharagpur (*Aug 2022 - Present*)

- Assisted by seniors in learning Robot Operating System**(ROS)**, Arduino, control schemes like **Optimal Control**, PID Control.
- Participation as a team in the International Conference on Unmanned Aircraft Systems 2023.

First Year Trainee, TeamKART, Indian Institute of Technology, Kharagpur (*Jan 2022 - Aug 2022*)

- It is the official formula student team of IIT Kharagpur that designs formula-student style prototype race cars.
- Learnt about different aspects of cars like types of suspension, slip angles, caster, camber, KPI, electronic sensors like butterfly sensor, throttle position sensor, crankshaft position sensor etc.
- Performed in-depth analysis of Battery Management System **(BMS)**, its components, topology etc.
- Prepared Failure Mode and Effect Analysis **(FMEA)** of the team's future project: Electric Vehicle.

Positions of Responsibility

Secretary, E&ECE Department Society (*Oct 28;22 - Present*)

- Assisted with initiating a blog series, **Corepedia**, which aims to guide students through core internship preparation.
- Acted as the first point of contact for department students about queries related to department and efficiently resolved them.

Extra-Curricular Activities

- Member of **National Sport Organization**, introduced by the Government of India to promote the development of athletics and sporting activities among the nation's youth.
- Part of four member **Mathematics Olympiad** team of Radhakrishnan Hall of Residence in **General Championship** at Indian Institute of Technology Kharagpur.
- Active participation in **Table Tennis** in Radhakrishnan Hall of Residence at Indian Institute of Technology Kharagpur.

Academic References

- Prof. Dr. Mrigank Sharad
  Indian Institute of Technology
  Kharagpur, West Bengal 721302
  India
  Relationship: Research Guide
- Dr. Vishnu Paramasivam
  Senior Scientist
  Institute of Microelectronics
  Innovis - 2, Fusionopolis Way
  Singapore 138634
  Relationship: Research Guide
- Prof. Dr. Pechetti Sasi Vinay
  Indian Institute of Technology
  Kharagpur, West Bengal 721302
  India
  Relationship: Course Professor