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9.1 Function Description to LP-2900

Due to the rapid improvement in electronic technology in these years, our life is becoming more and more convenient and comfortable. The domestic electrics, mobile phones and computer side products all of these indicate the electric products are getting smaller, light-weighted, and powerful. Digital circuits are gradually replacing the analog circuits. At the mean time, with the improvement of production in digital circuits, the standard IC, such as TTL/COMS is being replaced by CPLD/FPGA. With the population of CPLD chip, it is about time to reverse the teaching methodologies in Logic Design. LP-2900 CPLD Logic Design Lab Platform (Figure 9.1) is a product produced by Leap Electronic Co. in 1999. Under the devoted research and development, Leap Electronic Co. integrates the major functions--design, simulation, and verification--to provide a comprehend logic design teaching environment, in which the features are easy to set up and operate, instant response, and the course arrangement set from generous to sophisticated.

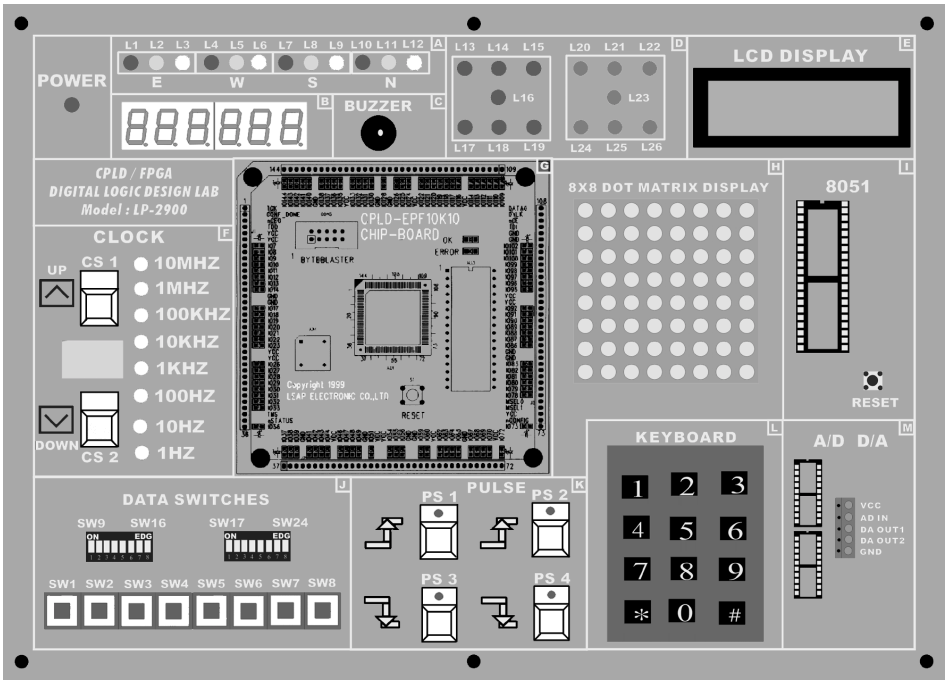


Figure 9.1 LP-2900 Logic Design Lab Platform

Taking ALTERA EPF10K10TC144-4 CPLD chip as the core, LP-2900 is designed as a multi-functional logic design lab platform, which is divided into four sections, CPLD chipboard, I/O device lab board, PC printer download interface, and power.

❖ CPLD chip board

The four parts (Figure 9.2) set on the CPLD chip board include one ALTERA 10K series chip, one EPROM chip socket, one reset bottom, and one pin status display LED (Surface Mounted Device, SMD). ALTERA EPF10K10TC144-4 CPLD chip provides a diversity and convenient rout of constant re-loading to program new circuits. To provide an alternative method to program, users can insert EPROM chip with programmed “configuration data” to EPROM chip socket. The reset bottom is set to allow 10K chip to exit the user mode and enter into the command mode. After configuring the circuits and resetting, it will progress to re-activate the user mode. The programming methods introduced in this book allow 10K chip automatically exit user mode, enter into the command mode to configure and reset and then re-activate the user mode. Thus, it is not necessary to push the reset bottom before downloading. The pin status display LED is a SMD, showing the status of each pin after the power turns on, for detecting the situation of the circuits.

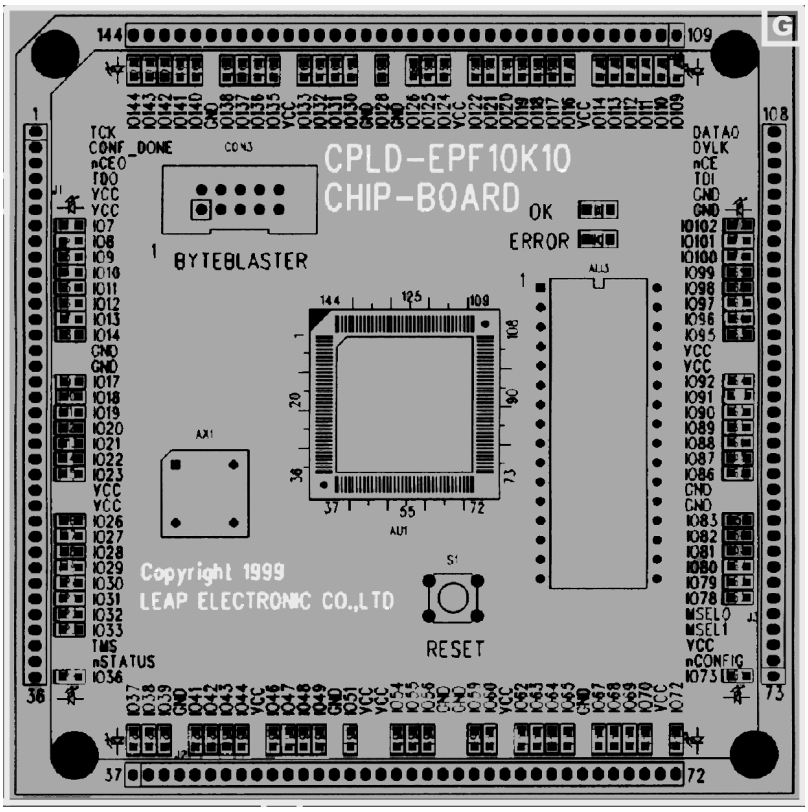


Figure 9.2 CPLD chip-board

❖ I/O device lab board

The big board under the CPLD chipboard is the I/O device lab board. There are 12 I/O devices on the board, which are (1) 4 sets of Red-Yellow-Green LED; (2) 6 common cathode 7 segment display; (3) one buzzer; (4) 2 electronic dices; (5) one clock circuit; (6) 3 sets of 8-bit data switch; (7) 4 pulse bottom; (8) one frequently-used 4 × 3 keyboard; (9) one 8 × 8 dot matrix LED display; (10) one LCD; (11) A/D & D/A circuit module; and (12) 8051 single chip module. The board contains all frequent-used I/O devices of digital logic circuits to provide a learning comprehend environment.

❖ PC printer download interface circuit

The circuit provides downloading “configuration data” from PC printer port that is a

convenient rout for programming 10K chip. It saves the trivial works for disassembling to set the interface. The only job that takes is to connect printer bus line to PC printer port.

❖ **Power**

AC 90V~260V, 50Hz/60Hz, DC 5V, 2A input, providing all the power needed for all circuits and it has a short-circuit-protected measure.

LP-2900 CPLD Logic Design Lab Platform should be used with ALTERA MAX+PLUS II software. Currently, the top three popular versions in the market of Taiwan are (1) Business Version (9.1 version, February 1999). To make the whole functions work, it requires a connecting key-pro to the printer port. (2) Student Version (7.21SE version, June 1999). Required by the US universities to apply CPLD courses, 7.21SE Version is designed for educating. Although this version does not provide functional simulation (except timing simulation), and only supply 2 types of chip, EPM7128S and EPF10K20, however, it provides VHDL design environment. (3) Baseline Version (9.23 Version, June 1999). Except for VHDL design environment, it provides a design environment as graphic entry, text entry, and waveform entry. Meanwhile, it provides functional and timing simulations. This version can be used with any ALTERA chips. For free download and usage of Student and Baseline Version, please login at http://www.altera.com.

The features of LP-2900 CPLD Logic Design Lab Platform are：

1. Easy to setup and collect;
2. Clear description on the board for easier operation;
3. EPF10K10TC144-4 CPLD chip on the CPLD chipboard provides constant reloading for programming new circuits. This is very flexible and

convenient. Meanwhile, EPF10K10TC144-4 chip offers a wide range circuit application from tiny to large circuits.

4. The pin status display of SMD LED shows the current status of each pin. This equipment is quite convenient for circuit detection.
5. I/O device lab-board comprises most of the I/O devices required for digital logic circuit, providing a comprehensive learning environment.
6. Used with MAX+PLUS II, it provides an integrated environment of design, simulation, and verification of digital circuit. This integrated environment can not only ease the universities' courses on digital logic design, digital circuit design, digital system design and VHDL digital circuit design but also provide an excellent environment for the department of R&D to develop circuits.
7. The book "CPLD Logic Circuit Design and Practice" is edited by graphic-oriented, arranged from simple to sophisticated, draw out a lots of illustrations, instruct with detail descriptions. Teaching with that book to present logic design instruction and practices, and unite theories and phenomenon testimony are the brand new teaching methodology.
8. To complete the combined circuit practices using 8051 and CPLD.
9. Compatible with WIN95/98/2000/NT working systems.

9.2 Setting up LP-2900

❖ **Setting up LP-2900 CPLD Logic Design Lab Platform**

It requires only two steps to setup LP-2900,

1. Connecting the power cord with 110V socket；
2. Connecting one terminal of the printer bus line with the parallel port of PC,

which has MAX+PLUS II, and the other with the parallel port of LP-2900 CPLD Logic Design Lab Platform.

9.3 The Architecture and Circuits of LP-2900

1. Figure 9.3 illustrates LP-2900 Lab-Platform is composed by four parts, CPLD chipboard, I/O Lab-board, PC printer download interface and power.
2. Figure 9.4 demonstrates the connection status of the three components on the CPLD chipboard. There are module connector, CLPD chip, and ISP download bus connector.
3. Figure 9.5 illustrates the connection status of the eleven parts on the I/O Lab-board that are module connector, buzzer, 7 segment display, clock, pulse keys, 8 ×8 dot matrix display, LCD module, 4 ×3 keyboard module, 8051 single chip, A/D & D/A module, and LED display, including the LED of dice array.
4. Figure 9.6 describes the connection of EPF10K10TC144-4.
5. Figure 9.7 is the socket layout of the chip module.
6. Figure 9.8 is the circuit layout of I/O status LED on chip module.
7. Figure 9.9 is the download interface of EEPROM and printer parallel port.
8. Figure 9.10 illustrates the connection on I/O Lab-board.
9. Figure 9.11 demonstrates the module connector on CPLD chipboard.
10. Figure 9.12 is the LED display driver on I/O Device Lab-board.
11. Figure 9.13 is the driver of 7-segment display and buzzer on I/O Device Lab-board.
12. Figure 9.14 is the buttons of pulse and clock up/down on I/O Device Lab-board.

13. Figure 9.15 is the circuits of 8 × 8 Dot Matrix Display, LCD module, and 4 ×3 keyboard.
14. Figure 9.16 is the circuits of data switch on I/O Device Lab-board, one of which is a set of 8-key with LED display.
15. Figure 9.17 illustrates A/D and D/A circuits on I/O Device Lab-board.
16. Figure 9.18 demonstrates 8 × 8 Dot Matrix Module on I/O Device Lab-board.

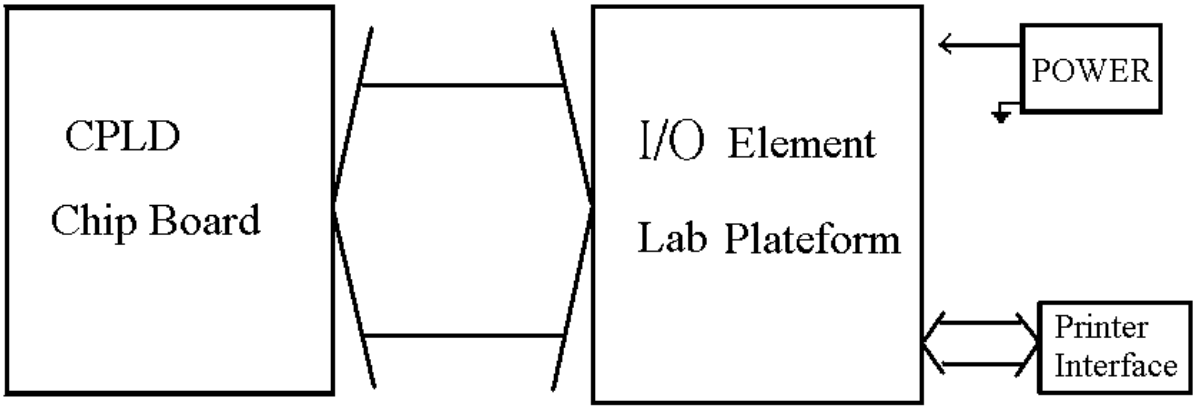


Figure 9.3 Blocks of LP-2900

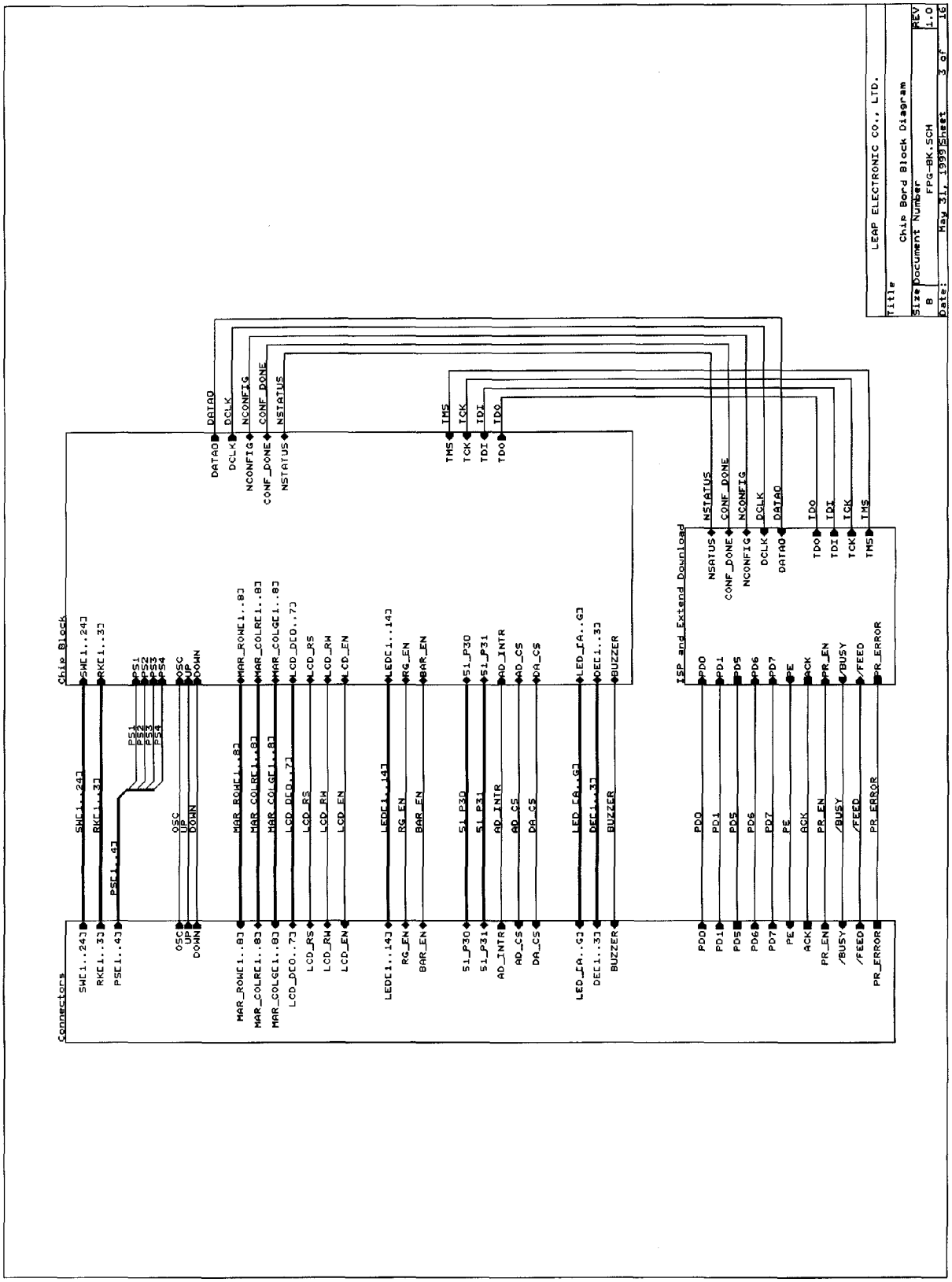


Figure 9.4 Connection of the three major parts on CPLD chip-board

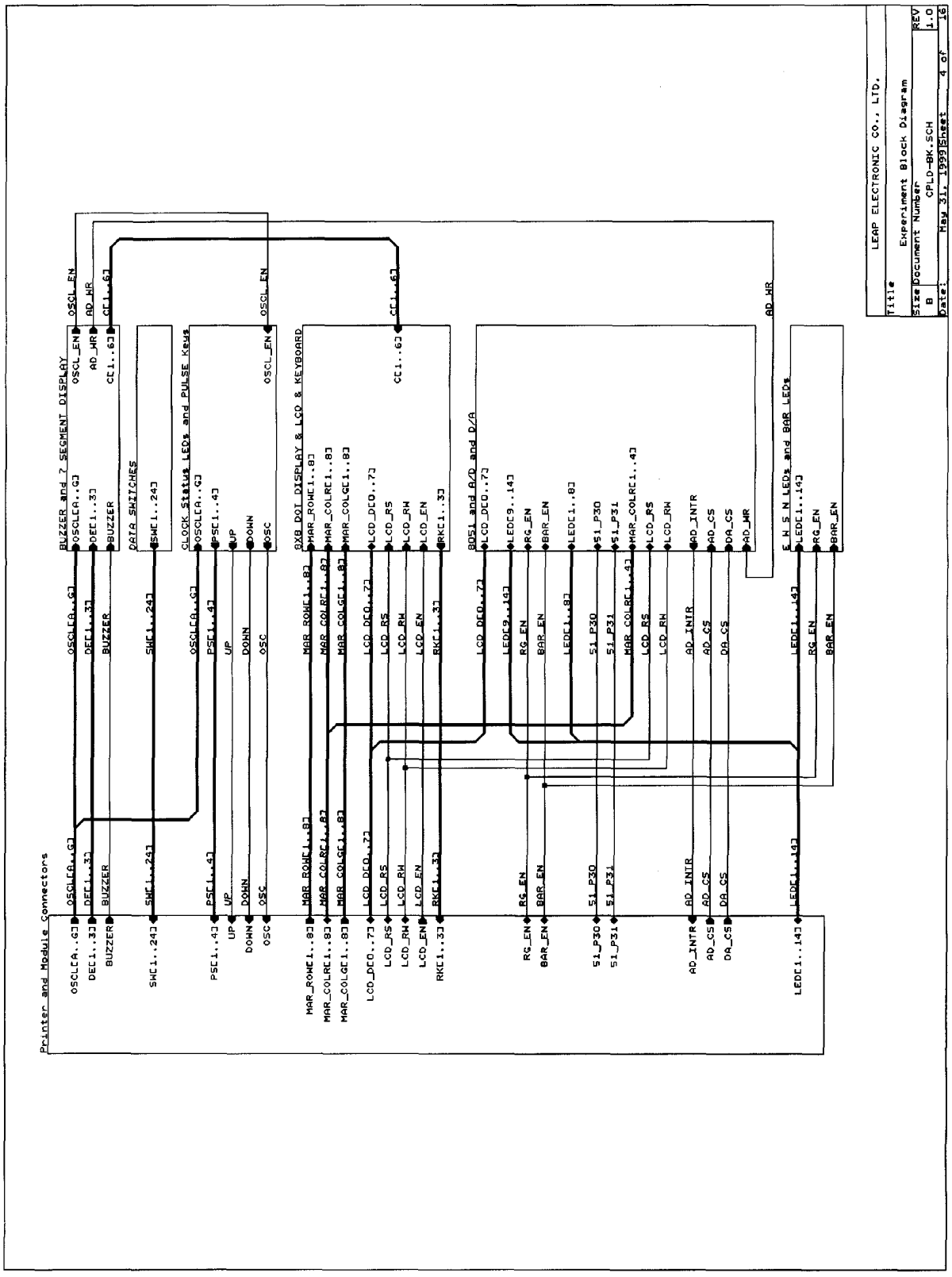


Figure 9.5 Block Diagram of I/O Device Lab-board

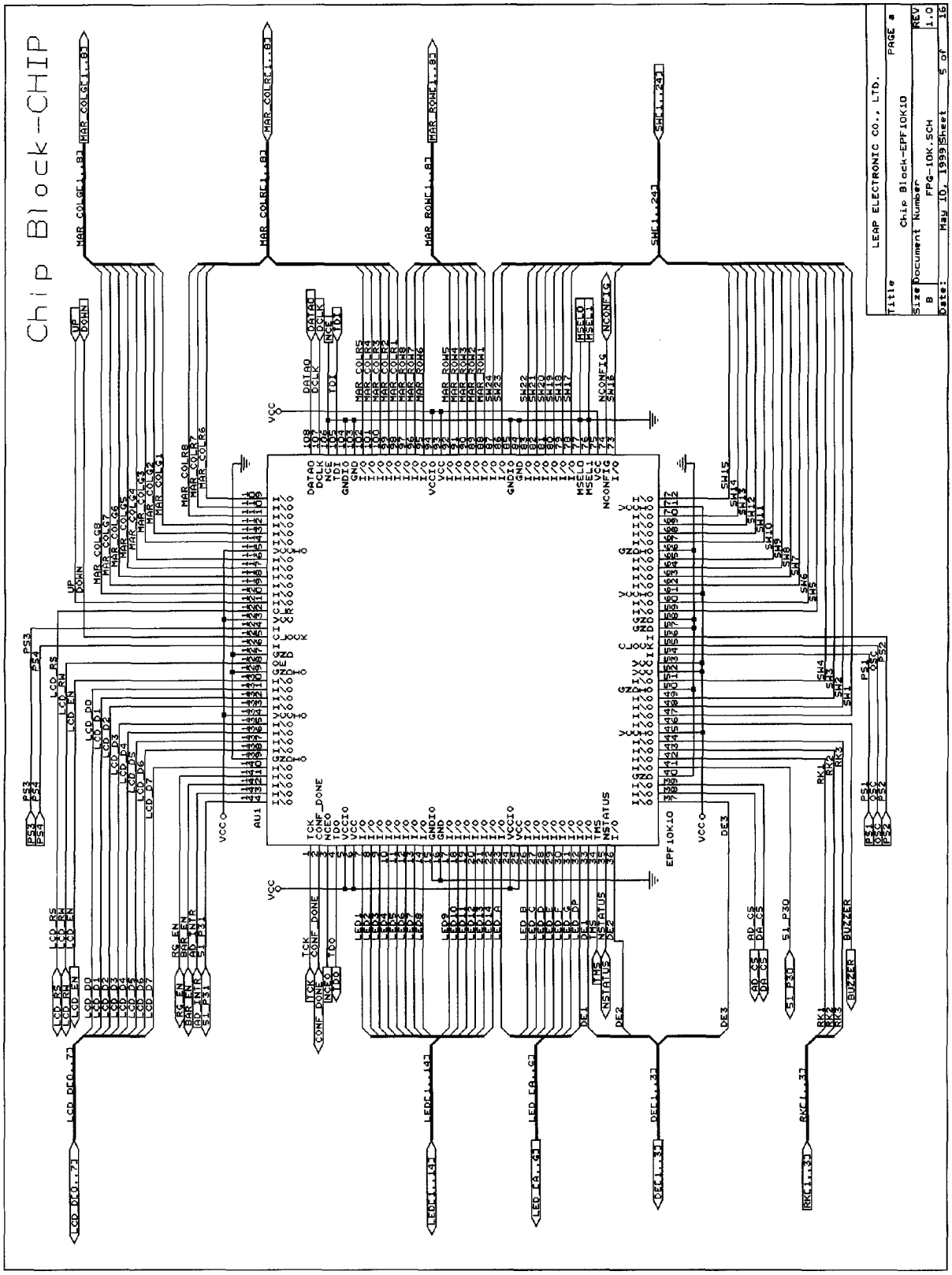


Figure 9.6 Connection of EPF10K10TC144-4

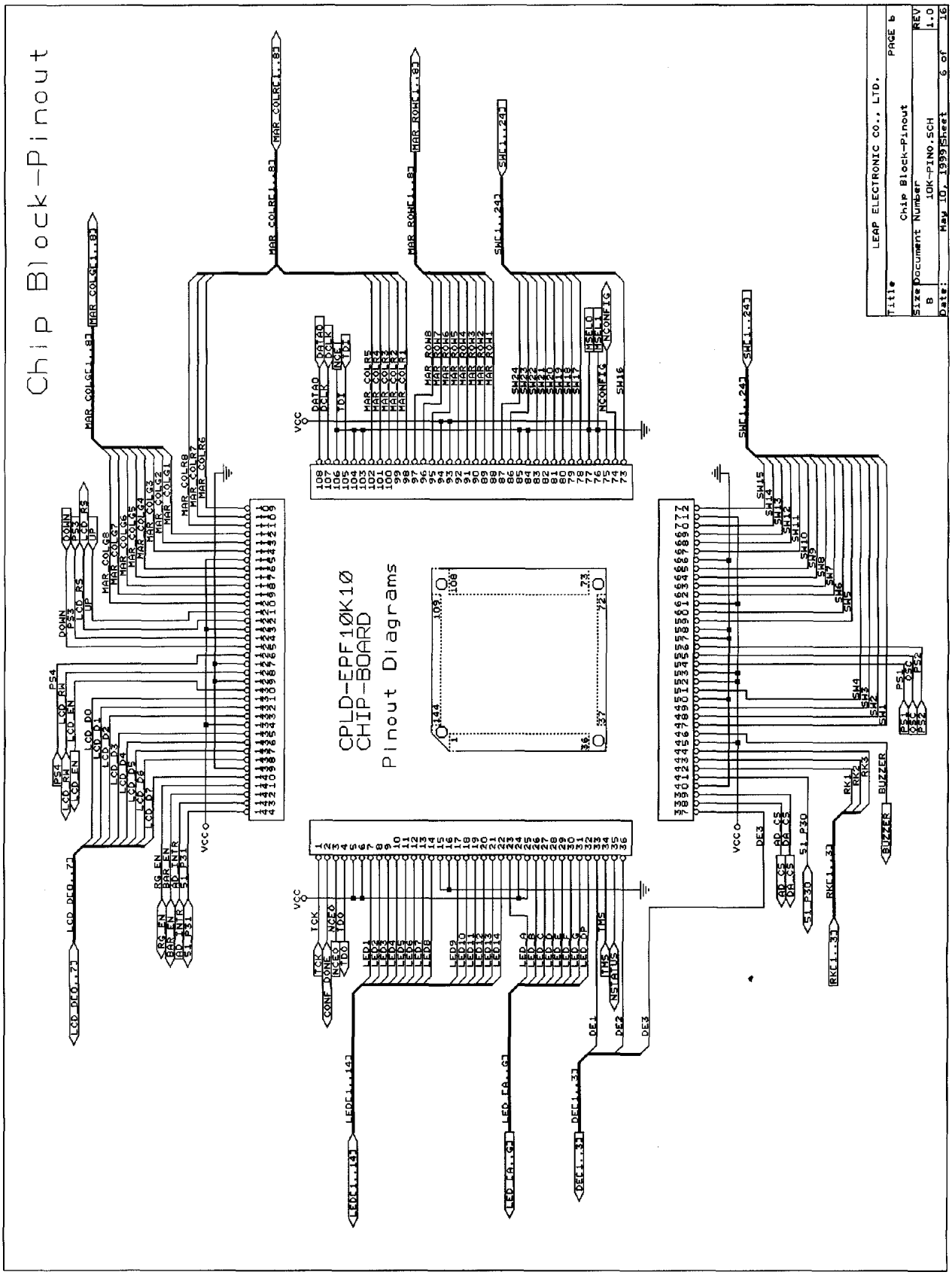


Figure 9.7 Chip Block-Pinout

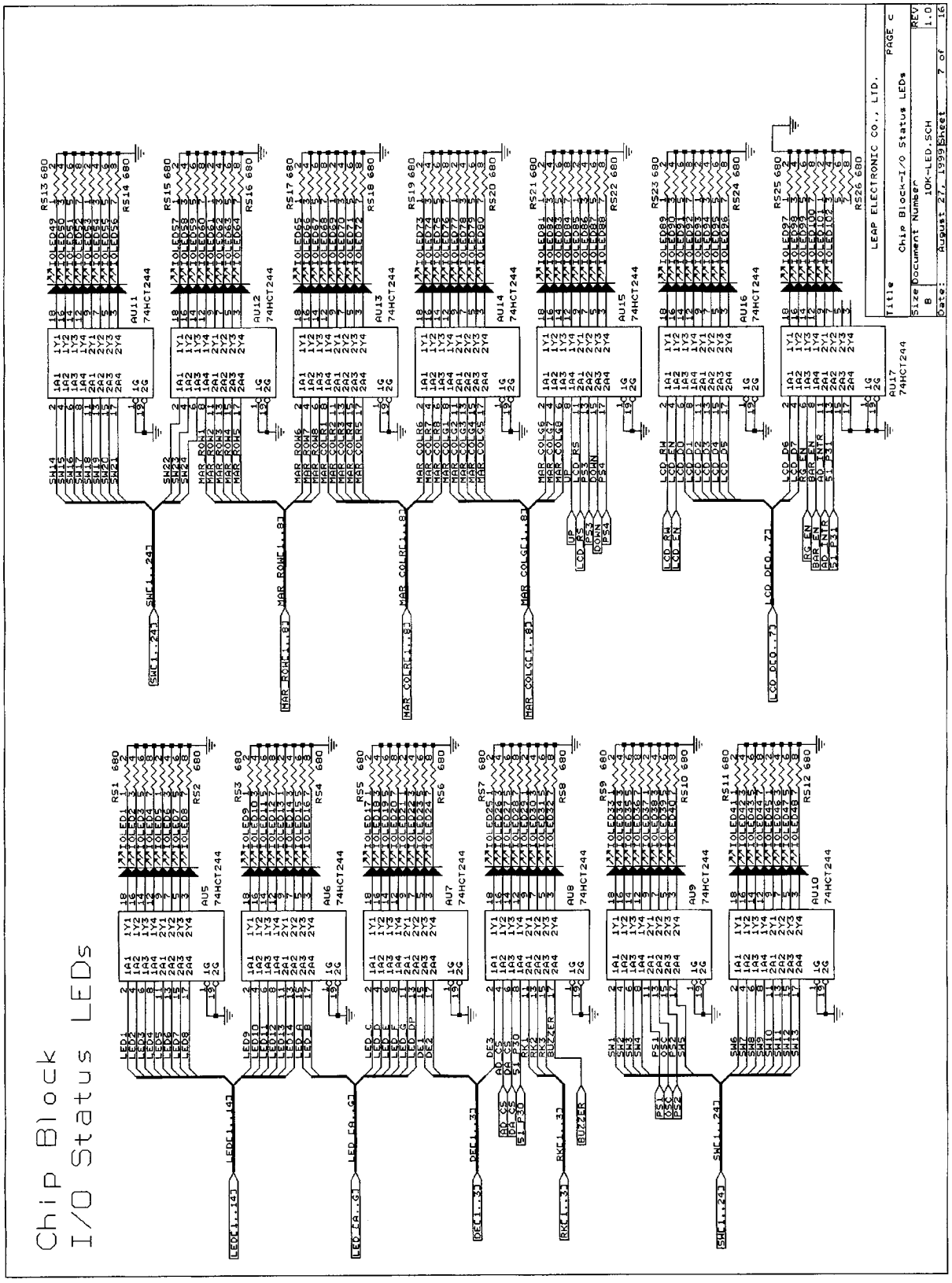


Figure 9.8 Chip Block I/O Status LEDs

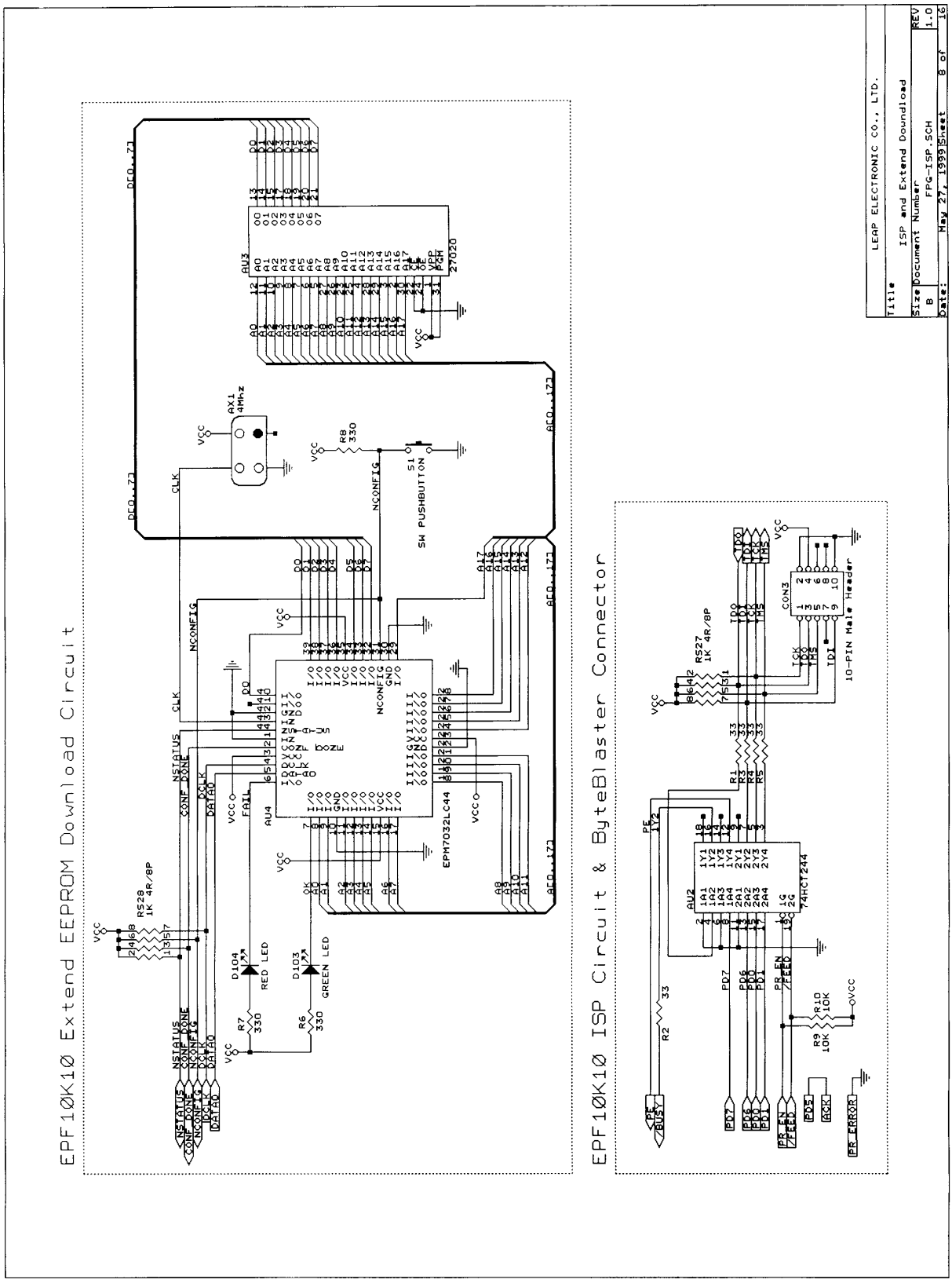


Figure 9.9 ISP and EEPROM Extend Download Circuit

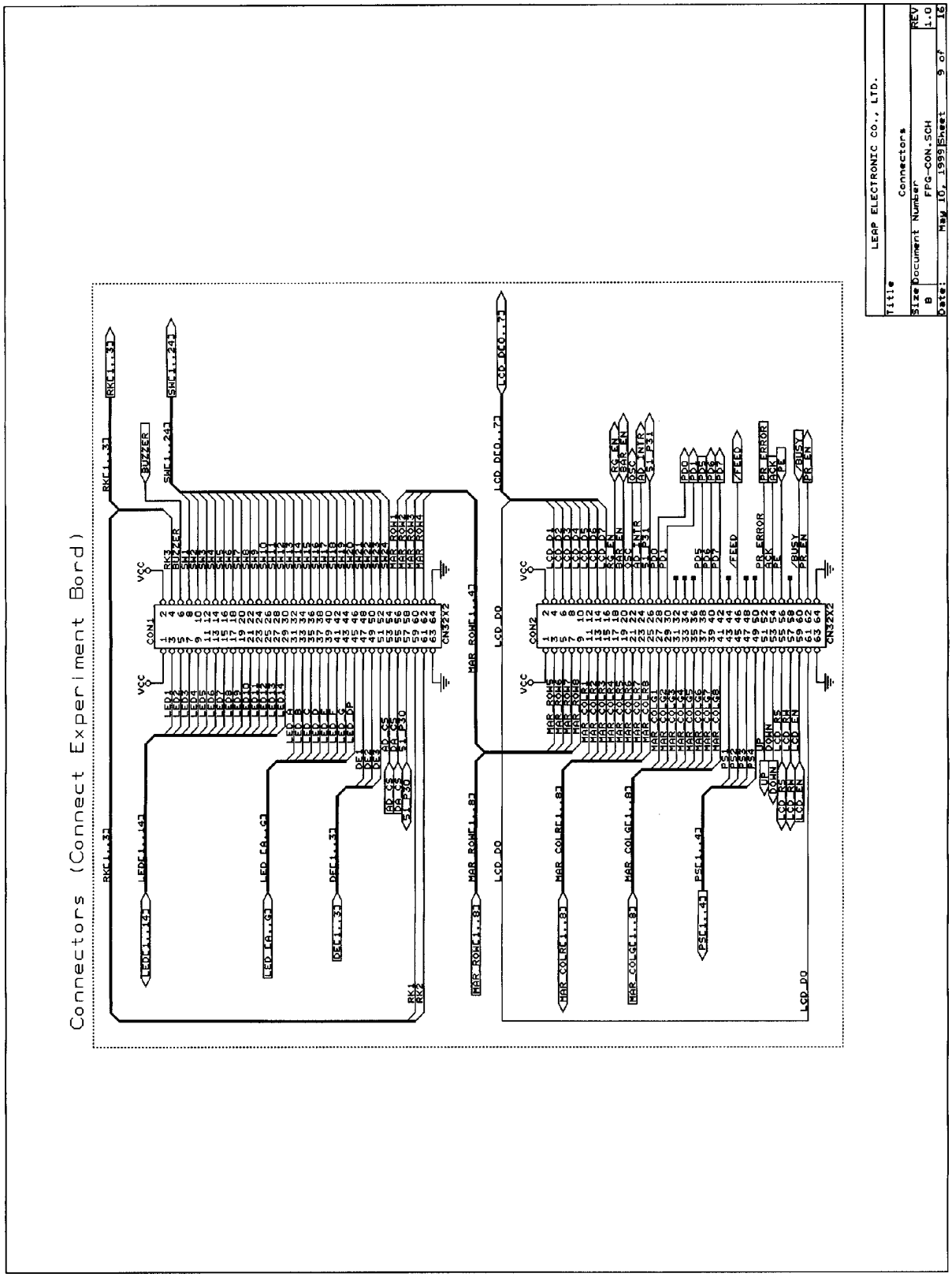


Figure 9.10 Connectors on I/O Device Lab-board

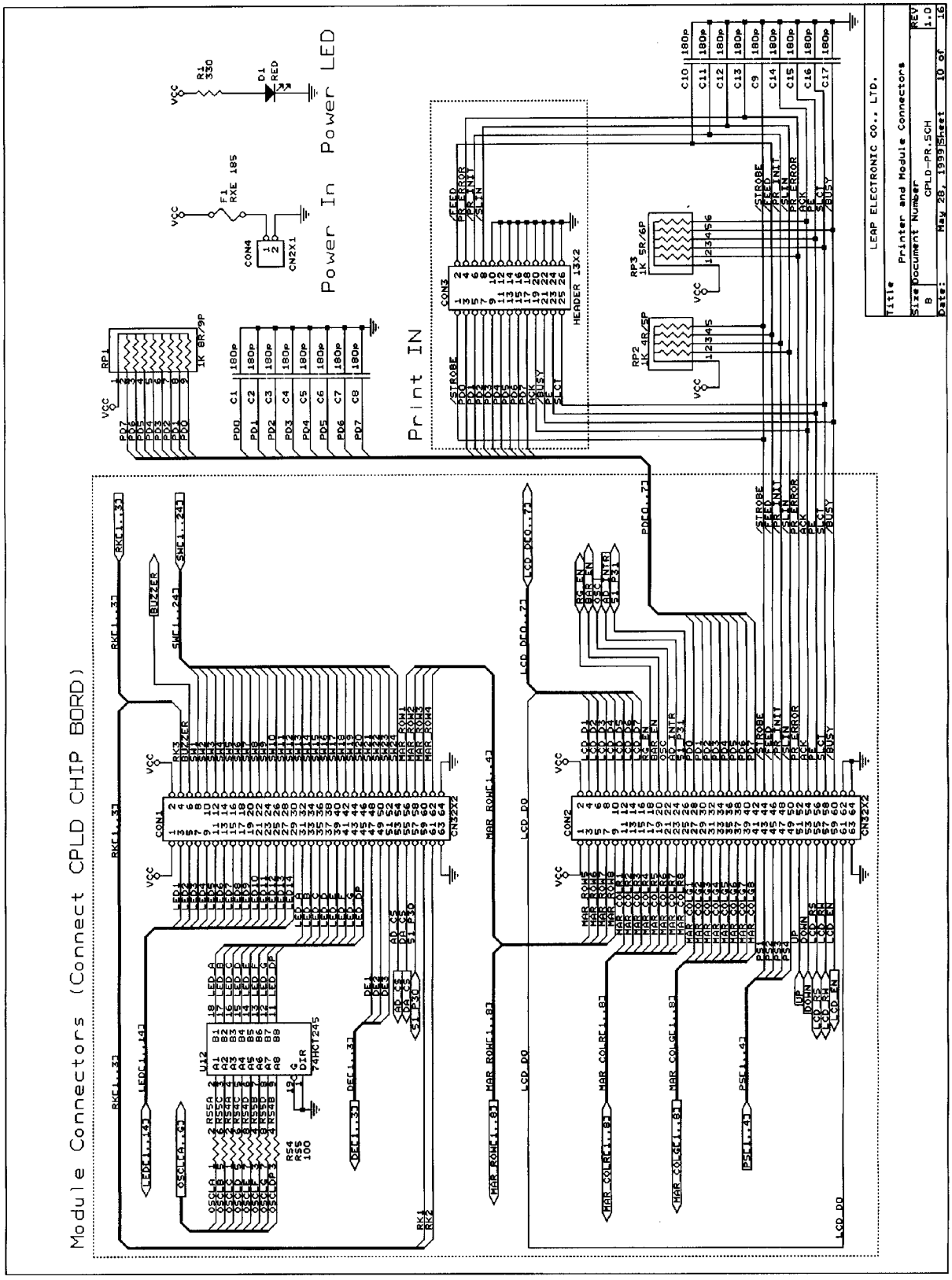


Figure 9.11 Module Connectors on CPLD chip-board

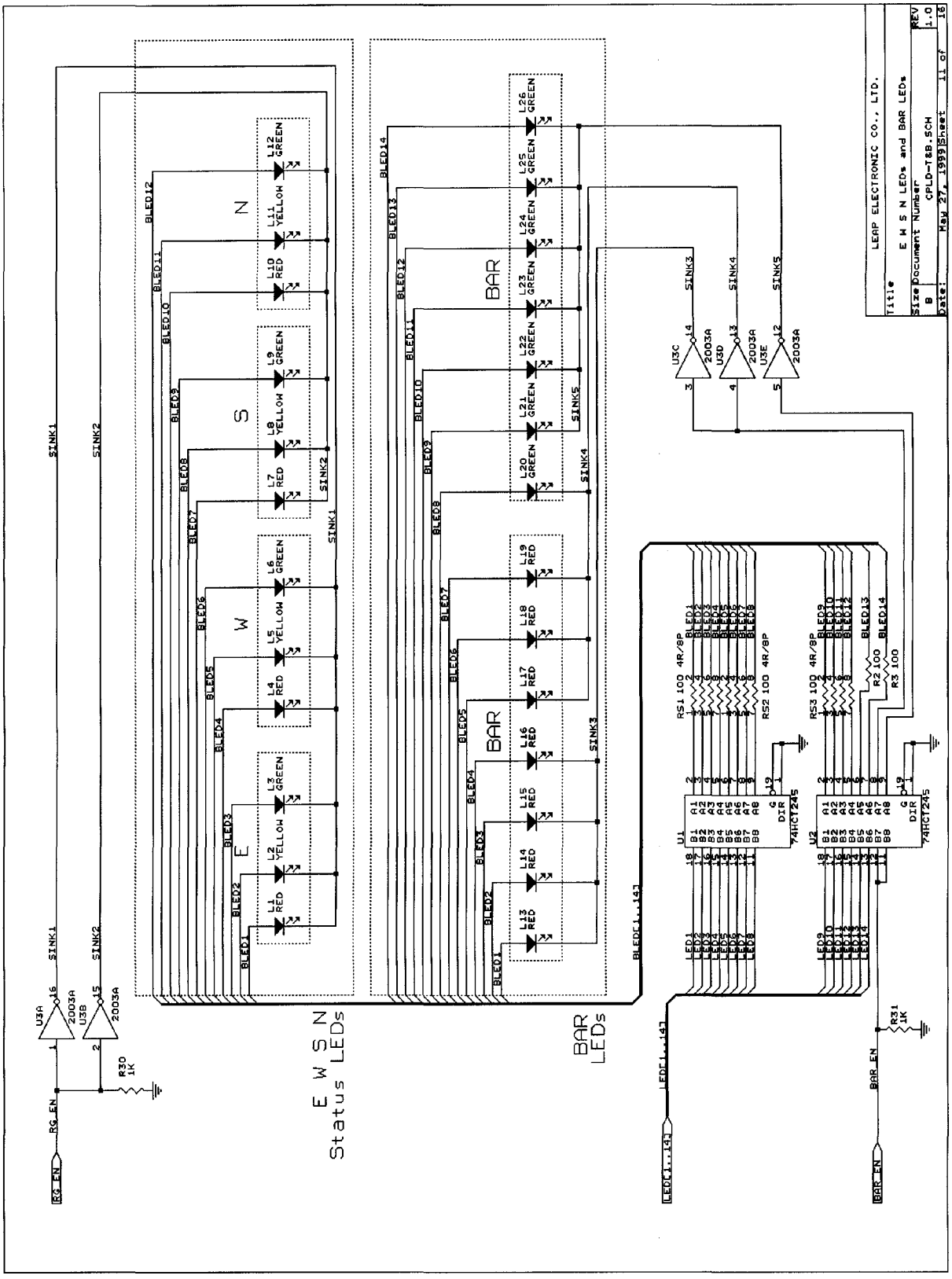


Figure 9.12 LED Display Driver on I/O Device Lab-board

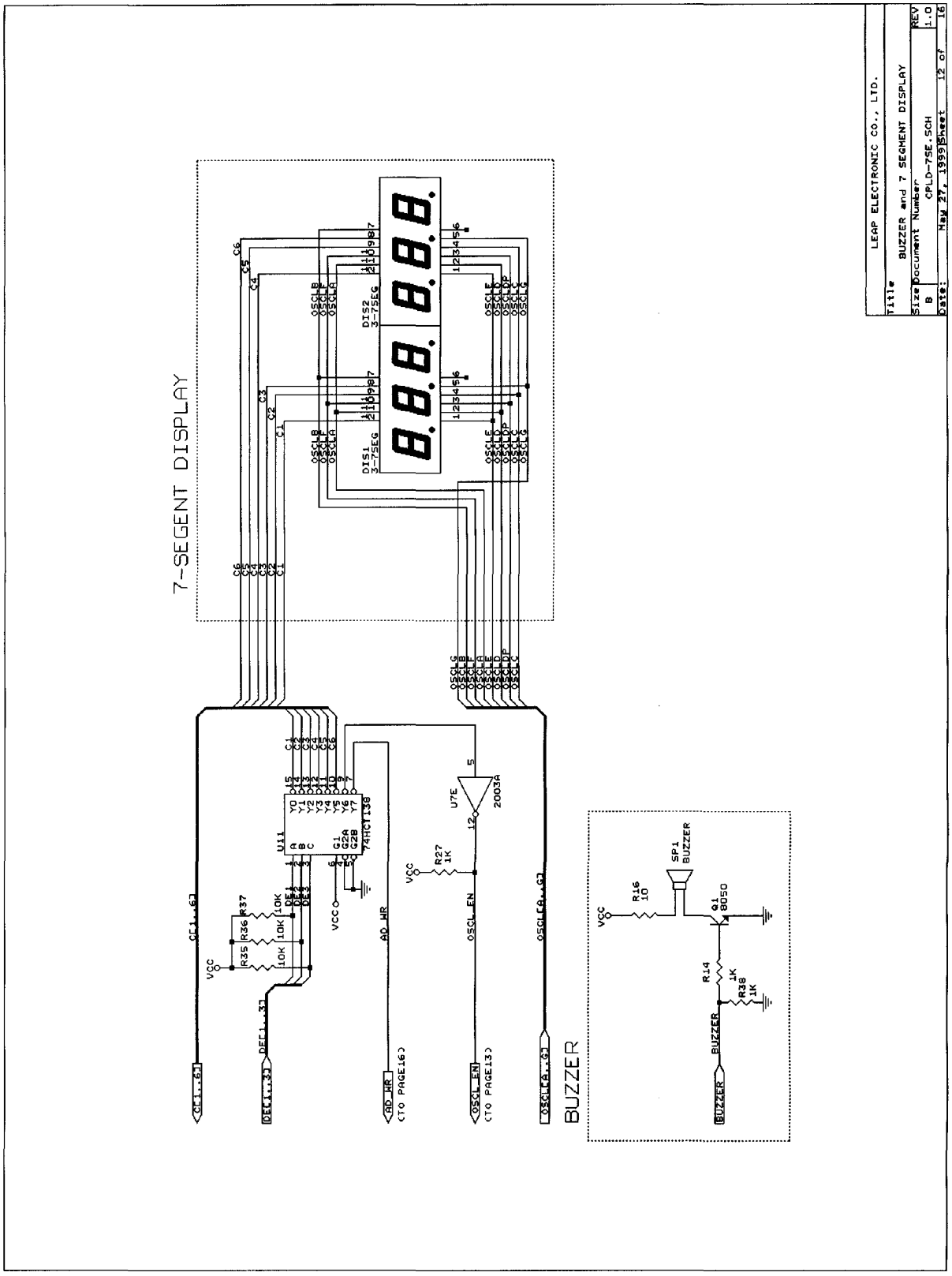


Figure 9.13 7-Segment Display and Buzzer on I/O Device Lab-board

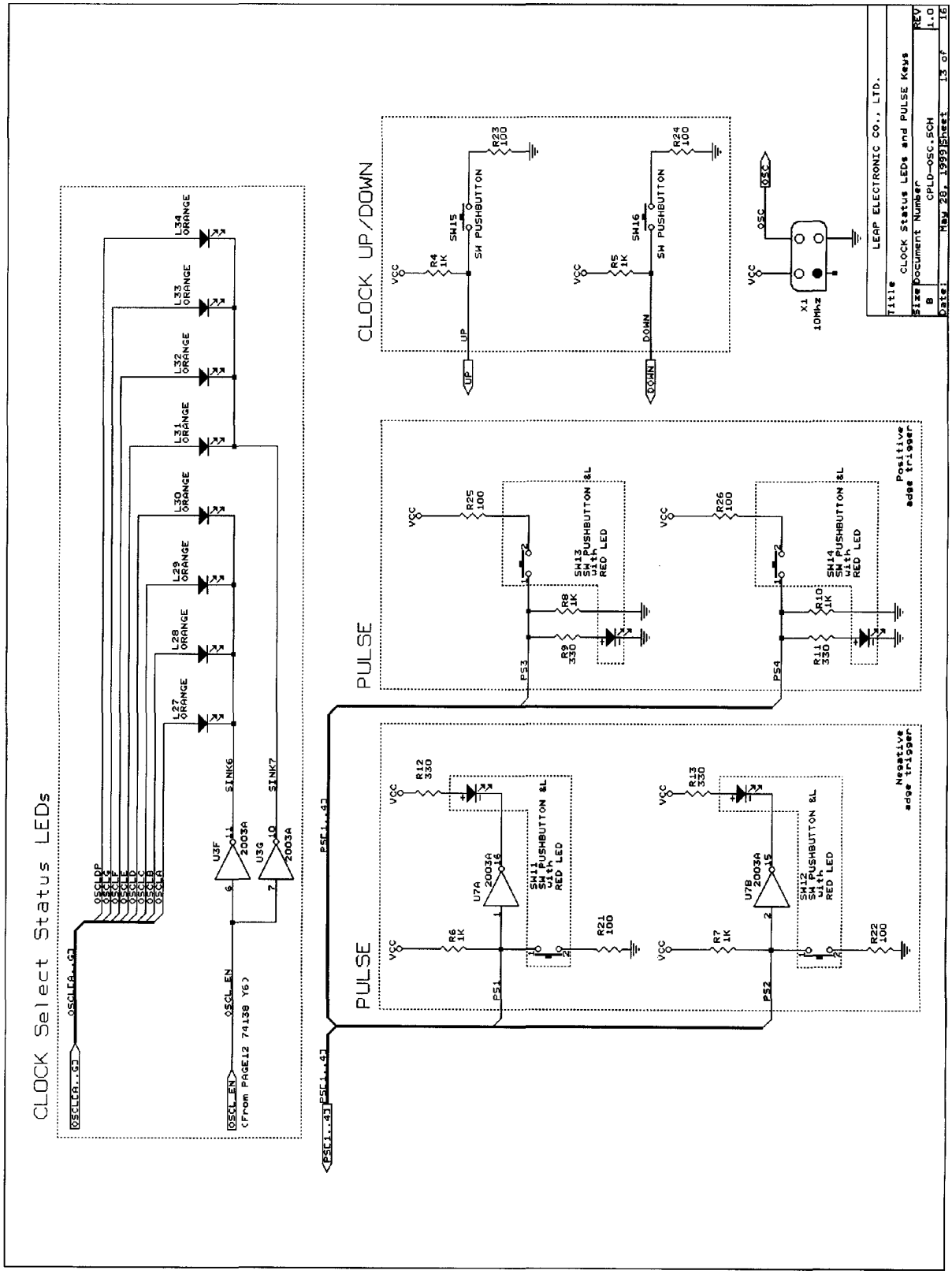


Figure 9.14 Pulse and Clock Up/Down Push Buttons on I/O Device Lab-board

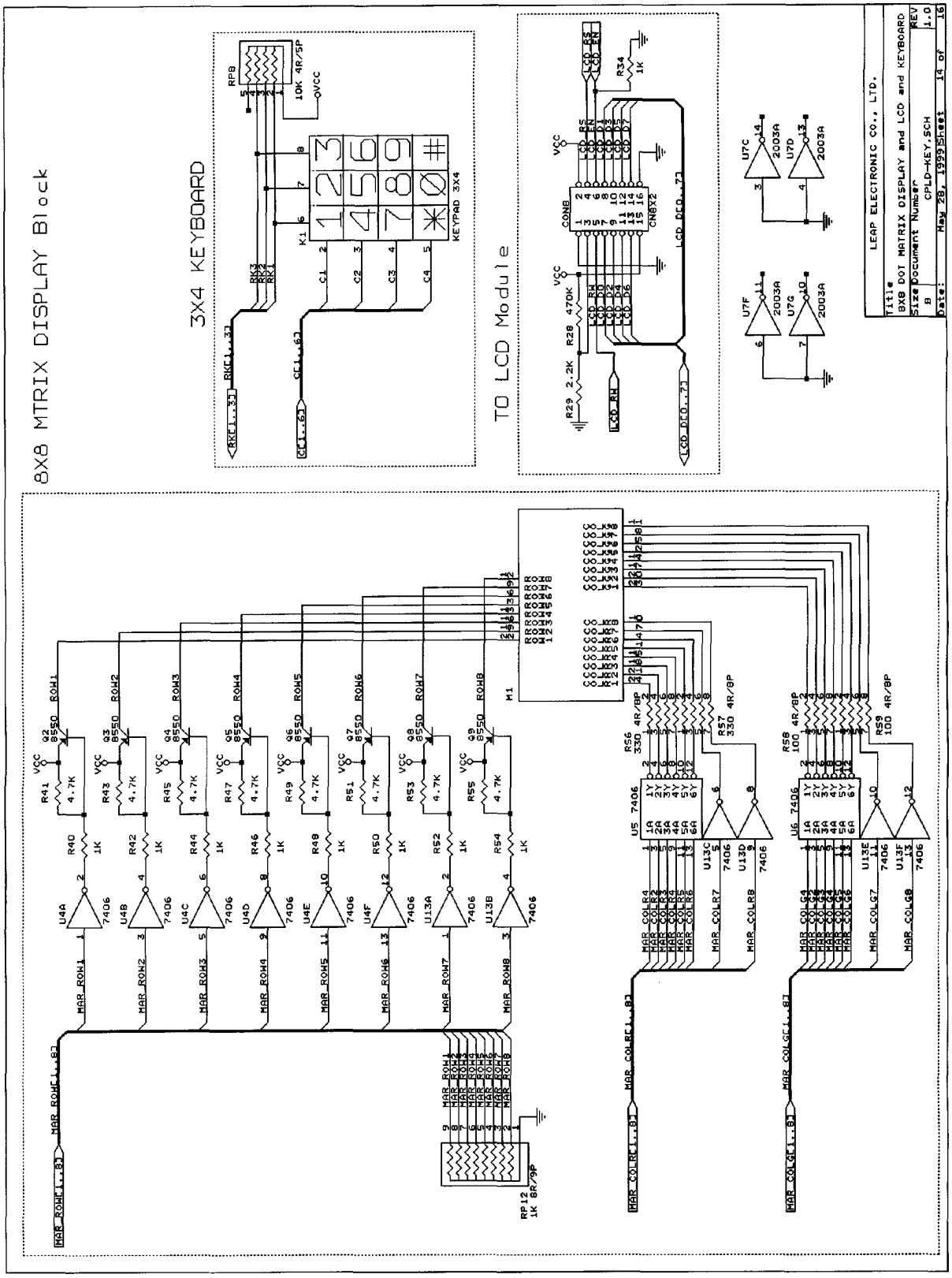


Figure 9.15 Dot Matrix Display, keyboard, and LCD Module

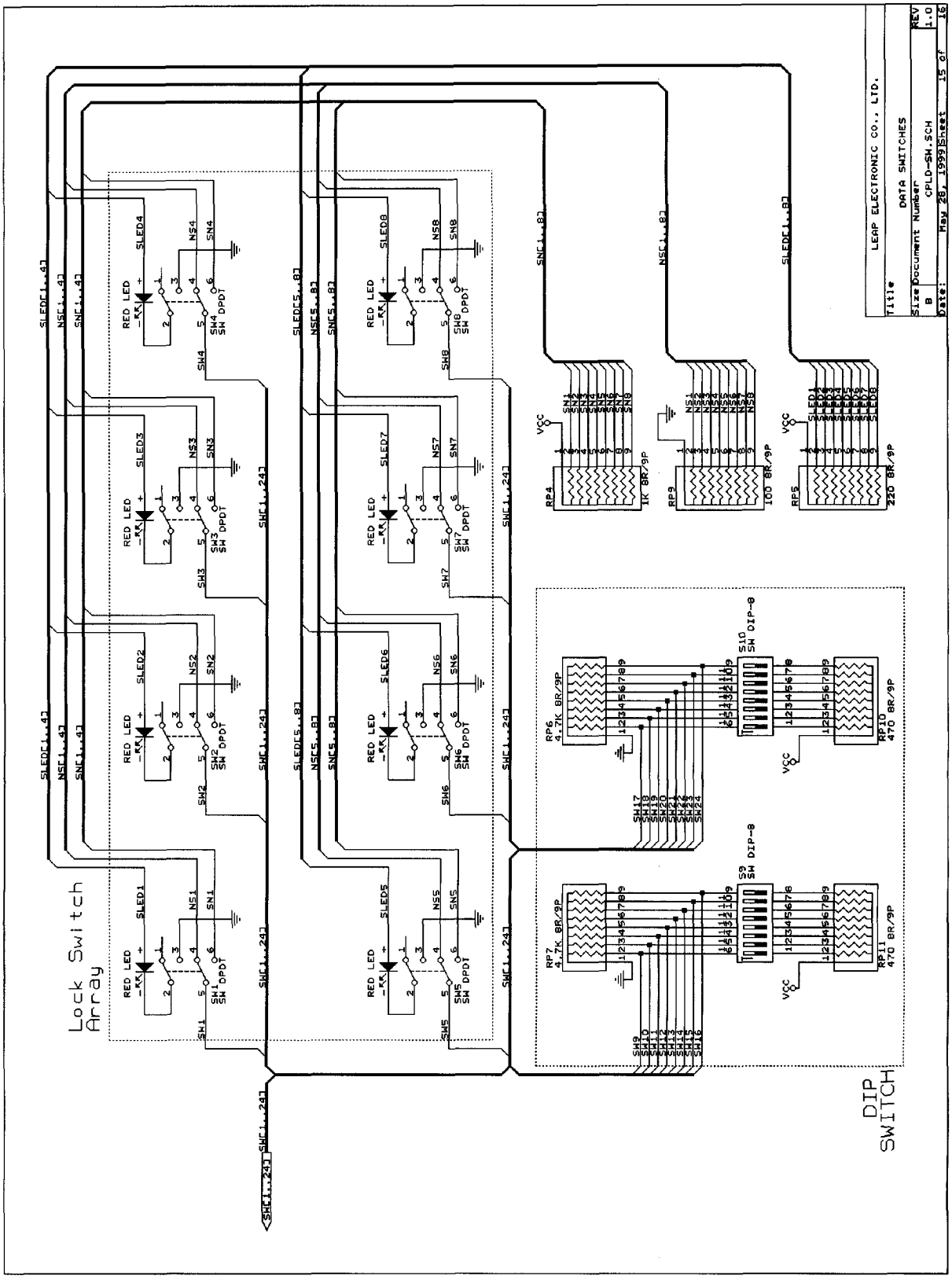


Figure 9.16 Data Switches on I/O Device Lab-board

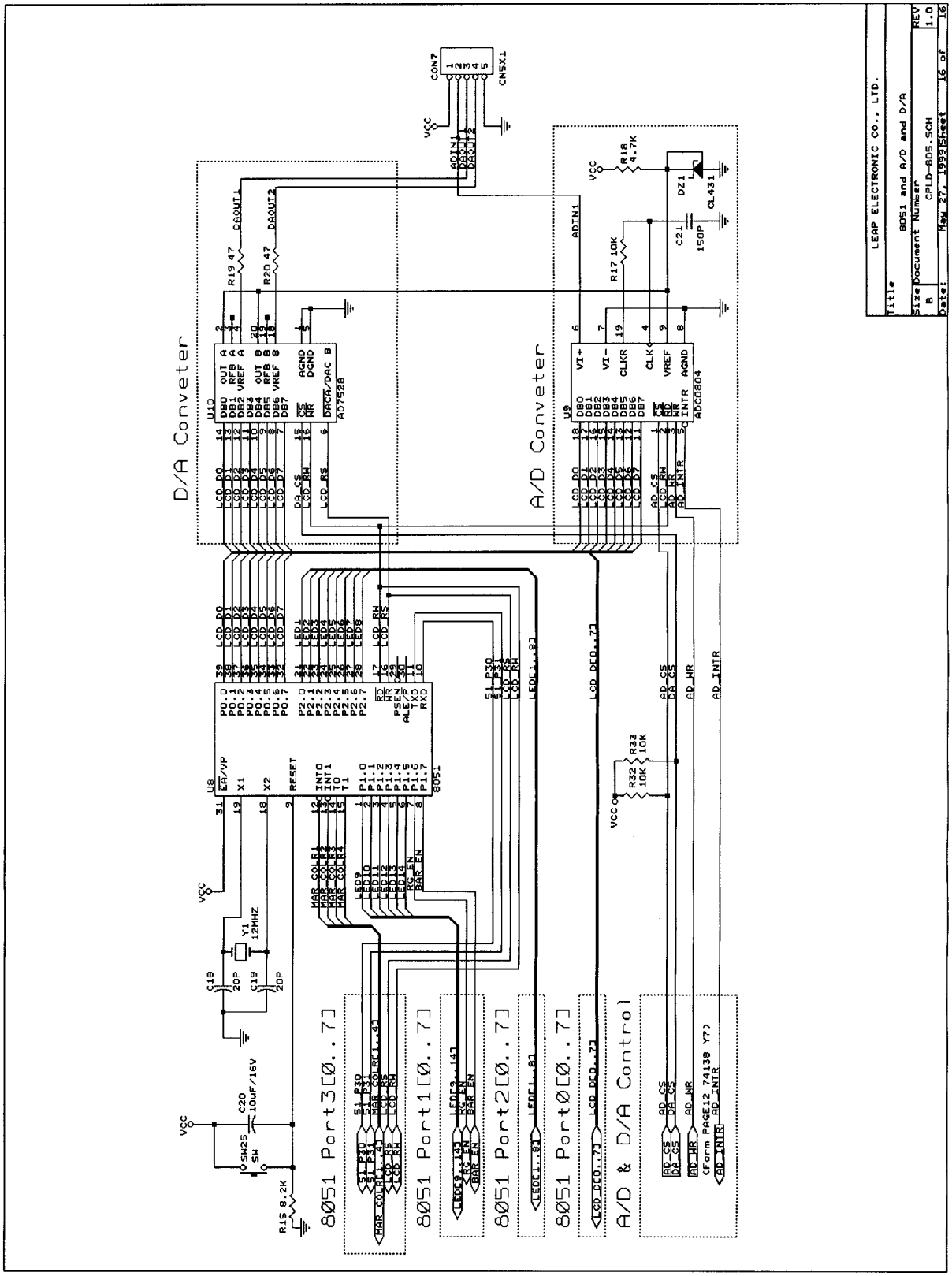


Figure 9.17 8051, A/D and D/A

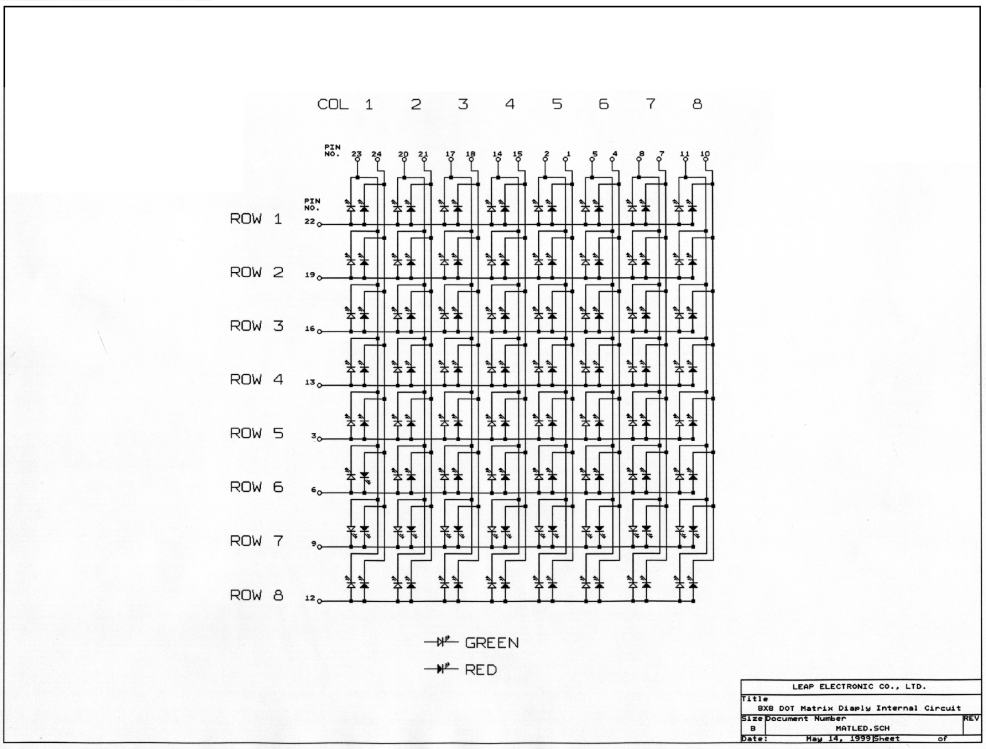
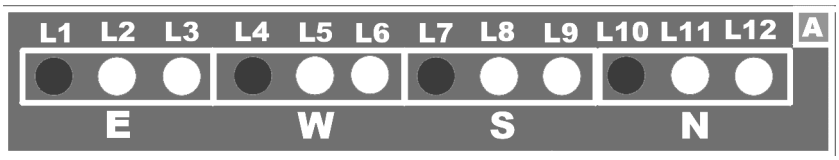


Figure 9.18 8 × 8 dot matrix module on I/O device lab board

9.4 Pin arrangement of LP-2900

Pin arrangement data, an important data that highly used, is an essential data for floor plane setup. The pin arrangement data of ALTERA EPF10K10TC144 on LP-2900 is described in detail as follows.

9.4.1 Red-Yellow-Green LED



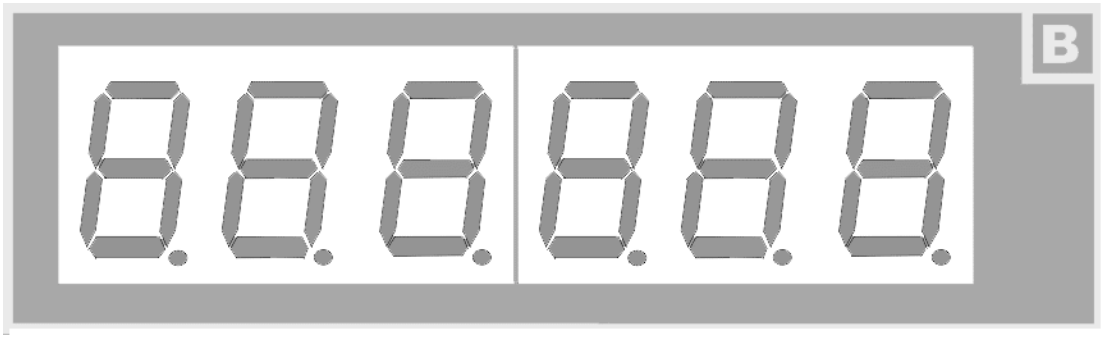
Code	L1	L2	L3	L4	L5	L6	L7	L8
Device	Red	Yellow	Green	Red	Yellow	Green	Red	Yellow
Pin	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12	Pin 13	Pin 14

Code	L9	L10	L11	L12	LED_COM
Device	Green LED	Red LED	Yellow LED	Green LED	Common cathode of LED1～LED12
Pin	Pin 17	Pin 18	Pin 19	Pin 20	Pin 141

† L1～L12 are LED anode inputs for each LED

† LED_COM is the common cathode of all LED

9.4.2 7-Segment Display with Common Cathode



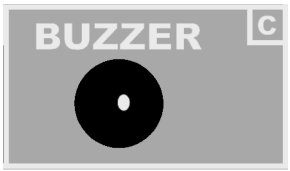
Code	A	B	C	D	E	F	G	DP
Device	7 Segment Display							
Pin	Pin 23	Pin 26	Pin 27	Pin 28	Pin 29	Pin 30	Pin 31	Pin 32

Code	DE1	DE2	DE3	—	—	—	—	—
Device	74138			—	—	—	—	—
Pin	Pin33	Pin36	Pin37	—	—	—	—	—

† DE1, DE2 and DE3 are connected to 74138 which outputs Y0～Y5 as C1～C6.

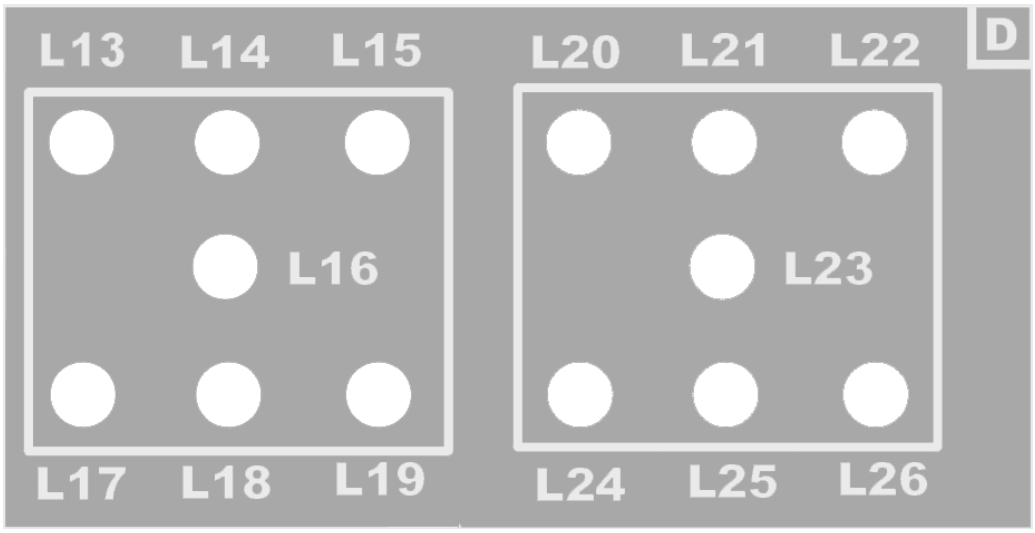
† C1～C6 are the common cathodes of 6 7-segment display.

9.4.3 BUZZER



Code	SP1
Device	Sp1
Pin	Pin 46

9.4.4 Electronic Dice



Code	L13	L14	L15	L16	L17	L18	L19
Device	Red Dice						
Pin	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12	Pin 13

Code	L20	L21	L22	L23	L24	L25	L26
Device	Green Dice						
Pin	Pin 14	Pin 17	Pin 18	Pin 19	Pin 20	Pin 21	Pin 22

Code	Dice_COM	—	—	—	—
Device	Common cathode of L13～L26	—	—	—	—
Pin	Pin 142	—	—	—	—

† L13～L26 are anode inputs for each LED

† Dice_COM is the common cathode of L13～L26

9.4.5 LCD display

Code	EN	RS	RW	D0	D1	D2	D3	D4
Device	LCD							
Pin	Pin 130	Pin 122	Pin 128	Pin 131	Pin 132	Pin 133	Pin 135	Pin 136

Code	D5	D6	D7	—	—	—	—	—
Device	LCD			—	—	—	—	—
Pin	Pin 137	Pin 138	Pin 140	—	—	—	—	—

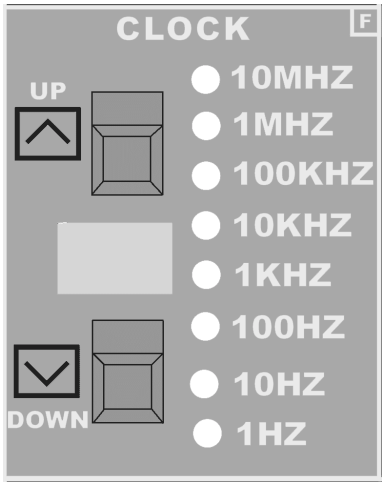
9.4.6 CLOCK

Code	L27	L28	L29	L30	L31	L32	L33	L34
Device	Yellow LED							
Pin	Pin 23	Pin 26	Pin 27	Pin 28	Pin 29	Pin 30	Pin 31	Pin 32

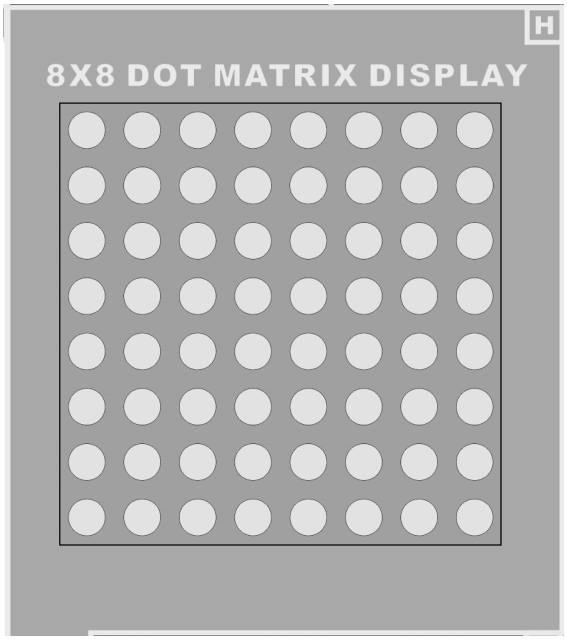
Code	DE1	DE2	DE3
Device	74138		
Pin	Pin 33	Pin 36	Pin 37

Code	OSC	UP	DOWN
Device	OSC	Button	Button
Pin	Pin 55	Pin 121	Pin 125

† DE1, DE2 and DE3 are connected with 74138 which output Y6 as common cathode of L27～L34.



9.4.7 8 x 8 Dot Matrix LED Display



❖ **Common Anodes**

Code	Row 1	Row 2	Row 3	Row 4	Row 5	Row 6	Row 7	Row 8
Device	8 ×8 Dot Matrix							
Pin	Pin 88	Pin 89	Pin 90	Pin 91	Pin 92	Pin 95	Pin 96	Pin 97

❖ **Red Cathodes**

Code	CR1	CR2	CR3	CR4	CR5	CR6	CR7	CR8
Device	8 ×8 Dot Matrix							
Pin	Pin 98	Pin 99	Pin 100	Pin 101	Pin 102	Pin 109	Pin 110	Pin 111

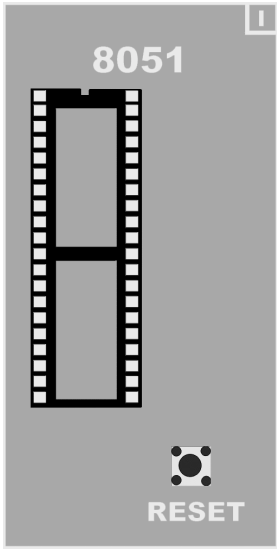
† CR1～CR8 driven by HI

❖ **Green Cathodes**

Code	CG1	CG2	CG3	CG4	CG5	CG6	CG7	CG8
Device	8 ×8 Dot Matrix							
Pin	Pin 112	Pin 113	Pin 114	Pin 116	Pin 117	Pin 118	Pin 119	Pin 120

† CG1～CG8 driven by HI

9.4.8 8051 Single Chip



Code	P0.0	P0.1	P0.2	P0.3	P0.4	P0.5	P0.6	P0.7
Device	8051							
Pin	Pin 131	Pin 132	Pin 133	Pin 135	Pin 136	Pin 137	Pin 138	Pin 140

† P0.0～P0.7 also connect with D0～D7 of LCD

Code	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
Device	8051							
Pin	Pin 17	Pin 18	Pin 19	Pin 20	Pin 21	Pin 22	Pin 141	Pin 142

† P1.0～P1.7 also connect L21～L26 and LED_COM and Dice_COM。

Code	P2.0	P2.1	P2.2	P2.3	P2.4	P2.5	P2.6	P2.7
Device	8051							
Pin	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12	Pin 13	Pin 14

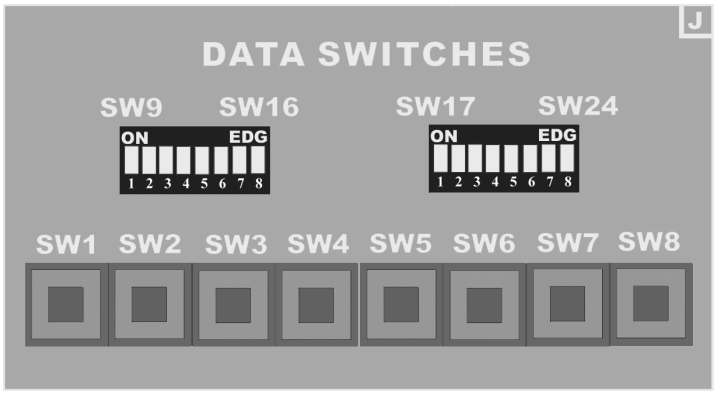
† P2.0～P2.7 also connect L1～L8。

Code	P3.0	P3.1	P3.2	P3.3	P3.4	P3.5	P3.6	P3.7
Device	8051							
Pin	Pin 41	Pin 144	Pin 98	Pin 99	Pin 100	Pin 101	Pin 122	Pin 128

† P3.2～P3.5 also connect CR1~CR4 on 8 × 8 Dot Matrix

† P3.6～P3.7 also connect RS and RW on LCD

9.4.9 DATA SWITCHES

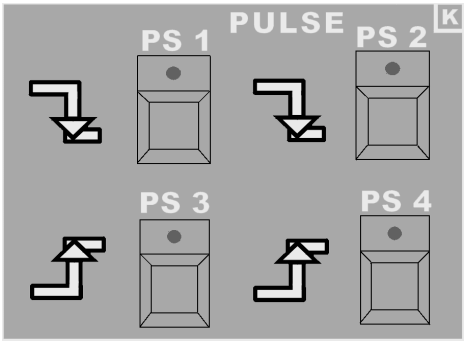


Code	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Device	Push Button							
Pin	Pin 47	Pin 48	Pin 49	Pin 51	Pin 59	Pin 60	Pin 62	Pin 63

Code	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Device	Dip Switch							
Pin	Pin 64	Pin 65	Pin 67	Pin 68	Pin 69	Pin 70	Pin 72	Pin 73

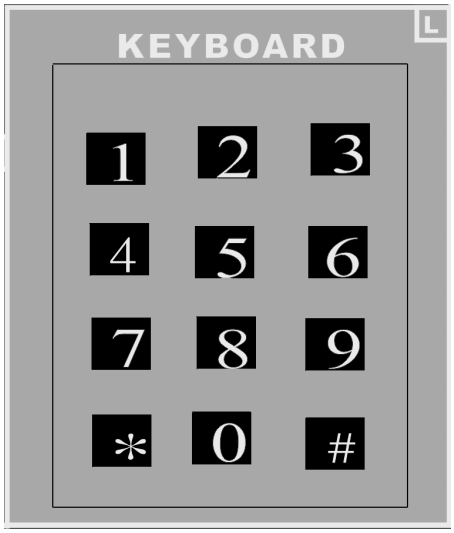
Code	SW17	SW18	SW19	SW20	SW21	SW22	SW23	SW24
Device	Dip Switch							
Pin	Pin 78	Pin 79	Pin 80	Pin 81	Pin 82	Pin 83	Pin 86	Pin 87

9.4.10 PULSE



Code	PS1	PS2	PS3	PS4
Device	Push Button with LED			
Pin	Pin 54	Pin 56	Pin 124	Pin 126

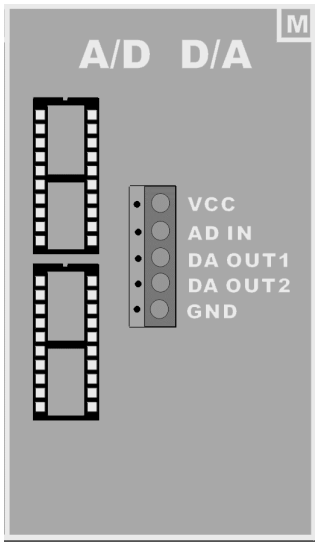
9.4.11 KEYBOARD



Code	DE1	DE2	DE3	RK1	RK2	RK3
Device	KEYBOARD					
Pin	Pin 33	Pin 36	Pin 37	Pin 42	Pin 43	Pin 44

† DE1, DE2 and DE3 are connected to 74138 which outputs Y0～Y3 connect to C1～C4 on the keyboard.

9.4.12 A/D, D/A



❖ **A/D → ADC0804**

Code	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
Device	ADC0804							
Pin	Pin 131	Pin 132	Pin 133	Pin 135	Pin 136	Pin 137	Pin 138	Pin 140

† DB0～DB7 also connect D0~D7 on LCD

Code	/CS	/RD	DE1	DE2	DE3	AD_INTR
Device	ADC0804					
Pin	Pin 38	Pin 128	Pin 33	Pin 36	Pin 37	Pin 143

† AD_WR connect to the output Y6 of 74138.

† DE1, DE2 and DE3 are connected to 74138 as inputs.

† /RD also connect RW on LCD

❖ **D/A-->AD7528**

Code	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
Device	AD7528							
Pin	Pin 131	Pin 132	Pin 133	Pin 135	Pin 136	Pin 137	Pin 138	Pin 140

† DB0～DB7 also connect D0~D7 on LCD

Code	/CS	/WR	/DACA	—	—	—	—	—
Device	AD7528			—	—	—	—	—
Pin	Pin39	Pin128	Pin122	—	—	—	—	—

† /WR also connect RW on LCD

† /DACA connect RS on LCD

9.5 Evaluations

Please do the following evaluations according to the questions listed below:

- Do you know which Lab-Platform is introduced in this chapter?
- Do you know which CPLD chip is adopted in this Lab-Platform?
- Do you know the main functions of Lab-Platform? Do you know how to setup?
- Do you know how to check the arrangement of Pins?