ECE 153B: Lab 4 Turn-in Questions

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1.

BRR stands for baud-rate register, in which we set the USARTDIV value. This value divides the system clock frequency. In the case of oversampling by 16, the corresponding baud rate is given by

baud rate =
$$\frac{f_{\text{clk}}}{\text{USARTDIV}}$$

2.

In the lab handout, we are instructed to choose a prescaler value of 7 such that an I2C clock frequency $f_{\text{PRESC}} = 10 \,\text{MHz}$ is achieved. The corresponding I2C clock period $t_{\text{PRESC}} = 100 \,\text{ns}$ is used in the calculation of all delays shown in the timing diagrams for I2C transactions. These calculations must be rounded up to the nearest integer, since the specified delays are minimum values.

For example, $t_{\text{SCLDEL}} = (\text{SCLDEL} + 1) \cdot t_{\text{PRESC}}$, where $t_{\text{SCLDEL}} = 1 \,\mu\text{s}$ and $t_{\text{PRESC}} = 100 \,\text{ns}$. This gives SCLDEL = 9.

Similar calculations outlined in the lab handout result in SDADEL = 13, SCLH = 40, and SCLL = 47.

3.

After setting the relevant registers in the accelerometer to configure it appropriately, we read data from the accelerometer by sending it a read command. Such a command consists of a read/write bit (1 for a read operation), then a multi-byte bit (always zero; we only perform single-byte transactions), followed by the six-bit address we wish to read. We then send a dummy byte of all zeros. Throughout this two-byte transaction, we are clocking in data from the accelerometer as well.

We throw out the first byte that was clocked in, since it was received while we were still sending to the accelerometer the address we wish to read. The second byte contains the actual data we wish to read, and was clocked in while we were sending the dummy byte.