EE533 NETWORK PROCESSOR DESIGN & PROGRAMMING

LAB#2: Xilinx ISE 10.1 SCHEMATIC (32-BIT ALU)

Instructor: Prof. Young Cho, PhD

CREATED AND COMPILED BY:

SARTHAK JAIN

(MS EE, UNIVERSITY OF SOUTHERN CALIFORNIA)

GITHUB LINK FOR MY REPOSITORY:

You'll find all the codes and the executables on this repository.

https://github.com/SARTHAK-JAIN-ASIC/EE533/tree/main/LAB2

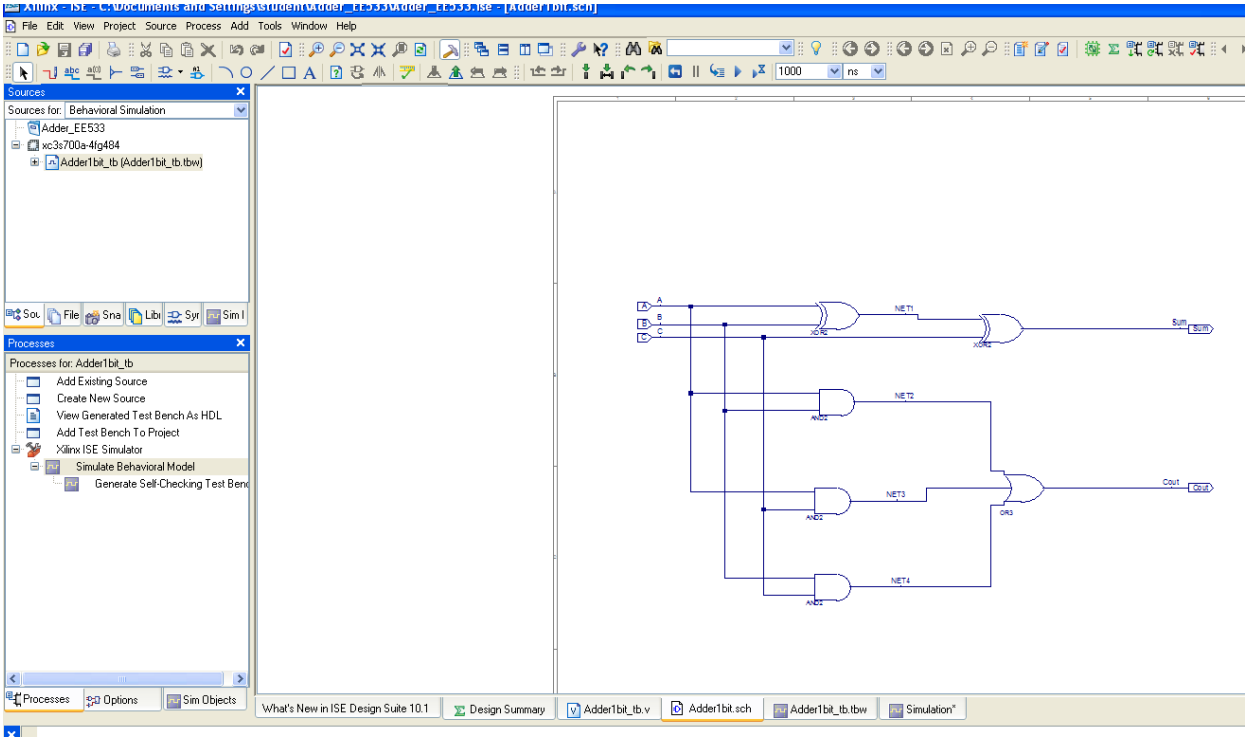
We first start with a one-bit adder

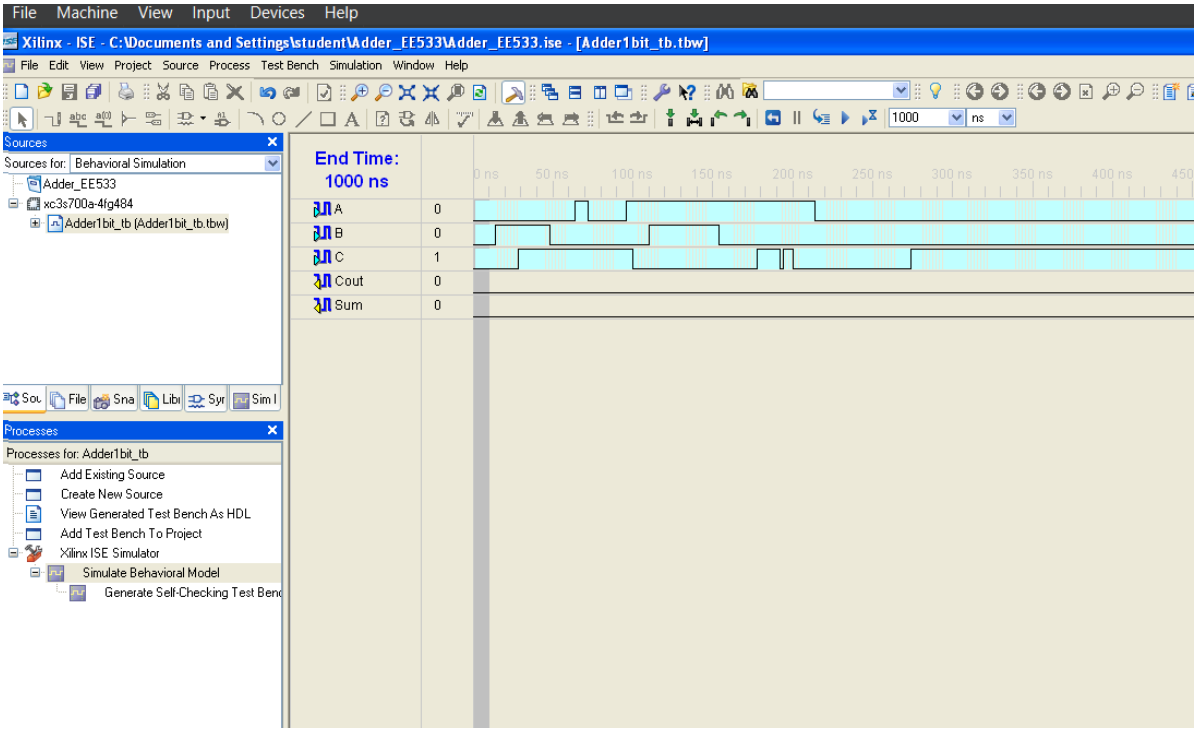
Shown for all subsequent circuits is:

1. Circuit
2. Testbench waveform
3. Actual simulation waveform

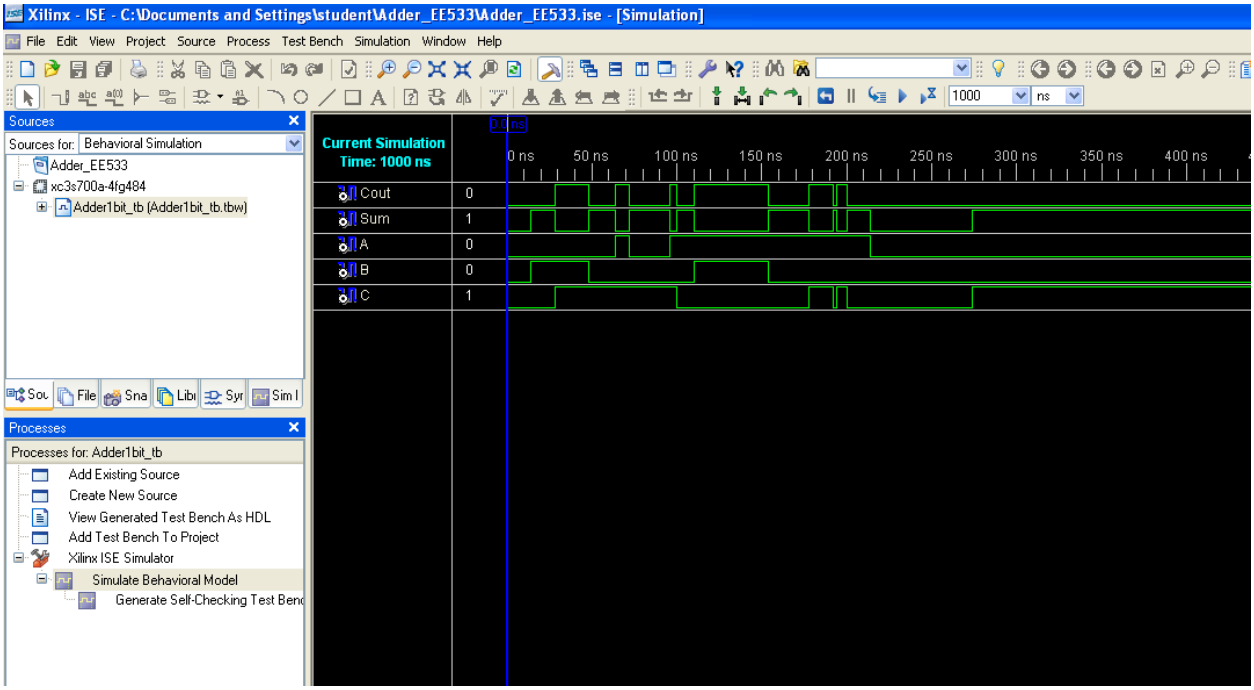
EE533 LAB2

1. ONE BIT ADDER

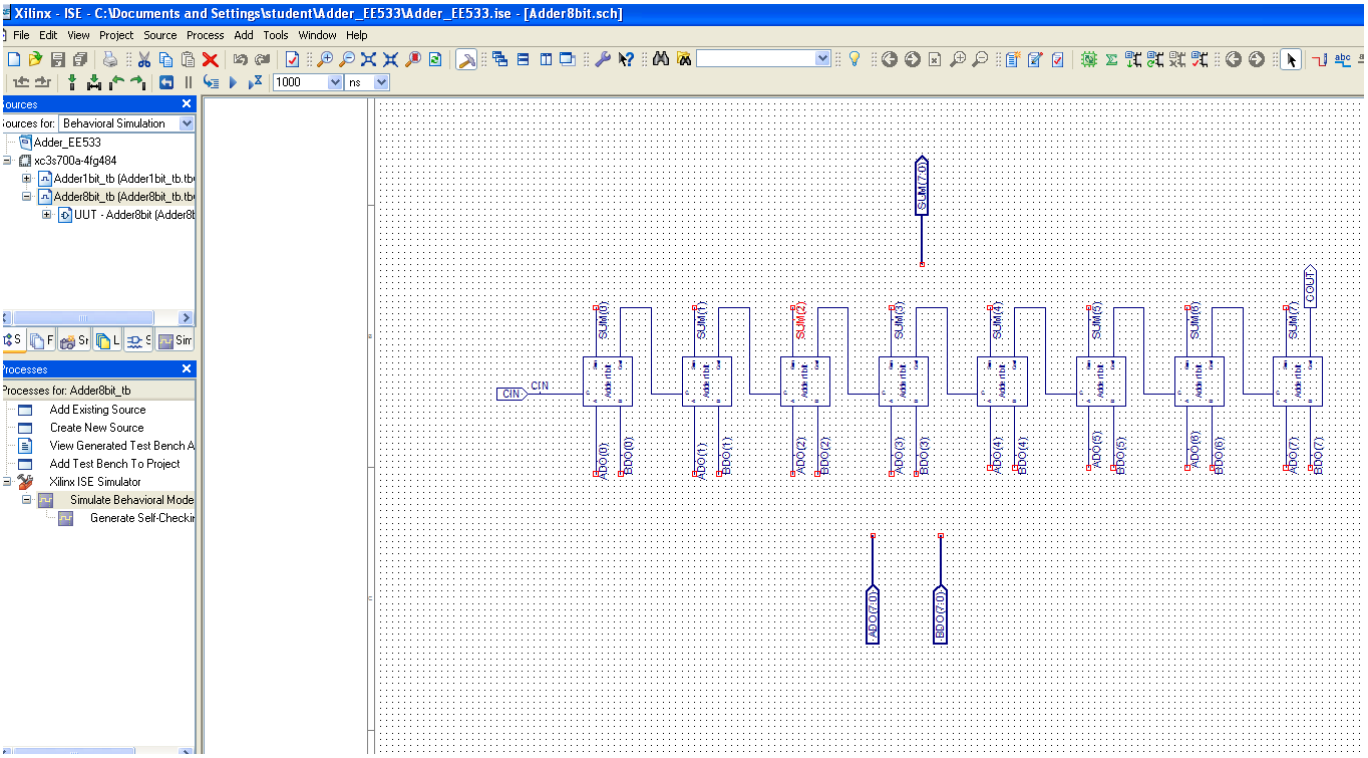


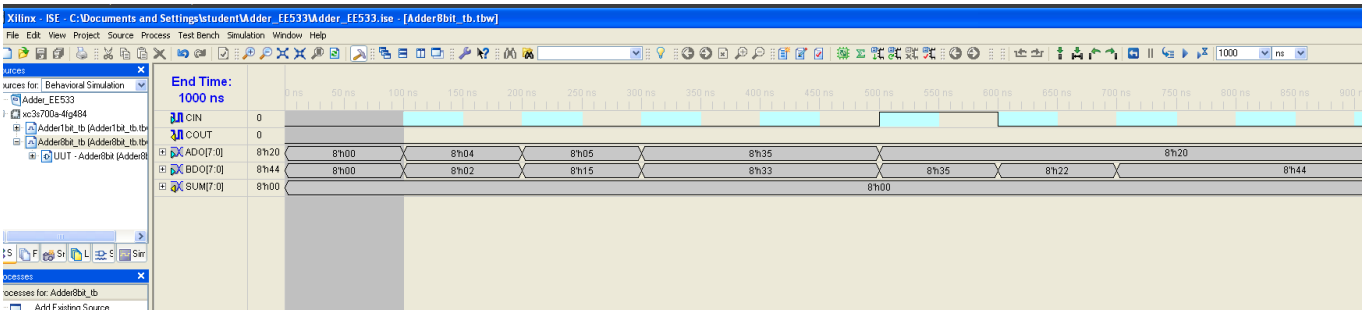


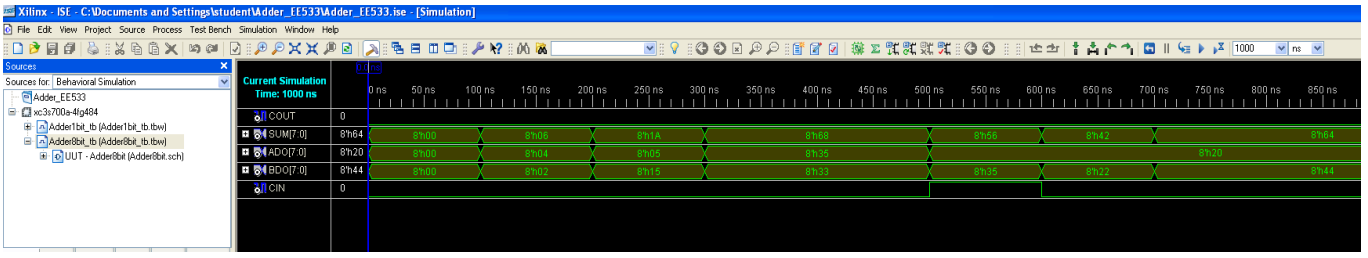
EE533 LAB2


Xilinx - ISE - C:\Documents and Settings\student\Adder_EE533\Adder_EE533.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources
Sources for: Behavioral Simulation
Adder_EE533
xc3s700a-4fg484
Adder1bit_tb (Adder1bit_tb.tbw)
Processes
Processes for: Adder1bit_tb
Add Existing Source
Create New Source
View Generated Test Bench As HDL
Add Test Bench To Project
Xilinx ISE Simulator
Simulate Behavioral Model
Current Simulation Time: 1000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
Cout
Sum
A
B
C
1000
ns

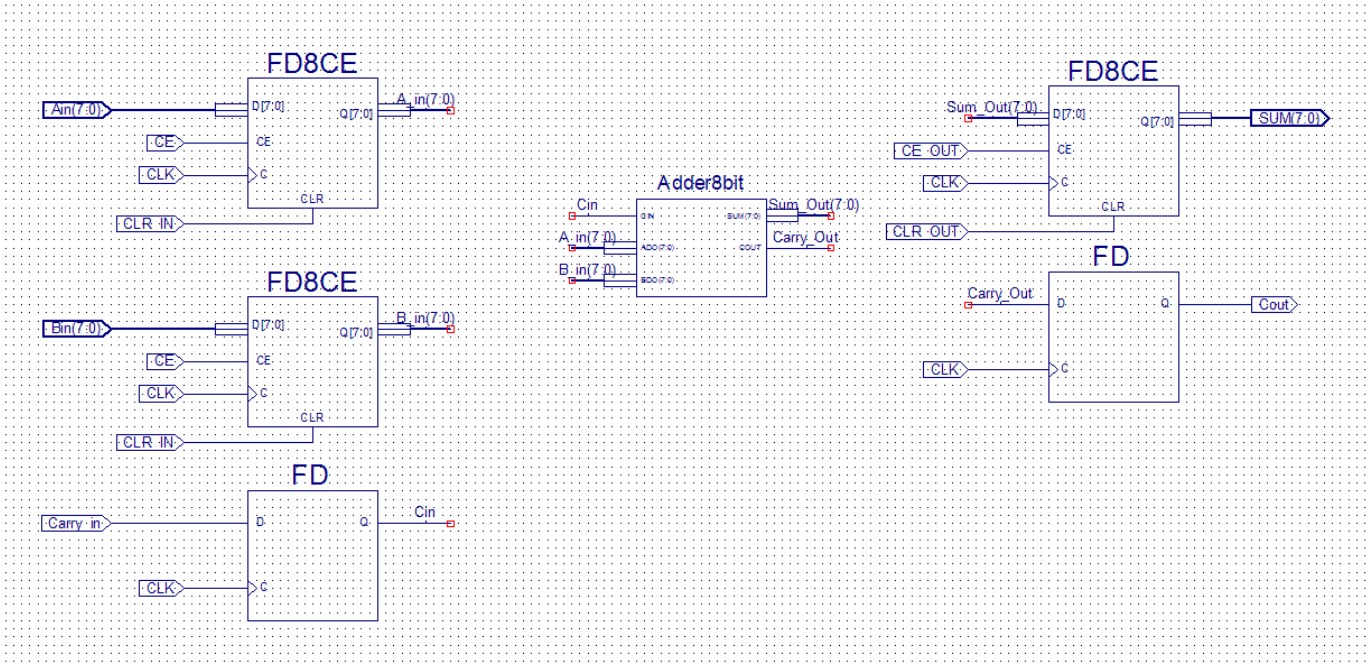
2. I then turned this adder into a SYMBOL and utilized it to make an 8-bit combinational adder

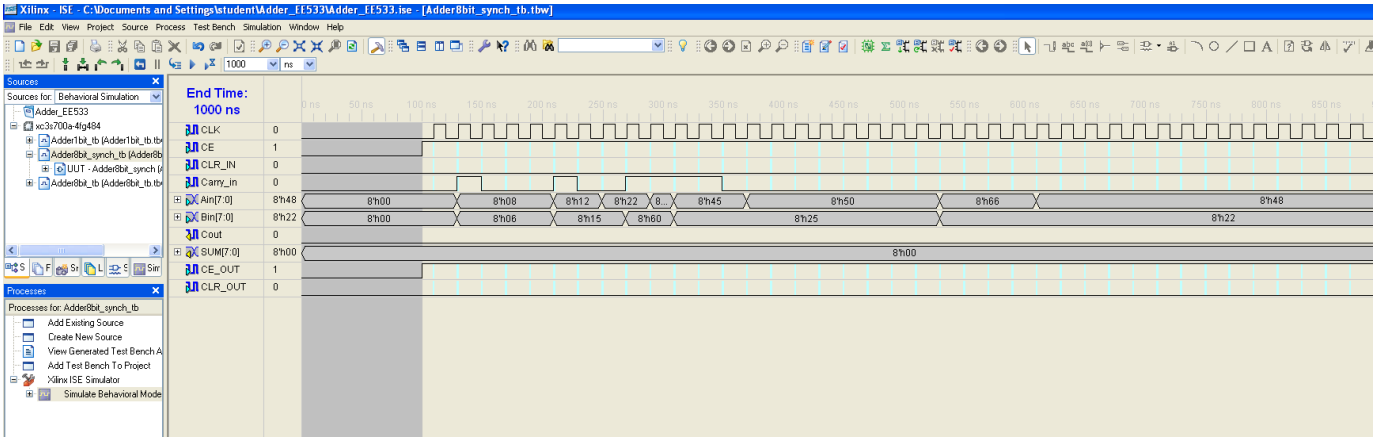


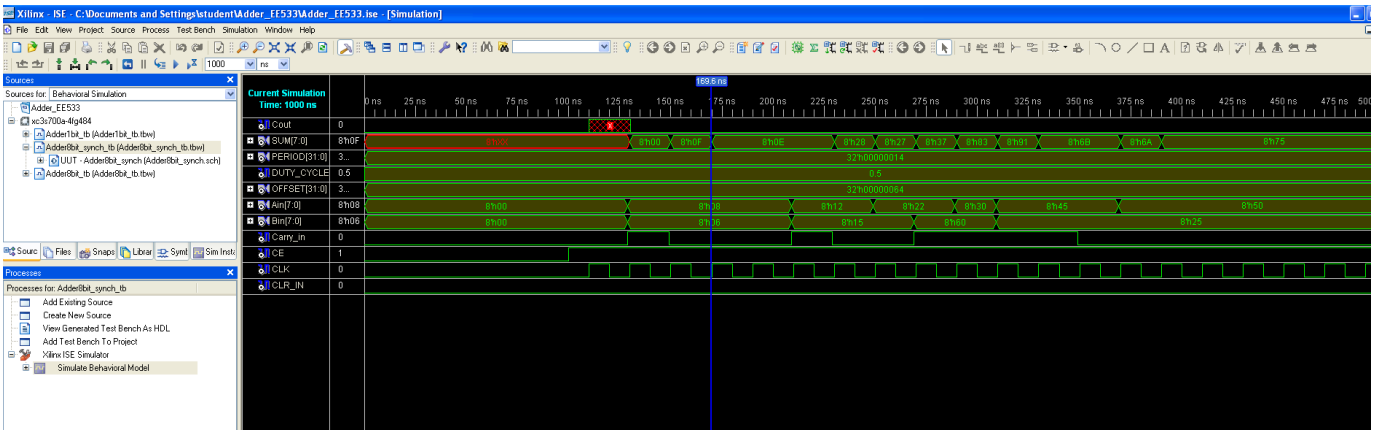




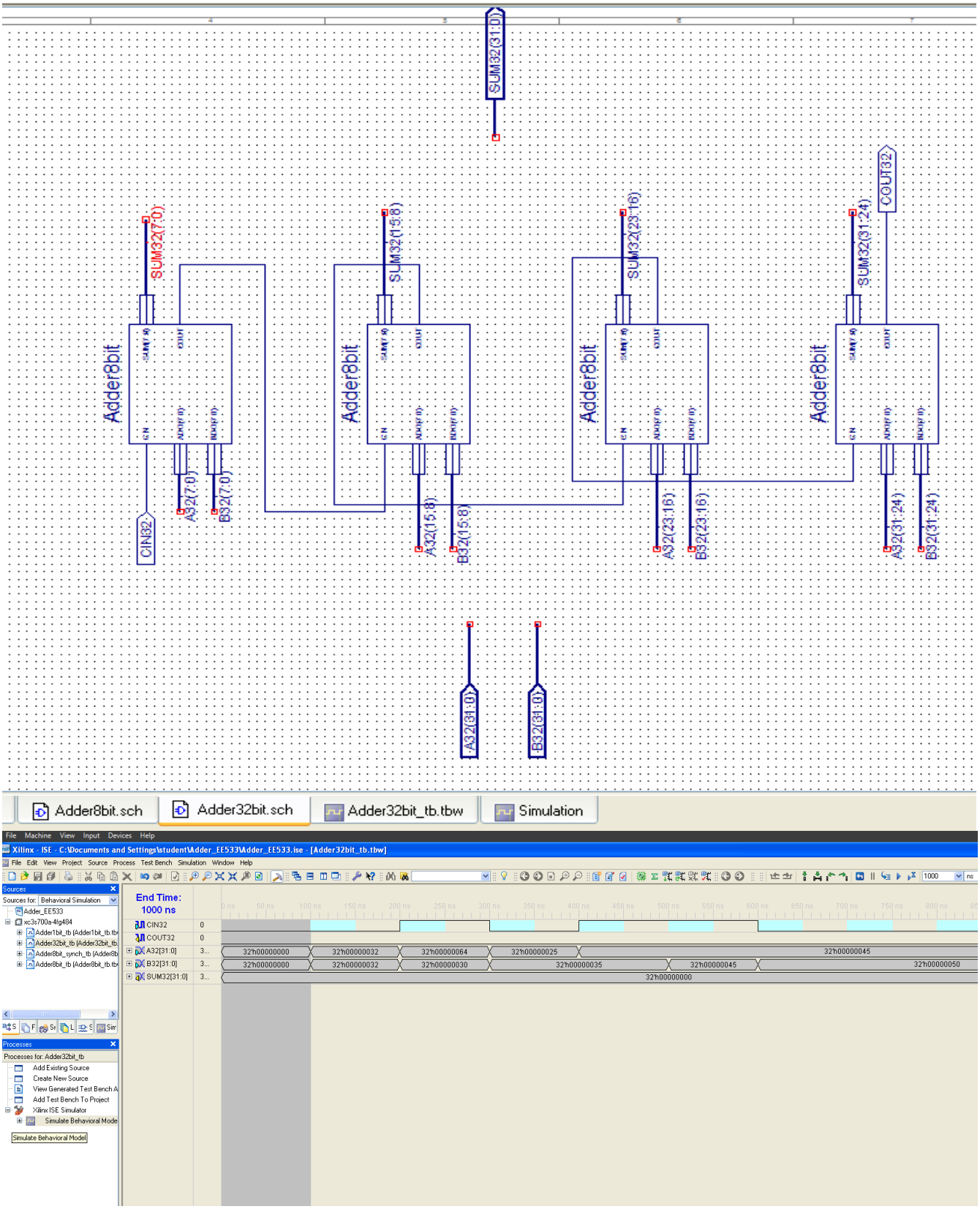
3. Finally, I made use of 8 bit FFs to turn my combinational adder into a synchronous one



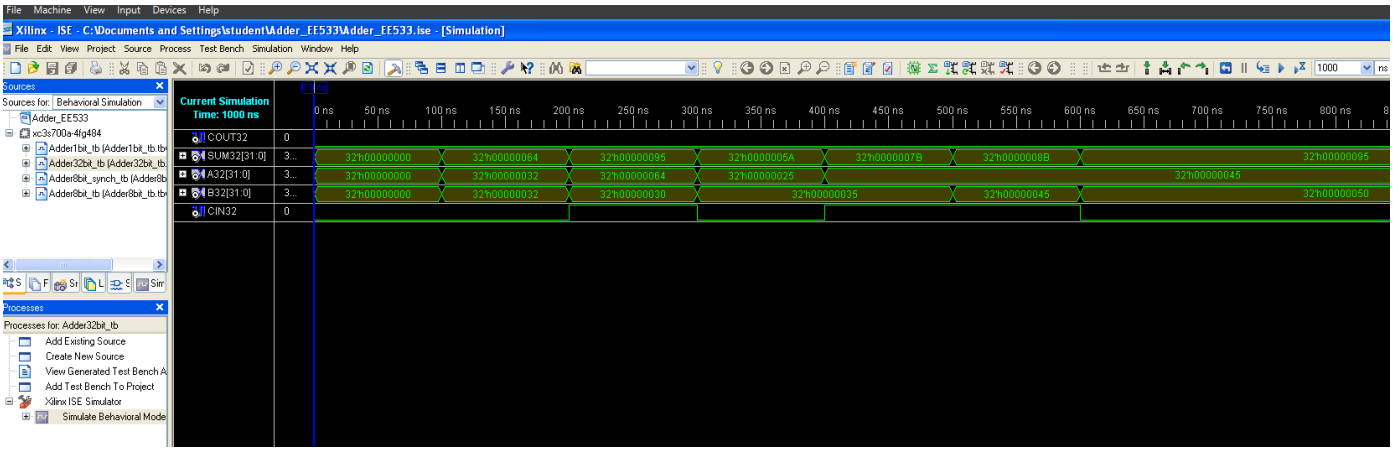




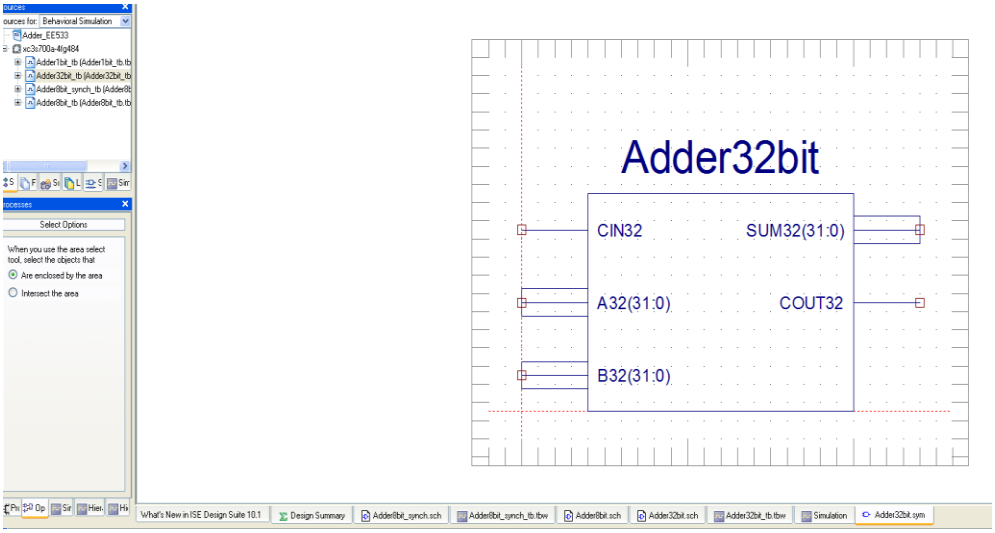
4. Next was to turn my 8-bit adder into a 32-bit one. As follows:



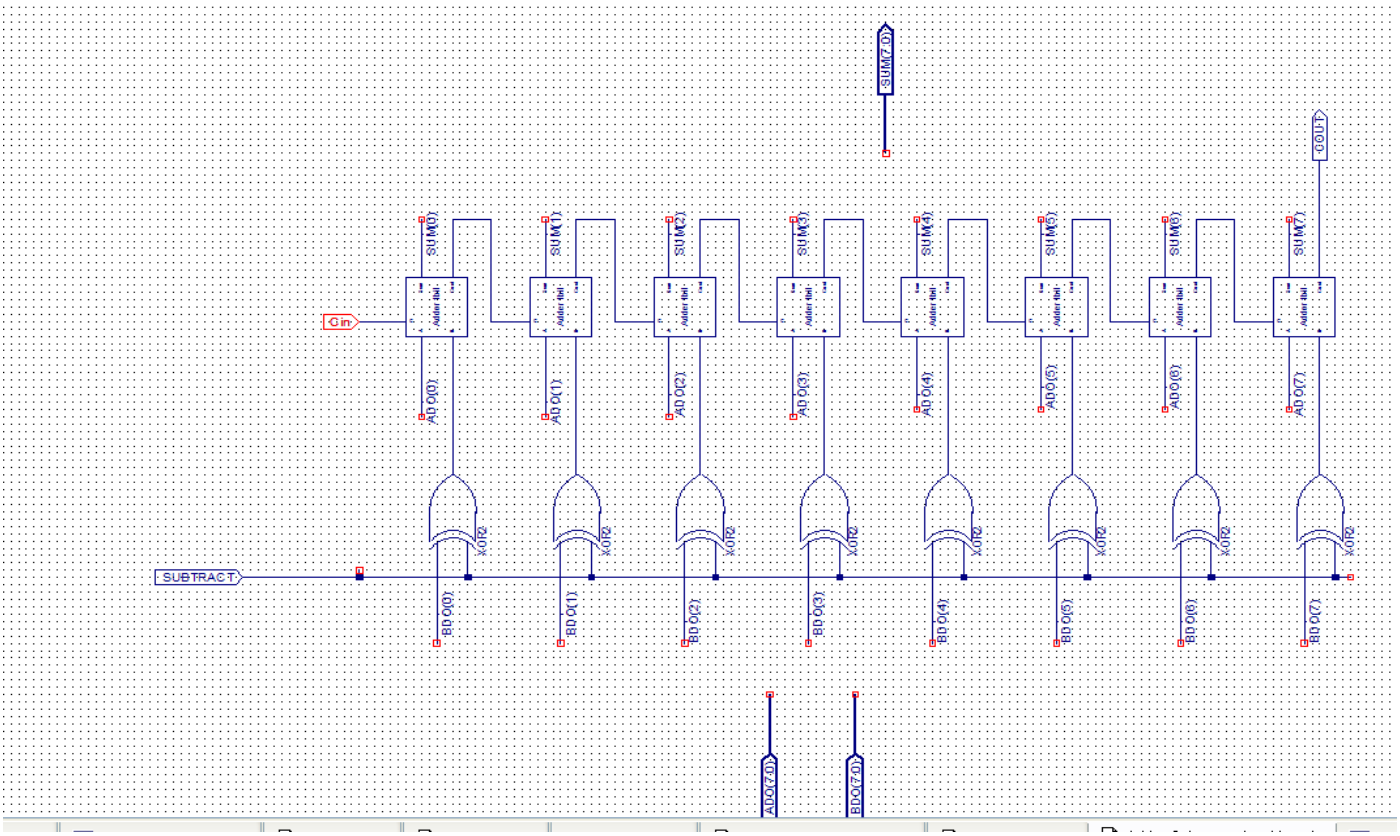
EE533 LAB2

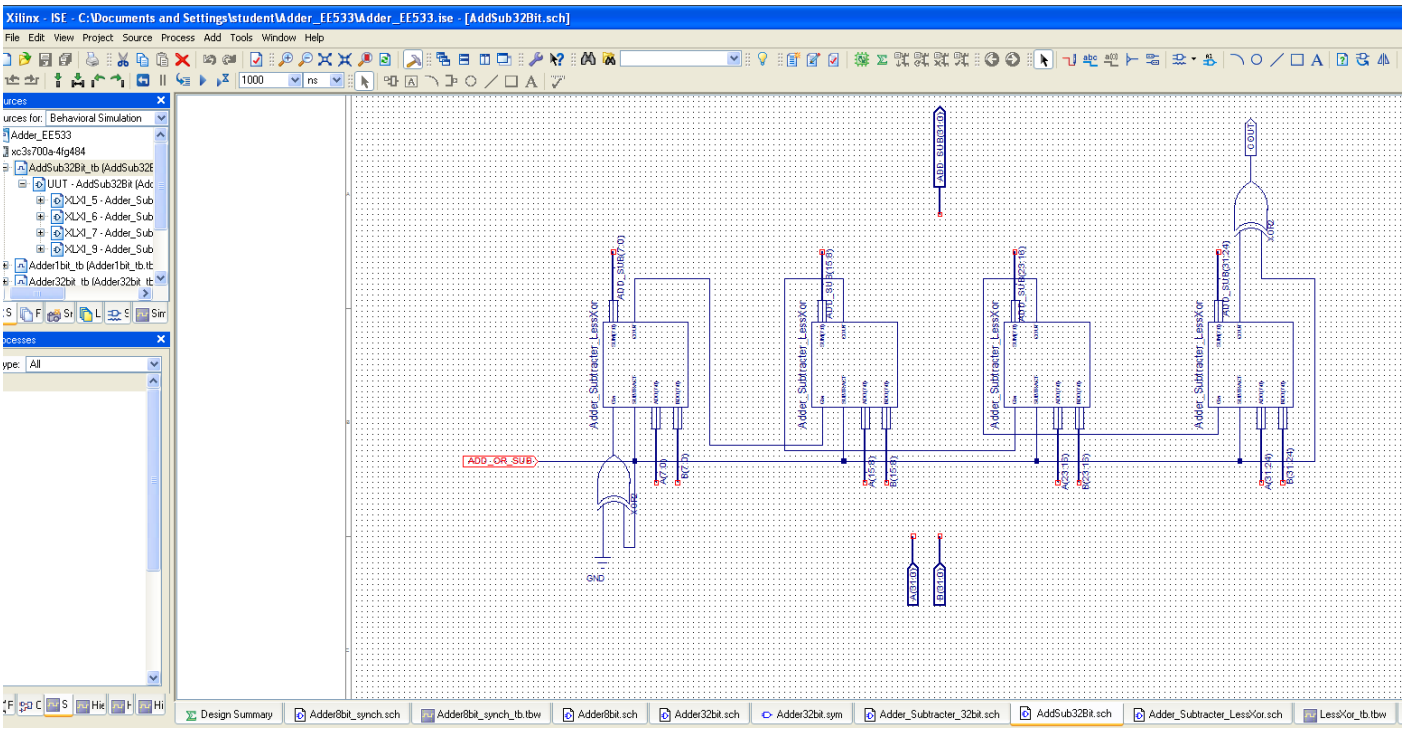


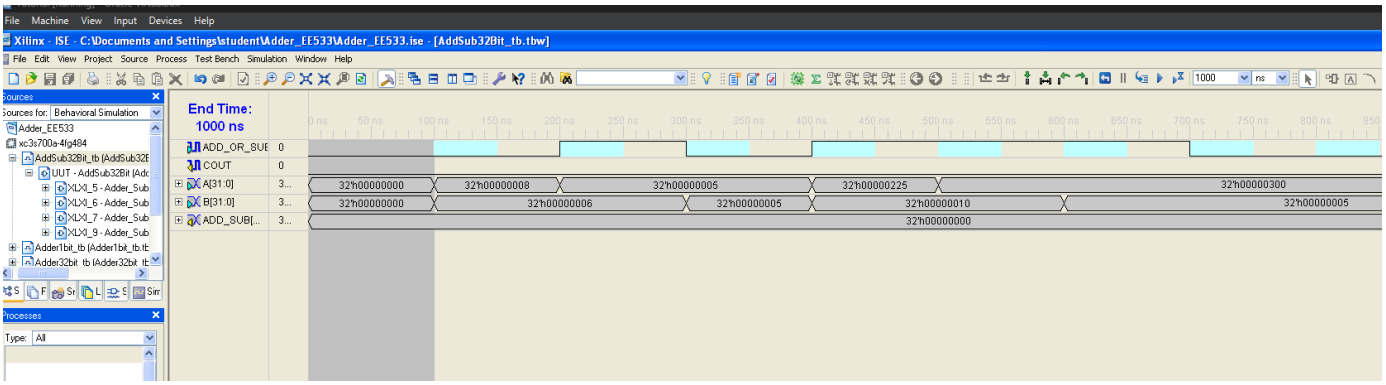
SYMBOL FOR THE SAME:

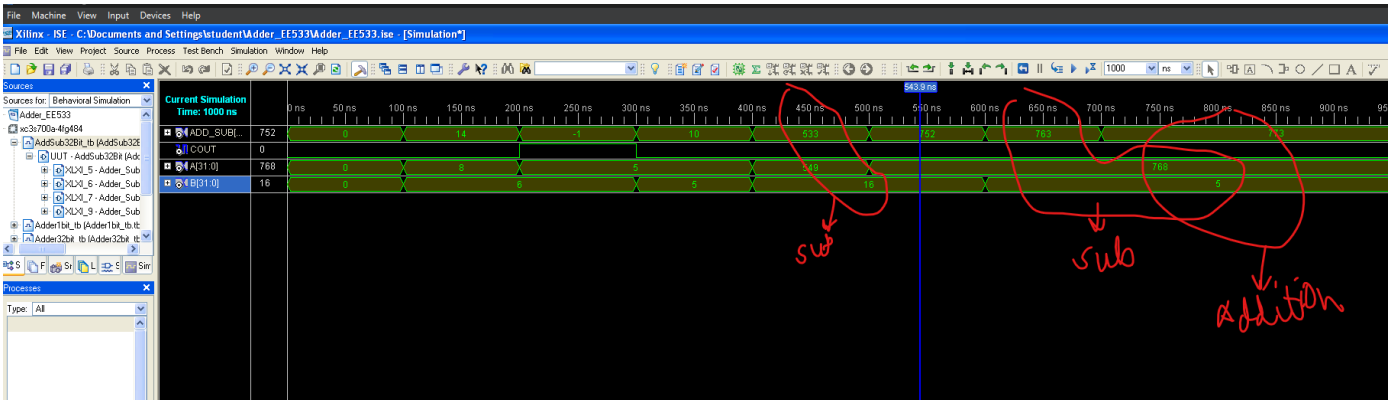


5. Next I wanted to create a **32-bit adder/subtractor** out of the adder that I already had. For that, I just had to utilize a few xor gates (made a symbol out of the intermediate stage) and gave the user an option to decide if the subtractor was required or the adder.

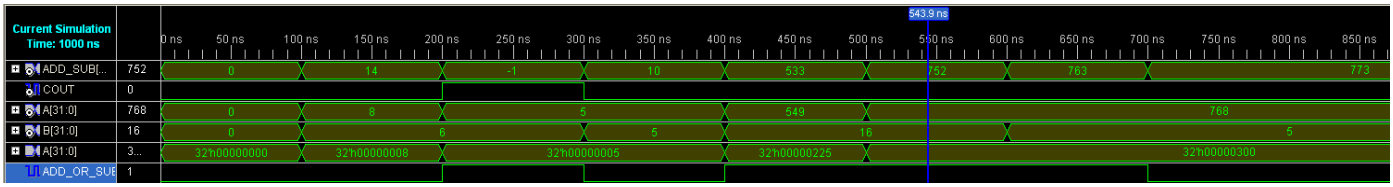


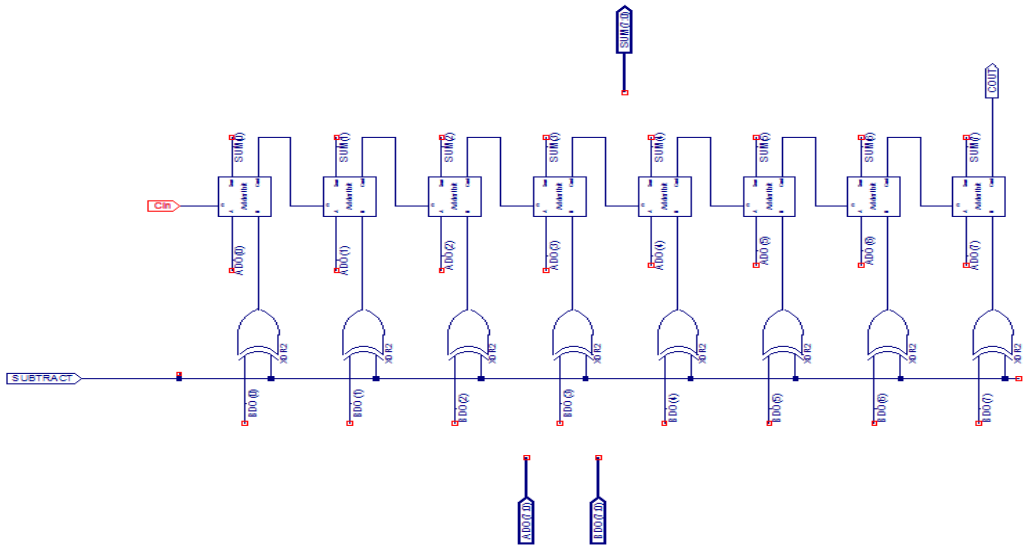






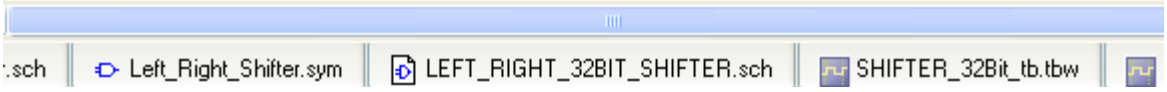
The waveform at the bottom shows the “subtract” signal, toggling addition and subtraction

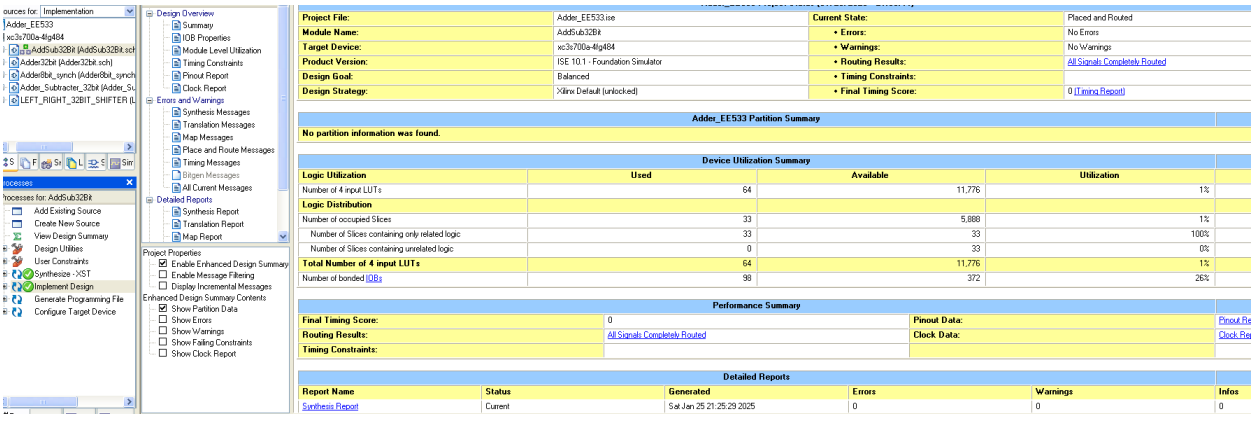




EE533 LAB2

```
================================================================================
*                            Final Report
================================================================================
Final Results
RTL Top Level Output File Name     : AddSub32Bit.ngr
Top Level Output File Name         : AddSub32Bit
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : NO

Design Statistics
# IOs                              : 98

Cell Usage :
# BELS                             : 227
#       AND2                       : 96
#       GND                        : 1
#       OR3                        : 32
#       XOR2                       : 98
# IO Buffers                       : 98
#       IBUF                       : 65
#       OBUF                       : 33
================================================================================

Device utilization summary:
---------------------------

Selected Device : 3s700afg484-4

 Number of Slices:                        0  out of    5888      0%
 Number of IOs:                          98
 Number of bonded IOBs:                  98  out of     372     26%
```





Project File:	Adder_EE533.ise	**Current State:**	Placed and Routed
Module Name:	AddSub32Bit	**• Errors:**	No Errors
Target Device:	xc3s700a-4fg484	**• Warnings:**	No Warnings
Product Version:	ISE 10.1 - Foundation Simulator	**• Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	**• Timing Constraints:**	
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	0 (Timing Report)

Adder_EE533 Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	64	11,776	1%
Logic Distribution			
Number of occupied Slices	33	5,888	1%
Number of Slices containing only related logic	33	33	100%
Number of Slices containing unrelated logic	0	33	0%
Total Number of 4 input LUTs	64	11,776	1%
Number of bonded IOBs	98	372	26%

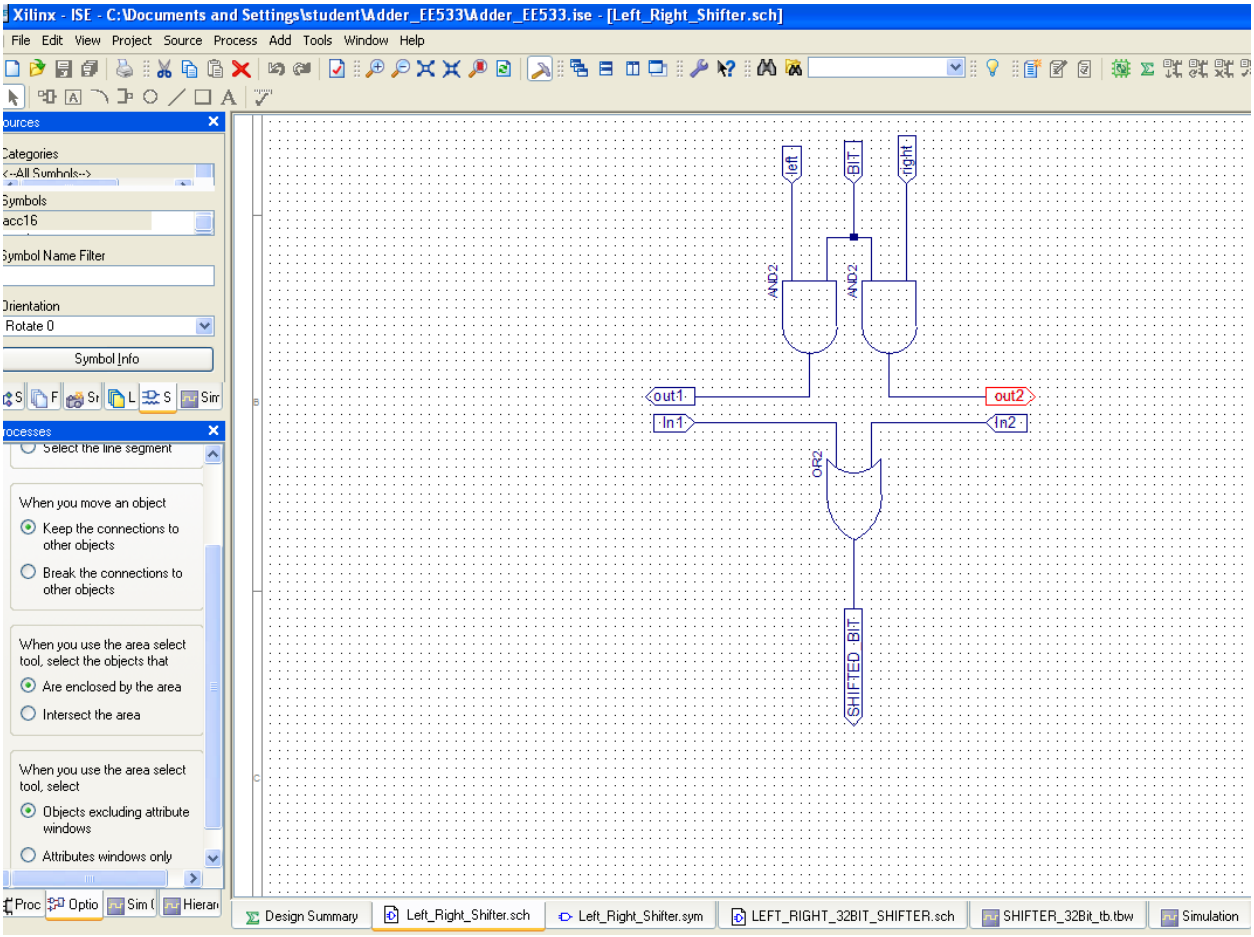
Performance Summary

Final Timing Score:	0	**Pinout Data:**	Pinout Re
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Re
Timing Constraints:			

Detailed Reports

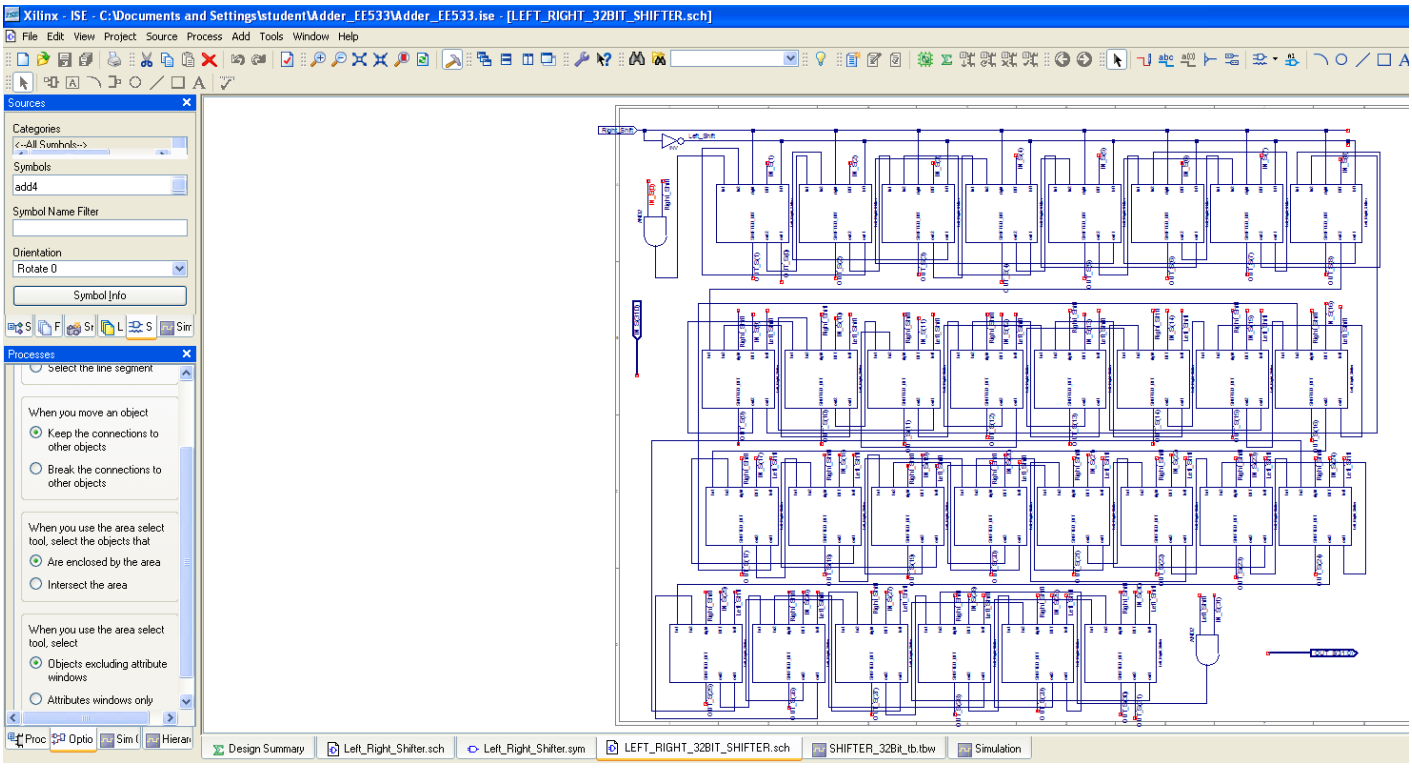
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Jan 25 21:25:29 2025	0	0	0

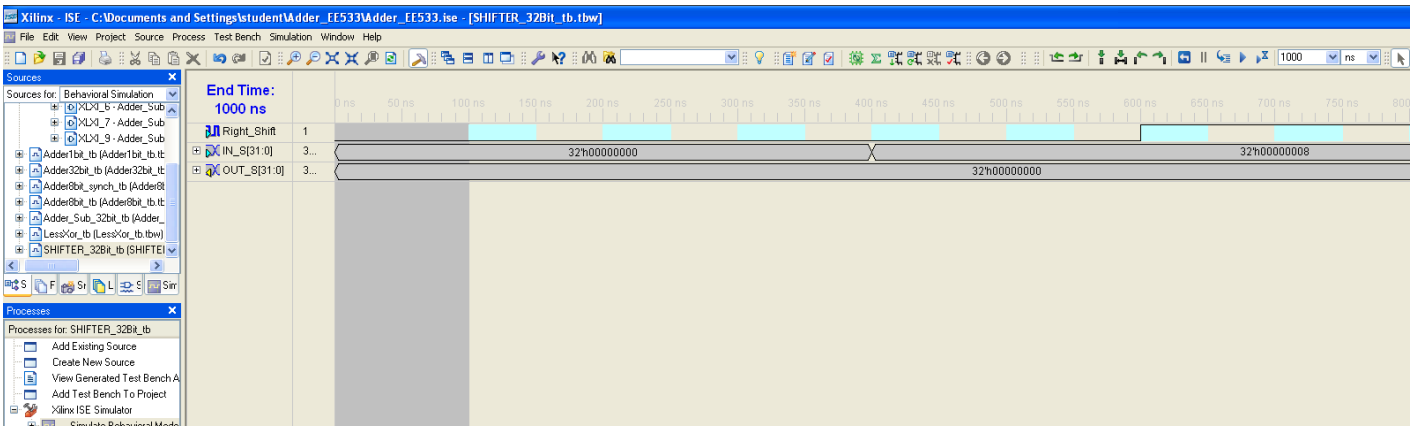
6. Next, it was time to make a shifter. For this, I gave a LINE/INPUT to decide if the user wanted to shift the number left or shift it right. First

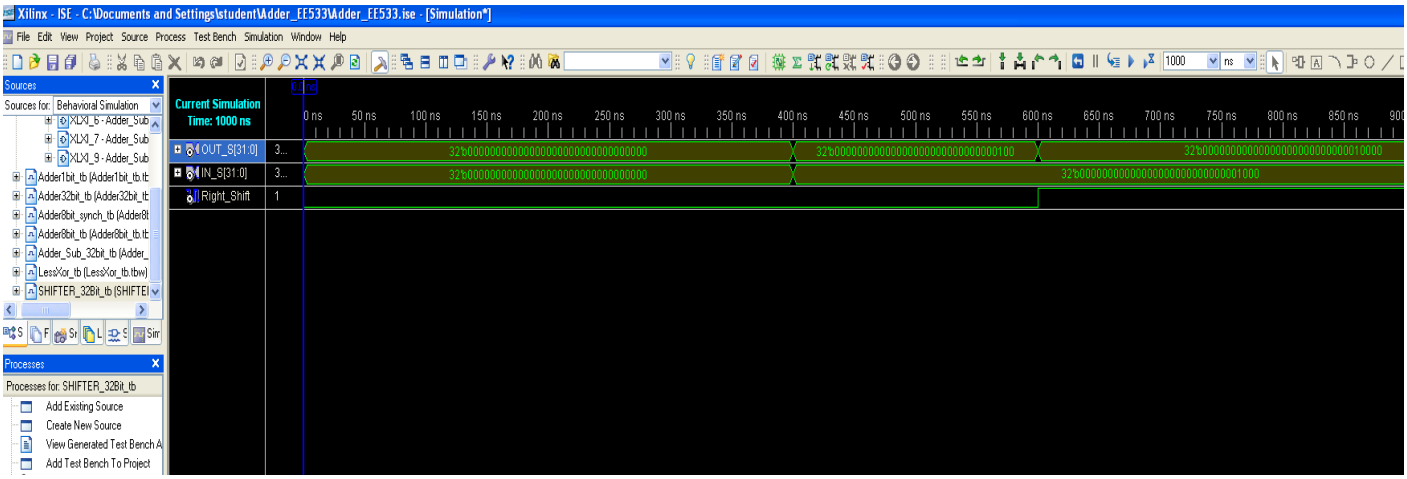


This was a very basic unit I used to make my shifter. Created a SYMBOL out of it and utilized that to create a 32-bit shifter.

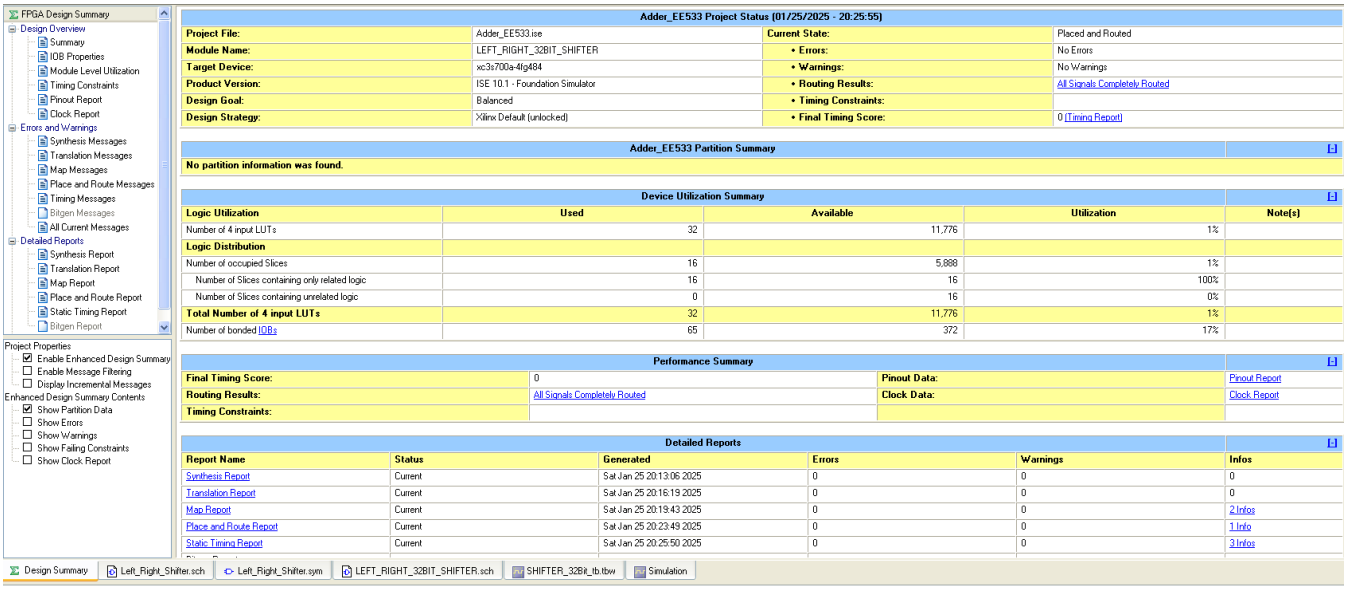
EE533 LAB2


Xilinx - ISE - C:\Documents and Settings\student\Adder_EE533\Adder_EE533.ise - [LEFT_RIGHT_32BIT_SHIFTER.sch]
File Edit View Project Source Process Add Tools Window Help
Sources
Categories
Symbols
add4
Symbol Name Filter
Orientation
Rotate 0
Symbol Info
Processes
When you move an object
Keep the connections to other objects
Break the connections to other objects
When you use the area select tool, select the objects that
Are enclosed by the area
Intersect the area
When you use the area select tool, select
Objects excluding attribute windows
Attributes windows only
Design Summary
Left_Right_Shifter.sch
Left_Right_Shifter.sym
LEFT_RIGHT_32BIT_SHIFTER.sch
SHIFTER_32Bit_tb.tbw
Simulation


Xilinx - ISE - C:\Documents and Settings\student\Adder_EE533\Adder_EE533.ise - [SHIFTER_32Bit_tb.tbw]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources
Sources for: Behavioral Simulation
Processes
Processes for: SHIFTER_32Bit_tb
Add Existing Source
Create New Source
View Generated Test Bench A
Add Test Bench To Project
Xilinx ISE Simulator
End Time:
1000 ns
Right_Shift
IN_S[31:0]
OUT_S[31:0]
32'h00000000
32'h00000008
32'h00000000


Xilinx - ISE - C:\Documents and Settings\student\Adder_EE533\Adder_EE533.ise - [Simulation*]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources
Sources for: Behavioral Simulation
Processes
Processes for: SHIFTER_32Bit_tb
Add Existing Source
Create New Source
View Generated Test Bench A
Add Test Bench To Project
Current Simulation Time: 1000 ns
OUT_S[31:0]
IN_S[31:0]
Right_Shift

The following shows the mapped implementation and the overall LUT and cell usage



FPGA Design Summary

- Design Overview
  - Summary
  - IOB Properties
  - Module Level Utilization
  - Timing Constraints
  - Pinout Report
  - Clock Report
- Errors and Warnings
  - Synthesis Messages
  - Translation Messages
  - Map Messages
  - Place and Route Messages
  - Timing Messages
  - Bitgen Messages
  - All Current Messages
- Detailed Reports
  - Synthesis Report
  - Translation Report
  - Map Report
  - Place and Route Report
  - Static Timing Report
  - Bitgen Report

Project Properties

- [x] Enable Enhanced Design Summary
- [ ] Enable Message Filtering
- [ ] Display Incremental Messages

Enhanced Design Summary Contents

- [x] Show Partition Data
- [ ] Show Errors
- [ ] Show Warnings
- [ ] Show Failing Constraints
- [ ] Show Clock Report

Adder_EE533 Project Status (01/25/2025 - 20:25:55)

Project File:	Adder_EE533.ise	**Current State:**	Placed and Routed
Module Name:	LEFT_RIGHT_32BIT_SHIFTER	**• Errors:**	No Errors
Target Device:	xc3s700a-4fg484	**• Warnings:**	No Warnings
Product Version:	ISE 10.1 - Foundation Simulator	**• Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	**• Timing Constraints:**	
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	0 (Timing Report)

Adder_EE533 Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	32	11,776	1%	
Logic Distribution				
Number of occupied Slices	16	5,888	1%	
Number of Slices containing only related logic	16	16	100%	
Number of Slices containing unrelated logic	0	16	0%	
Total Number of 4 input LUTs	32	11,776	1%	
Number of bonded IOBs	65	372	17%	

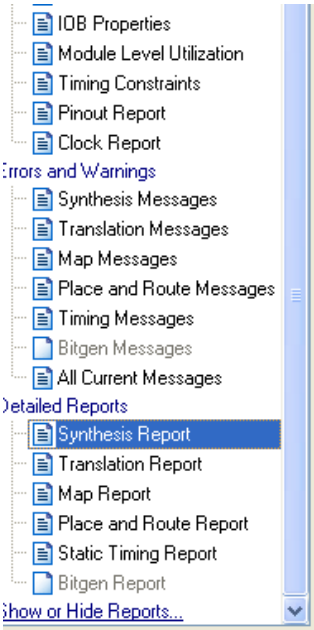
Performance Summary

Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:			

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Jan 25 20:13:06 2025	0	0	0
Translation Report	Current	Sat Jan 25 20:16:19 2025	0	0	0
Map Report	Current	Sat Jan 25 20:19:43 2025	0	0	2 Infos
Place and Route Report	Current	Sat Jan 25 20:23:49 2025	0	0	1 Info
Static Timing Report	Current	Sat Jan 25 20:25:50 2025	0	0	3 Infos

Design Summary | Left_Right_Shifter.sch | Left_Right_Shifter.sym | LEFT_RIGHT_32BIT_SHIFTER.sch | SHIFTER_32Bit_tb.tbw | Simulation



- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report

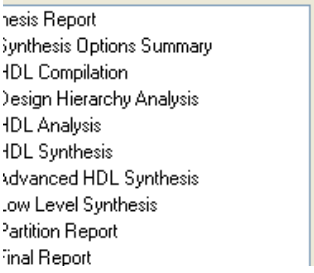
Errors and Warnings

- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Current Messages

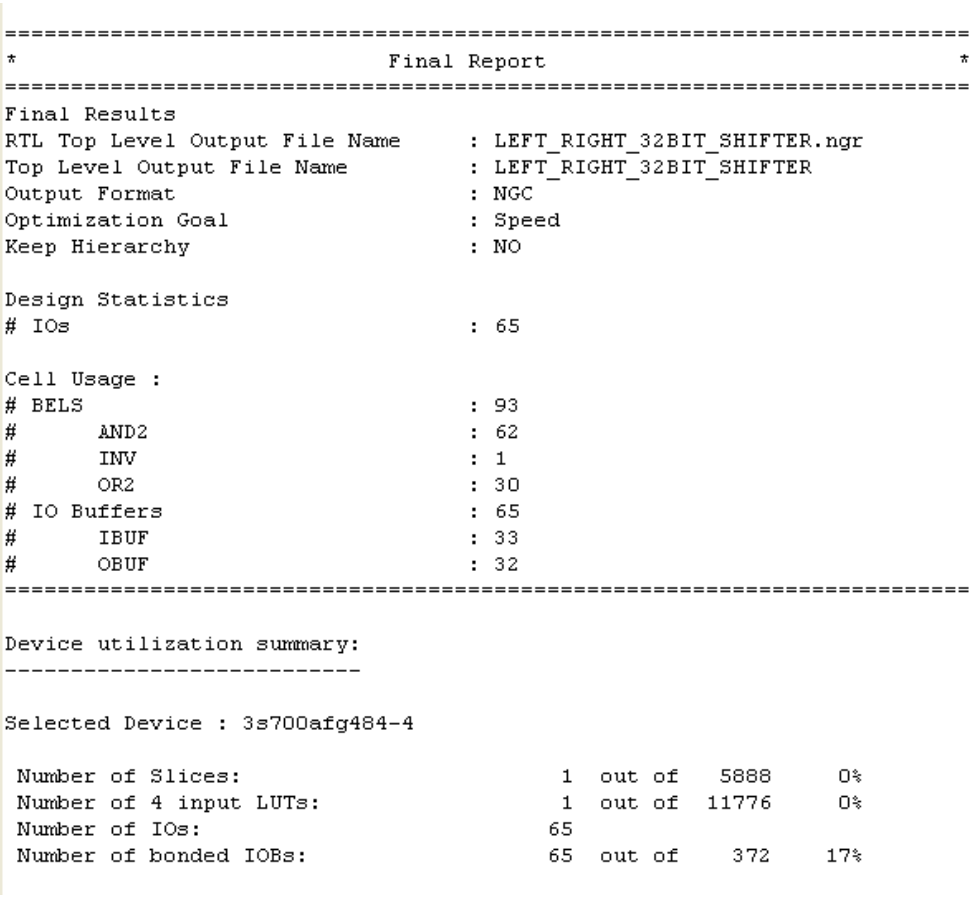
Detailed Reports

- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Static Timing Report
- Bitgen Report

Show or Hide Reports...

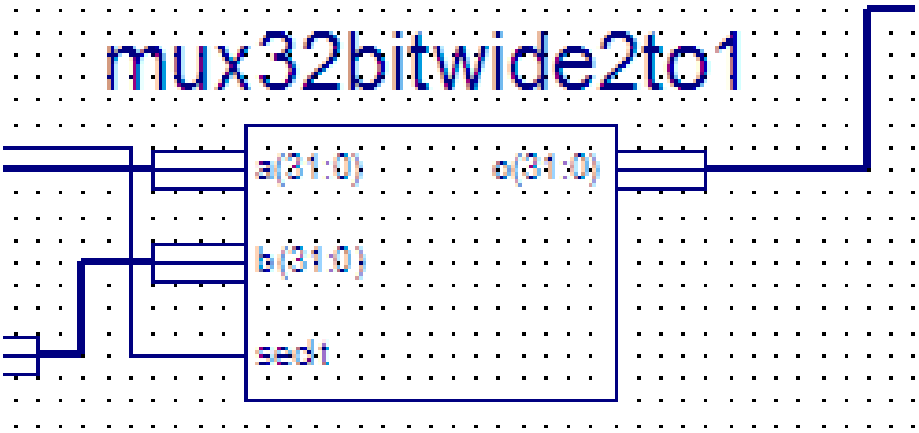


- nesis Report
- Synthesis Options Summary
- HDL Compilation
- Design Hierarchy Analysis
- HDL Analysis
- HDL Synthesis
- Advanced HDL Synthesis
- Low Level Synthesis
- Partition Report
- Final Report



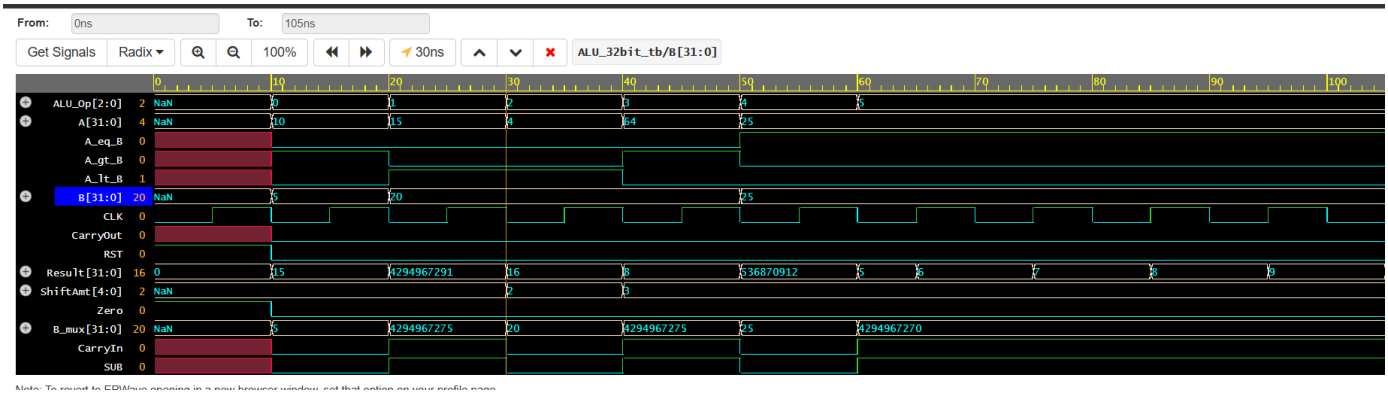
```
================================================================================
*                           Final Report                                       *
================================================================================
Final Results
RTL Top Level Output File Name     : LEFT_RIGHT_32BIT_SHIFTER.ngr
Top Level Output File Name         : LEFT_RIGHT_32BIT_SHIFTER
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : NO

Design Statistics
# IOs                              : 65

Cell Usage :
# BELS                             : 93
#      AND2                        : 62
#      INV                         : 1
#      OR2                         : 30
# IO Buffers                       : 65
#      IBUF                        : 33
#      OBUF                        : 32
================================================================================

Device utilization summary:
---------------------------

Selected Device : 3s700afg484-4

 Number of Slices:                        1  out of   5888     0%
 Number of 4 input LUTs:                  1  out of  11776     0%
 Number of IOs:                          65
 Number of bonded IOBs:                  65  out of    372    17%
```

MUX FOR THE ALU (starting with 32-bit 2x1)



VERILOG CODE IMPLEMENTATIONS:

The following is the waveform I got for the ALU when I wrote the Verilog code for the modules I implemented




```
Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of 4 input LUTs:                98 out of  11,776    1%
Logic Distribution:
  Number of occupied Slices:             49 out of   5,888    1%
    Number of Slices containing only related logic:      49 out of      49 100%
    Number of Slices containing unrelated logic:          0 out of      49   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:          98 out of  11,776    1%
  Number of bonded IOBs:                101 out of     372   27%

Peak Memory Usage:  158 MB
Total REAL time to MAP completion:  6 secs
Total CPU time to MAP completion:   5 secs
```

We realize from this that the number of gates in the schematic version is lower compared to the actual synthesis from the verilog code we created (as here, it the tool that decides what to ‘optimize’.

EE533 LAB2