TIMER TUTORIAL

Introduction:

1. We are using Timer to Generate the exact delay as required by the application.
2. As Timer works as an independent Hardware meanwhile CPU can take up the other process in multitasking Environment.
3. Operating Frequency of the Timers is Configurable in the STM32 microcontroller.
4. There are 14 Timers.
   *Twelve 16bit Timers including 2 PWM Timers, others are General Purpose Timers
   *Two 32 Bit General Purpose Timers.

Pre-scalar has to calculate to get the required frequency of the Timer clock

Calculation:

- Period of the timer clock is configured as 1 millisecond, which is useful to generate the delay in milliseconds, and seconds easily.
- If the required frequency is 1Khz.
- Pre-scalar= System Clock Frequency/Required Timer Clock frequency
  =16MHz/1KHz
  =16000

  i.e Timer clock will take 1mSec per tick.

- For 1tick(1count) =1ms
- 1000counts=1second
- Pre-scalar Register also assigned with Pre-scalar value
- Number of counts is assigned to Auto Reload Register (ARR) of the Timer

*ARR will load the value to counter (CNT register) automatically on every overflow.

*Counter will count for 1000 times as soon as Control Register enabled

Program steps to generate the Delay for LED Blinking

1. Add Header File named STM32F4xx.h to ‘inc’ folder of the project since it’s a CMSIS method of programming.
2. Enable GPIOA using AHB1ENR

   Set the LED pin as OUTPUT:
3. Configure the Moder 5(10 & 11) bit using GPIOA_MODER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODER15[1:0]		MODER14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODER9[1:0]		MODER8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODER7[1:0]		MODER6[1:0]		MODER5[1:0]		MODER4[1:0]		MODER3[1:0]		MODER2[1:0]		MODER1[1:0]		MODER0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 2y:2y+1 **MODERy[1:0]:** Port x configuration bits (y = 0..15)
These bits are written by software to configure the I/O direction mode.
00: Input (reset state)
01: General purpose output mode
10: Alternate function mode
11: Analog mode

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4. Set the bit 5 of GPIOAODR register to turn on the LED

7.4.6 GPIO port output data register (GPIOx_ODR) (x = A..H)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **ODRy**: Port output data (y = 0..15)
These bits can be read and written by software.
Note: For atomic bit set/reset, the ODR bits can be individually set and reset by writing to the GPIOx_BSRR register (x = A..H).

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Timer2 Configuration to generate the delay:

5. Enable TIMER2 using APB1ENR register

   Totally 5 Timer Registers are responsible to generate the delay

1. Pre-scalar Value given Pre-scalar Register
2. Number of counts given to ARR(Auto Reload Register) as counts-1, since it overflows the count as 0, this load to Counter Register automatically
3. Set the CEN(0) bit of Control Register to start the timer

17.4.1 TIMx control register 1 (TIMx_CR1)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	CKD[1:0]		ARPE	CMS		DIR	OPM	URS	UDIS	CEN
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:10 Reserved, must be kept at reset value.

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Bit 0 CEN: Counter enable

0: Counter disabled

1: Counter enabled

Note: External clock, gated mode and encoder mode can work only if the CEN bit has been

previously set by software. However trigger mode can set the CEN bit automatically by

hardware.

CEN is cleared automatically in one-pulse mode, when an update event occurs.

00: peripheral-to-memory

01: memory-to-peripheral

10: memory-to-memory

11: reserved

6. Check the status of UIF(0)bit of Status Register

17.4.5 TIMx status register (TIMx_SR)

Address offset: 0x10

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	CC4OF	CC3OF	CC2OF	CC1OF	Res.	Res.	TIF	Res.	CC4IF	CC3IF	CC2IF	CC1IF	UIF
			rc_w0	rc_w0	rc_w0	rc_w0			rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bits 15:13 Reserved, must be kept at reset value.

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7. If UIF bit is updated to 1(Over flow of the count), i.e delay has generated.
8. Clear the bit 5 of GPIOAODR register to turn off the LED
9. Call the Delay Function again