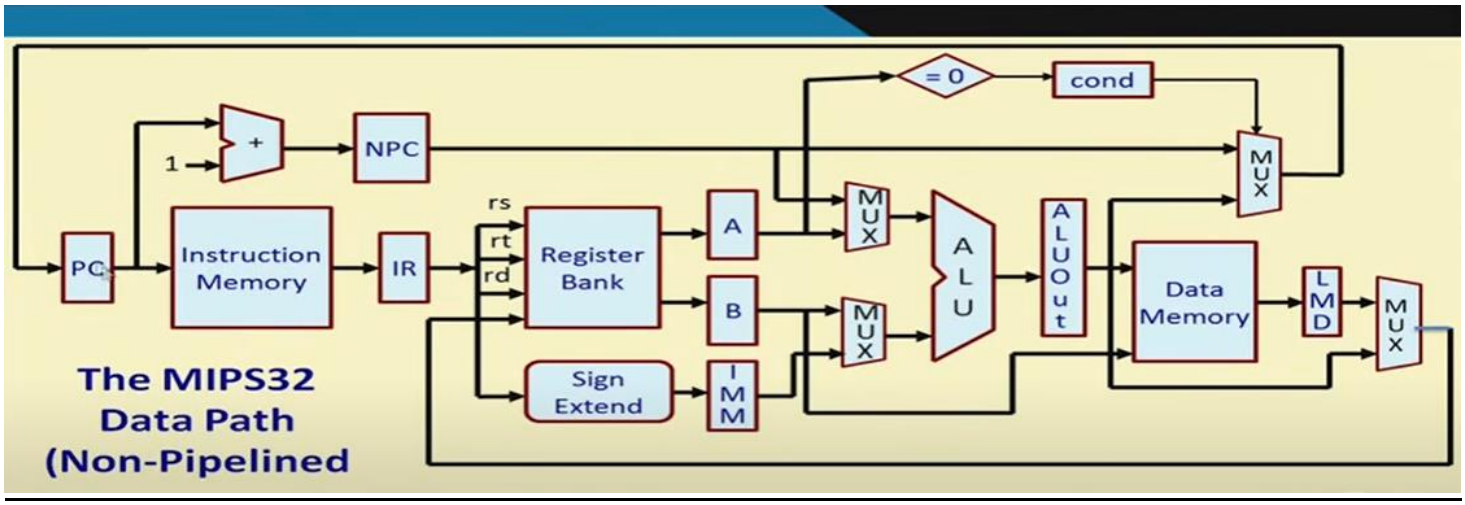
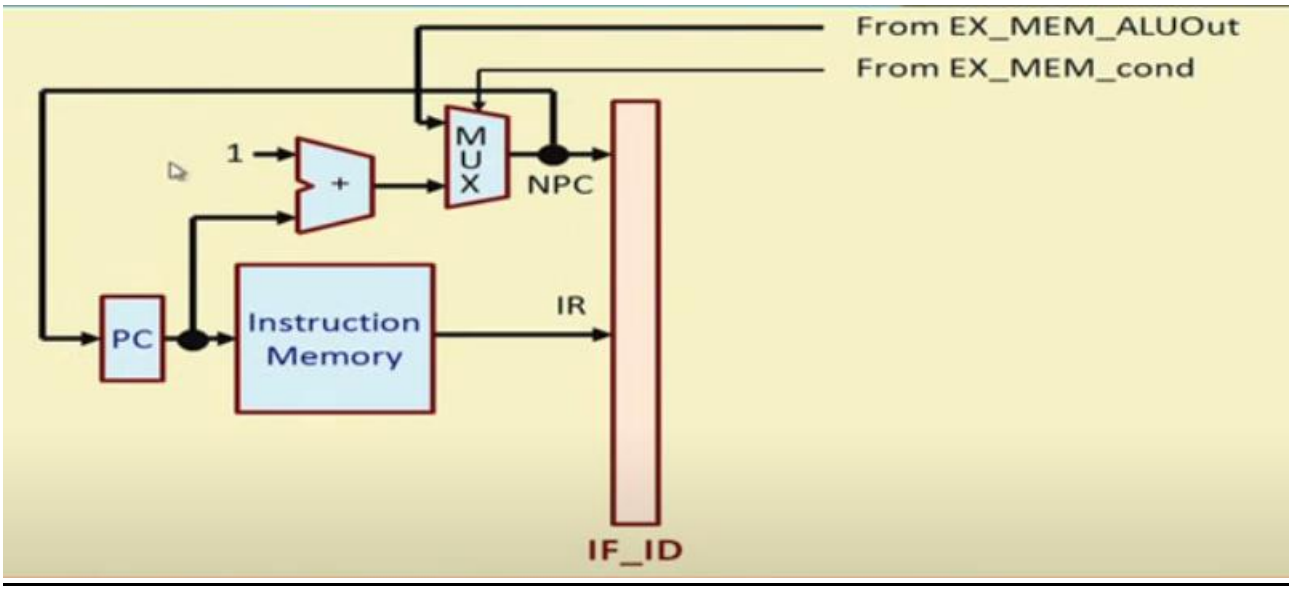
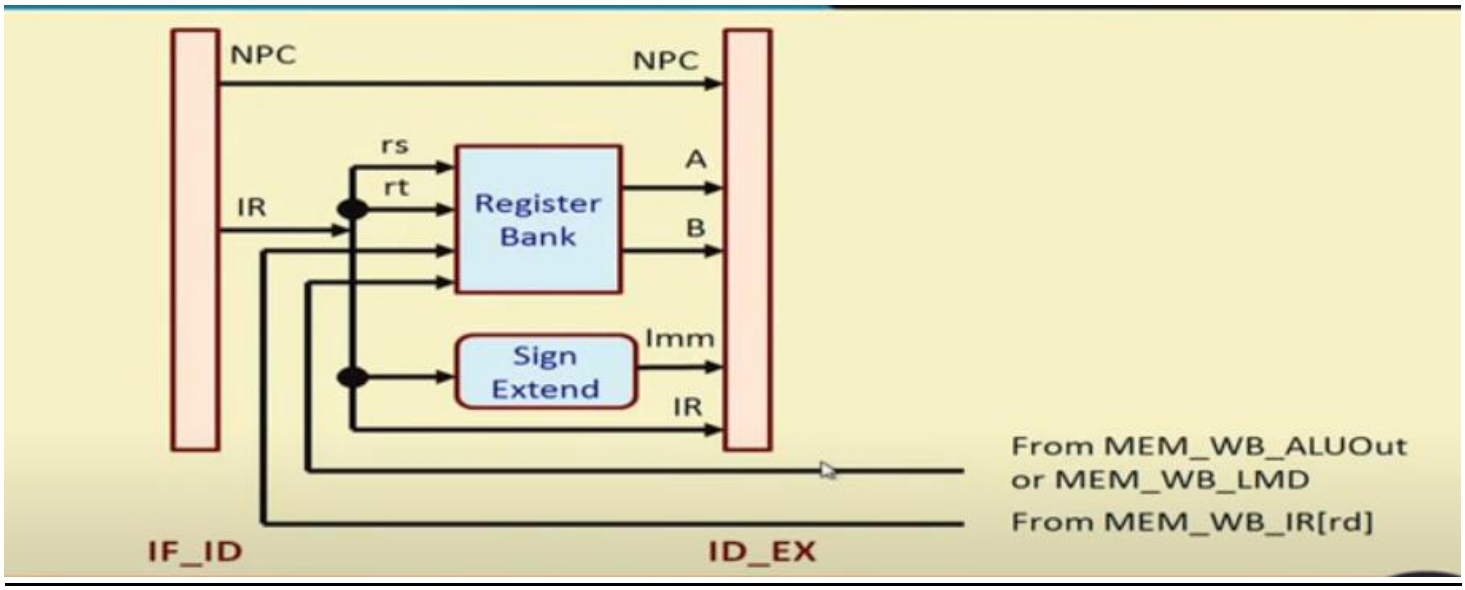
INITIAL DESIGN OF PROCESSOR



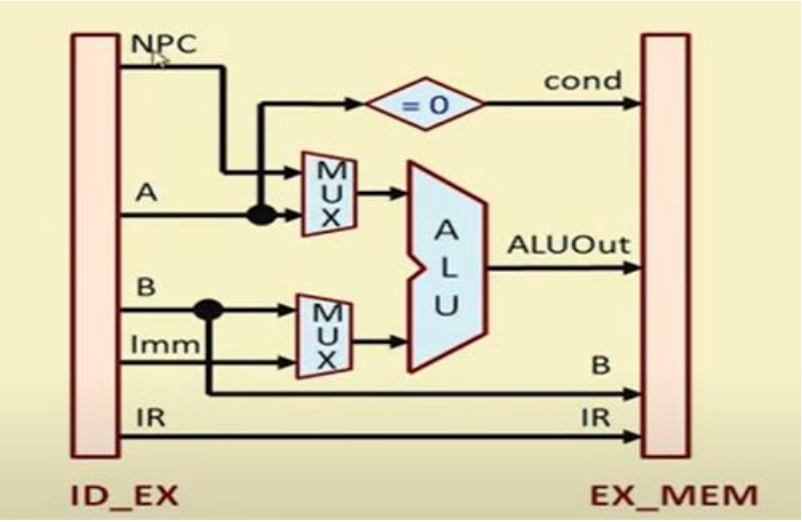
IF STAGE OF PIPELINED PROCESSOR



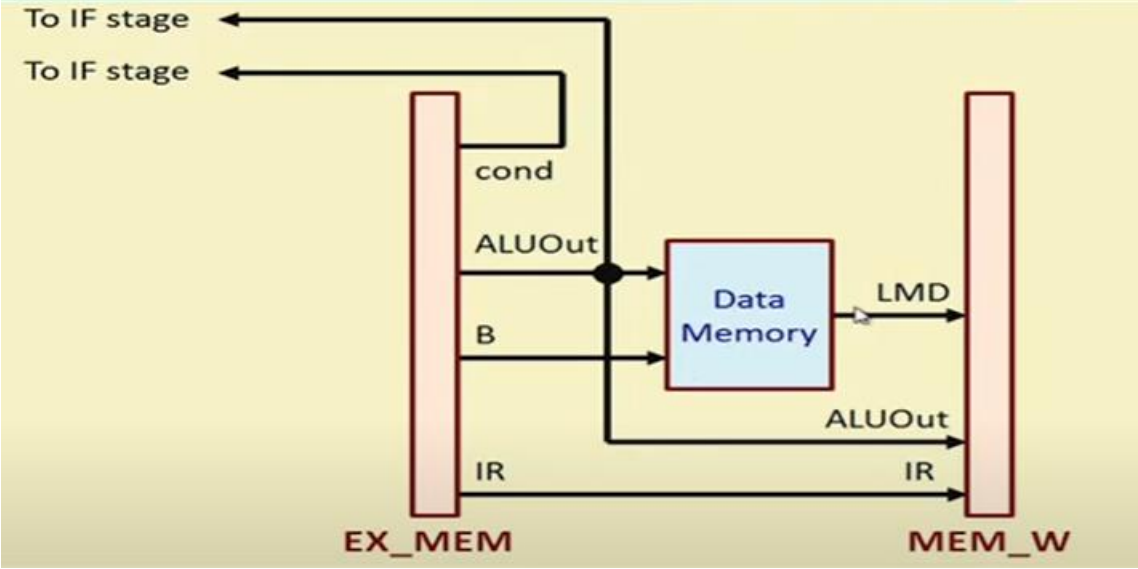
ID STAGE OF PIPELINED PROCESSOR



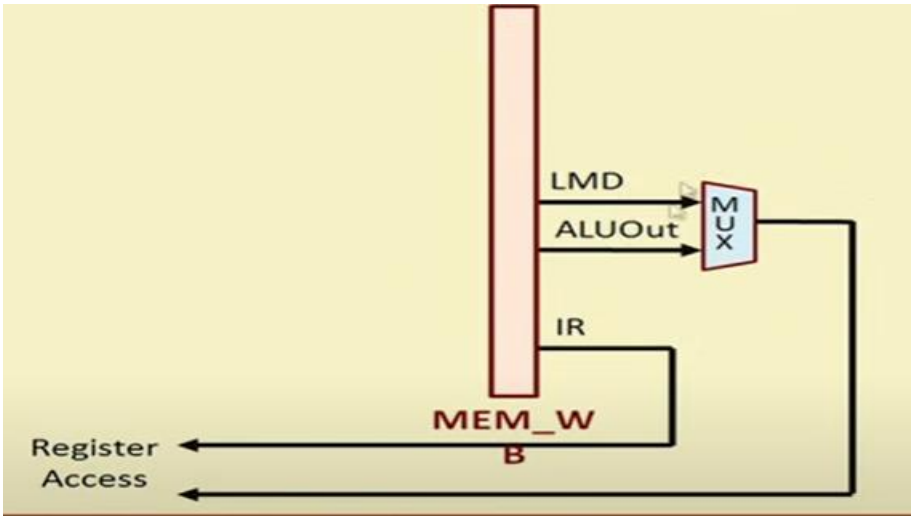
EX STAGE OF PIPELINED PROCESSOR



MEM STAGE OF PIPELINED PROCESSOR



WB STAGE OF PIPELINED PROCESSOR



FINAL PIPELINED PROCESSOR