intel

PRODUCT PREVIEW

# Intel386™ EX EMBEDDED MICROPROCESSOR

- Static Intel386™ CPU Core
  - Low Power Consumption
  - Operating Power Supply 2.7V to 5.5V
  - Operating Frequency 16 MHz at 2.7V to 3.3V; 20 MHz at 3.0V to 3.6V; 25 MHz at 4.5V to 5.5V
- Transparent Power-Management System Architecture
  - Intel System Management Mode Architecture Extension for Truly Compatible Systems
  - Power Management Transparent to Operating Systems and Application Programs
  - Programmable Power-Management Modes
- Powerdown Mode
  - Clock Stopping at Any Time
  - Only 10–20 μA Typical CPU Sink Current
- Full 32-Bit Internal Architecture
  - 8-, 16-, 32-Bit Data Types
  - 8 General Purpose 32-Bit Registers
- Runs Intel386 Architecture Software in a Cost Effective 16-Bit Hardware Environment
  - Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors
  - Object Code Compatible with 8086, 80186, 80286, and Intel386 Processors
- High Performance 16-Bit Data Bus
  - Two-Clock Bus Cycles
  - Address Pipelining Allows Use of Slower, Inexpensive Memories
- Integrated Memory Management Unit
  - Virtual Memory Support
  - Optional On-Chip Paging
  - 4 Levels of Hardware-Enforced Protection
  - MMU Fully Compatible with Those of the 80286 and Intel386 DX Processors
- Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System
- Large Uniform Address Space
  - 64 Megabyte Physical
  - 64 Terabyte Virtual
  - 4 Gigabyte Maximum Segment Size
- Numerics Support with Intel387™ SX and Intel387 SL Math Coprocessors
- On-Chip Debugging Support Including Breakpoint Registers
- Complete System Development Support
- High Speed CHMOS Technology
- Two Package Types
  - 132-Pin Plastic Quad Flatpack
  - 144-Pin Thin Quad Flatpack
- Integrated Peripheral Functions
  - Clock and Power Management Unit
  - Chip Select Unit
  - Interrupt Control Unit
  - Timer/Counter Unit
  - Watchdog Timer Unit
  - Asynchronous Serial I/O Unit
  - Synchronous Serial I/O Unit
  - Parallel I/O Unit
  - DMA and Bus Arbiter Unit
  - Refresh Control Unit
  - JTAG Boundary Scan Unit

The Intel386 EX Embedded Microprocessor is a highly integrated, 32-bit fully static CPU optimized for embedded control applications. With a 16-bit external data bus, a 26-bit external address bus, and Intel's System Management Mode (SMM), the Intel386 EX brings the vast software library of Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.



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Order Number: 272420-001

# Intel386™ EX Embedded Microprocessor

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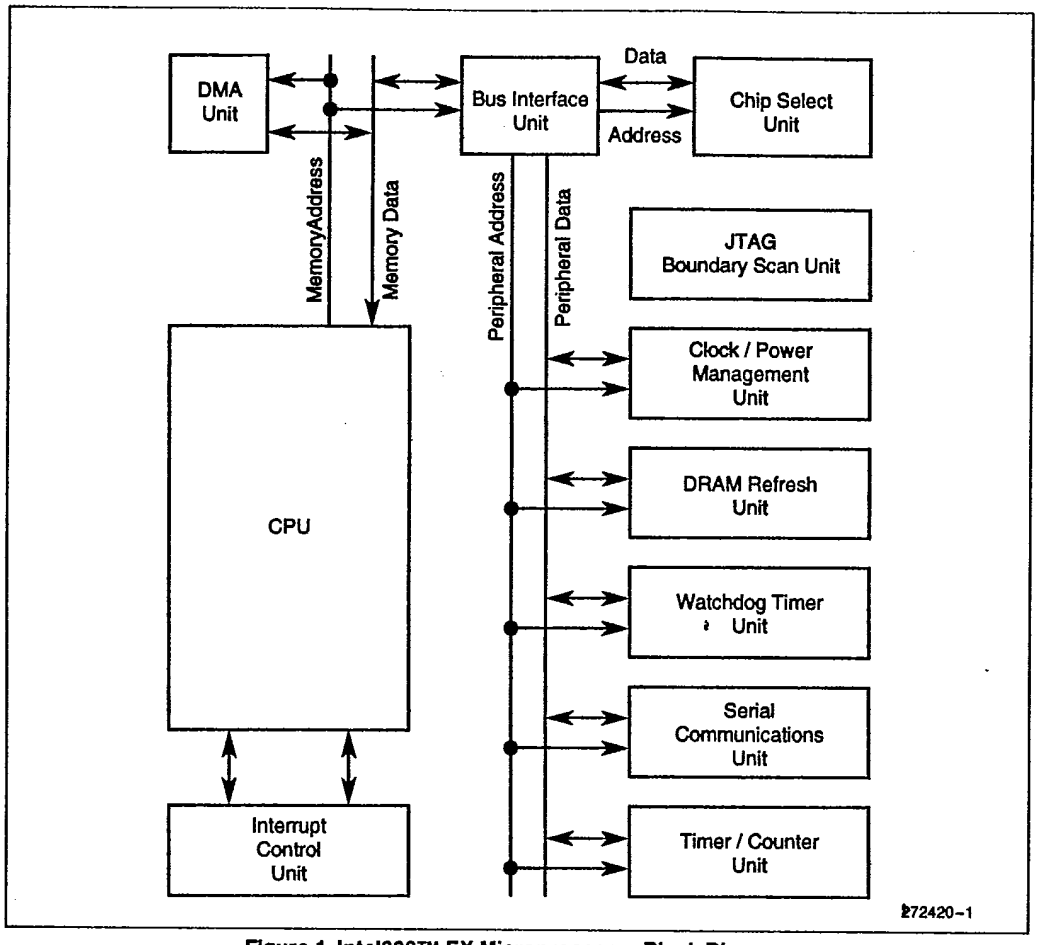


**Figure 1. Intel386™ EX Microprocessor Block Diagram**

## 1.0 PIN ASSIGNMENT

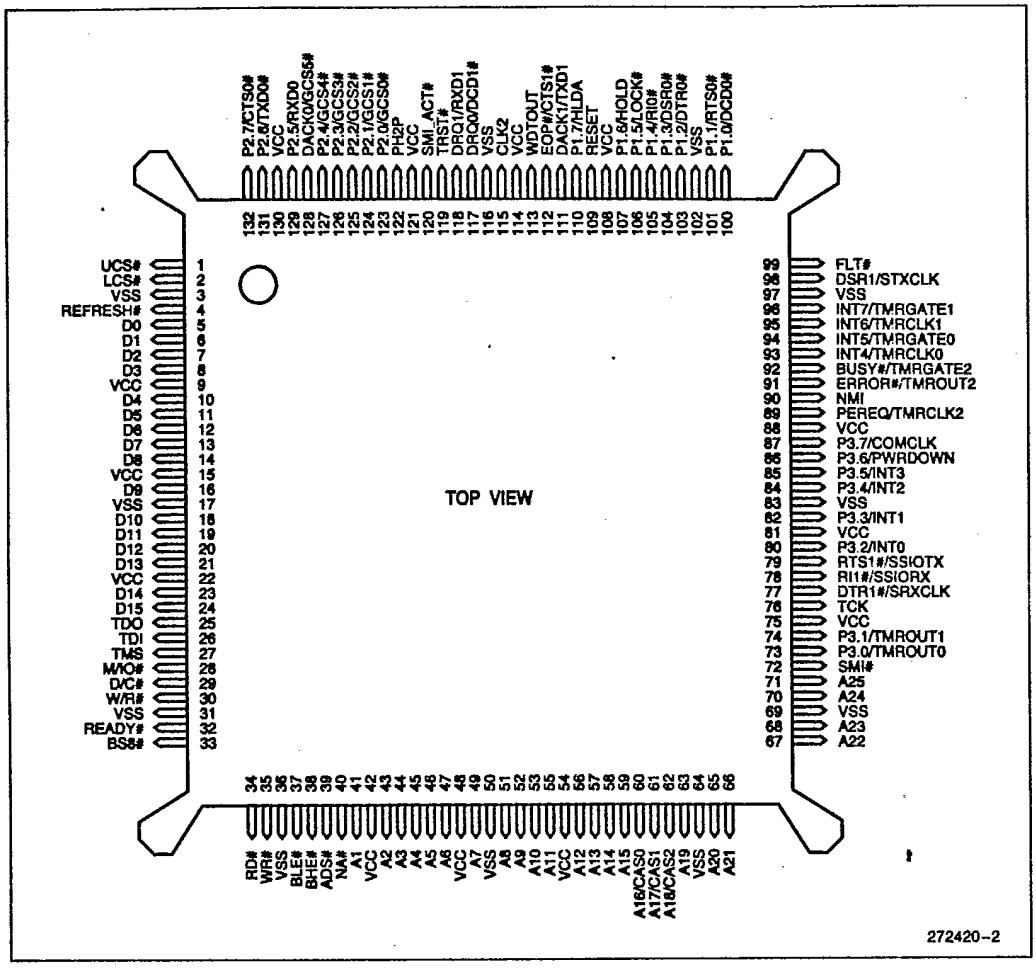


**Figure 2. Intel386™ EX Microprocessor 132-Pin PQFP Pin Assignment**

Table 1. 132-Pin PQFP Pin Assignment

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | UCS# | 34 | RD# | 67 | A22 | 100 | P1.0/DCD0# |
| 2 | LCS# | 35 | WR# | 68 | A23 | 101 | P1.1/RTS0# |
| 3 | $V_{SS}$ | 36 | $V_{SS}$ | 69 | $V_{SS}$ | 102 | $V_{SS}$ |
| 4 | REFRESH# | 37 | BLE# | 70 | A24 | 103 | P1.2/DTR0# |
| 5 | D0 | 38 | BHE# | 71 | A25 | 104 | P1.3/DSR0# |
| 6 | D1 | 39 | ADS# | 72 | SMI# | 105 | P1.4/RI0# |
| 7 | D2 | 40 | NA# | 73 | P3.0/TMROUT0 | 106 | P1.5/LOCK# |
| 8 | D3 | 41 | A1 | 74 | P3.1/TMROUT1 | 107 | P1.6/HOLD |
| 9 | $V_{CC}$ | 42 | $V_{CC}$ | 75 | $V_{CC}$ | 108 | $V_{CC}$ |
| 10 | D4 | 43 | A2 | 76 | TCK | 109 | RESET |
| 11 | D5 | 44 | A3 | 77 | DTR1#/SRXCLK | 110 | P1.7/HLDA |
| 12 | D6 | 45 | A4 | 78 | RI1#/SSIORX | 111 | DACK1/TXD1 |
| 13 | D7 | 46 | A5 | 79 | RTS1#/SSIOTX | 112 | EOP#/CTS1# |
| 14 | D8 | 47 | A6 | 80 | P3.2/INT0 | 113 | WDTOUT |
| 15 | $V_{CC}$ | 48 | $V_{CC}$ | 81 | $V_{CC}$ | 114 | $V_{CC}$ |
| 16 | D9 | 49 | A7 | 82 | P3.3/INT1 | 115 | CLK2 |
| 17 | $V_{SS}$ | 50 | $V_{SS}$ | 83 | $V_{SS}$ | 116 | $V_{SS}$ |
| 18 | D10 | 51 | A8 | 84 | P3.4/INT2 | 117 | DRQ0/DCD1# |
| 19 | D11 | 52 | A9 | 85 | P3.5/INT3 | 118 | DRQ1/RXD1 |
| 20 | D12 | 53 | A10 | 86 | P3.6/PWRDOWN | 119 | TRST# |
| 21 | D13 | 54 | A11 | 87 | P3.7/COMCLK | 120 | SMI_ACT# |
| 22 | $V_{CC}$ | 55 | $V_{CC}$ | 88 | $V_{CC}$ | 121 | $V_{CC}$ |
| 23 | D14 | 56 | A12 | 89 | PEREQ/TMRCLK2 | 122 | PH2P |
| 24 | D15 | 57 | A13 | 90 | NMI | 123 | P2.0/GCS0# |
| 25 | TDO | 58 | A14 | 91 | ERROR#/TMROUT2 | 124 | P2.1/GCS1# |
| 26 | TDI | 59 | A15 | 92 | BUSY#/TMRGATE2 | 125 | P2.2/GCS2# |
| 27 | TMS | 60 | A16/CAS0 | 93 | INT4/TMRCLK0 | 126 | P2.3/GCS3# |
| 28 | M/IO# | 61 | A17/CAS1 | 94 | INT5/TMRGATE0 | 127 | P2.4/GCS4# |
| 29 | D/C# | 62 | A18/CAS2 | 95 | INT6/TMRCLK1 | 128 | DACK0/GCS5# |
| 30 | W/R# | 63 | A19 | 96 | INT7/TMRGATE1 | 129 | P2.5/RXD0 |
| 31 | $V_{SS}$ | 64 | $V_{SS}$ | 97 | $V_{SS}$ | 130 | $V_{SS}$ |
| 32 | READY# | 65 | A20 | 98 | DSR1/STXCLK | 131 | P2.6/TXD0# |
| 33 | BS8# | | | 99 | FLT# | 132 | P2.7/CTS0# |

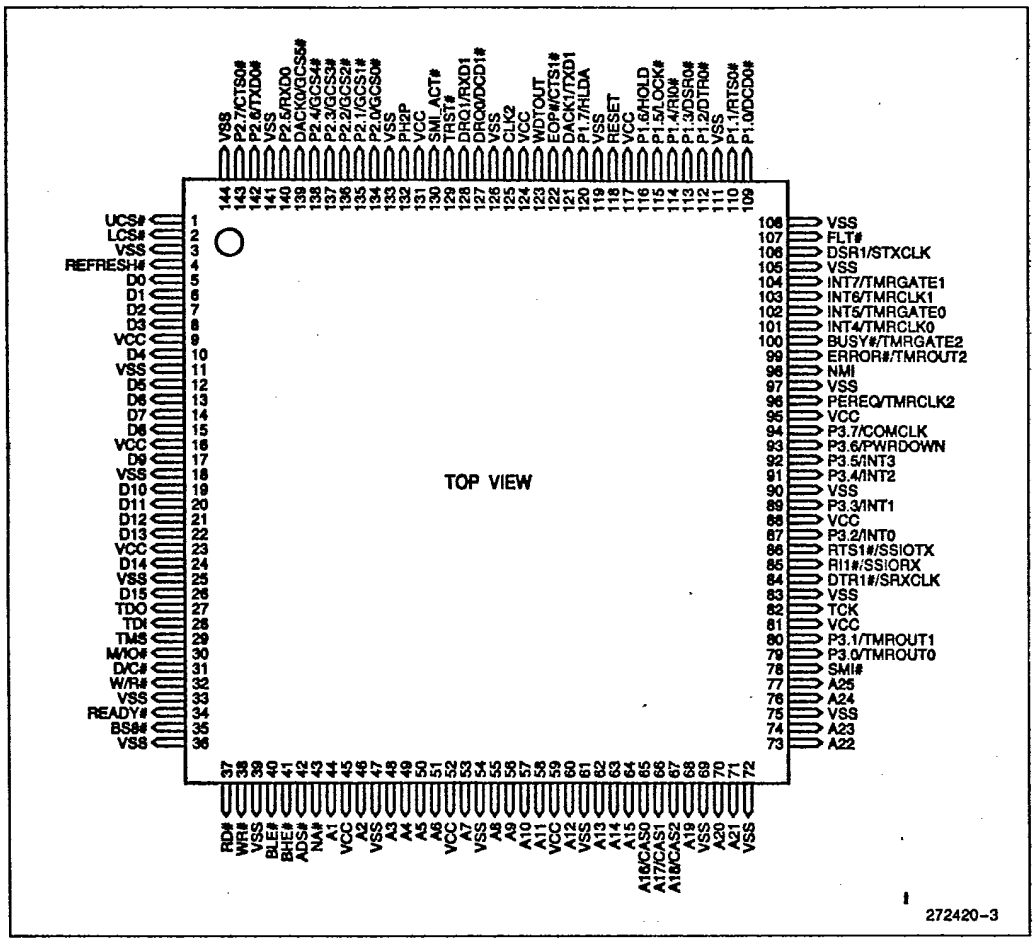


Figure 3. Intel386™ EX Microprocessor 144-Pin TQFP Pin Assignment

**Table 2. 144 Pin TQFP Pin Assignment**

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | UCS# | 37 | RD# | 73 | A22 | 109 | P1.0/DCD0# |
| 2 | LCS# | 38 | WR# | 74 | A23 | 110 | P1.1/RTS0# |
| 3 | $V_{SS}$ | 39 | $V_{SS}$ | 75 | $V_{SS}$ | 111 | $V_{SS}$ |
| 4 | REFRESH# | 40 | BLE# | 76 | A24 | 112 | P1.2/DTR0# |
| 5 | D0 | 41 | BHE# | 77 | A25 | 113 | P1.3/DSR0# |
| 6 | D1 | 42 | ADS# | 78 | SMI# | 114 | P1.4/RI0# |
| 7 | D2 | 43 | NA# | 79 | P3.0/TMROUT0 | 115 | P1.5/LOCK# |
| 8 | D3 | 44 | A1 | 80 | P3.1/TMROUT1 | 116 | P1.6/HOLD |
| 9 | $V_{CC}$ | 45 | $V_{CC}$ | 81 | $V_{CC}$ | 117 | $V_{CC}$ |
| 10 | D4 | 46 | A2 | 82 | TCK | 118 | RESET |
| 11 | $V_{SS}$ | 47 | $V_{SS}$ | 83 | $V_{SS}$ | 119 | $V_{SS}$ |
| 12 | D5 | 48 | A3 | 84 | DTR1#/SRXCLK | 120 | P1.7/HLDA |
| 13 | D6 | 49 | A4 | 85 | RI1#/SSIORX | 121 | DACK1/TXD1 |
| 14 | D7 | 50 | A5 | 86 | RTS1#/SSIOTX | 122 | EOP#/CTS1# |
| 15 | D8 | 51 | A6 | 87 | P3.2/INT0 | 123 | WDTOUT |
| 16 | $V_{CC}$ | 52 | $V_{CC}$ | 88 | $V_{CC}$ | 124 | $V_{CC}$ |
| 17 | D9 | 53 | A7 | 89 | P3.3/INT1 | 125 | CLK2 |
| 18 | $V_{SS}$ | 54 | $V_{SS}$ | 90 | $V_{SS}$ | 126 | $V_{SS}$ |
| 19 | D10 | 55 | A8 | 91 | P3.4/INT2 | 127 | DRQ0/DCD1# |
| 20 | D11 | 56 | A9 | 92 | P3.5/INT3 | 128 | DRQ1/RXD1 |
| 21 | D12 | 57 | A10 | 93 | P3.6/PWRDOWN | 129 | TRST# |
| 22 | D13 | 58 | A11 | 94 | P3.7/COMCLK | 130 | SMI_ACT# |
| 23 | $V_{CC}$ | 59 | $V_{CC}$ | 95 | $V_{CC}$ | 131 | $V_{CC}$ |
| 24 | D14 | 60 | A12 | 96 | PEREQ/TMRCLK2 | 132 | PH2P |
| 25 | $V_{SS}$ | 61 | $V_{SS}$ | 97 | $V_{SS}$ | 133 | $V_{SS}$ |
| 26 | D15 | 62 | A13 | 98 | NMI | 134 | P2.0/GCS0# |
| 27 | TDO | 63 | A14 | 99 | ERROR#/TMROUT2 | 135 | P2.1/GCS1# |
| 28 | TDI | 64 | A15 | 100 | BUSY#/TMRGATE2 | 136 | P2.2/GCS2# |
| 29 | TMS | 65 | A16/CAS0 | 101 | INT4/TMRCLK0 | 137 | P2.3/GCS3# |
| 30 | M/IO# | 66 | A17/CAS1 | 102 | INT5/TMRGATE0 | 138 | P2.4/GCS4# |
| 31 | D/C# | 67 | A18/CAS2 | 103 | INT6/TMRCLK1 | 139 | DACK0/GCS5# |
| 32 | W/R# | 68 | A19 | 104 | INT7/TMRGATE1 | 140 | P2.5/RXD0 |
| 33 | $V_{SS}$ | 69 | $V_{SS}$ | 105 | $V_{SS}$ | 141 | $V_{SS}$ |
| 34 | READY# | 70 | A20 | 106 | DSR1/STXCLK | 142 | P2.6/TXD0# |
| 35 | BS8# | 71 | A21 | 107 | FLT# | 143 | P2.7/CTS0# |
| 36 | $V_{SS}$ | 72 | $V_{SS}$ | 108 | $V_{SS}$ | 144 | $V_{SS}$ |

## 2.0 PIN DESCRIPTIONS

Table 3 lists the Intel386 EX microprocessor pin descriptions. The following definitions are used in the pin descriptions:

- # The named signal is active low.
- I Standard CMOS Input signal.
- O Standard CMOS Output signal.
- I/O Input and Output signal.
- I/OD Input and Open-Drain Output signal.
- ST Schmitt-Triggered Input signal.
- P Power pin.
- G Ground pin.

**Table 3. Intel386™ EX Microprocessor Pin Descriptions**

| Symbol | Type | Name and Function |
|---|---|---|
| A25:1 | O | **Address Bus** outputs physical memory or port I/O addresses. These signals are valid when ADS# is active and remain valid until the next T1, T2P, or Ti. During HOLD cycles they are driven to a high-impedance state. A18:16 are multiplexed with CAS2:0. |
| ADS# | O | **Address Status** indicates that the processor is driving a valid bus-cycle definition and address (W/R#, D/C#, M/IO#, A25:1, BHE#, BLE#) onto its pins. |
| BHE# | O | **Byte High Enable** indicates that the processor is transferring a high data byte. |
| BLE# | O | **Byte Low Enable** indicates that the processor is transferring a low data byte. |
| BS8# | I | **Bus Size** indicates that an 8-bit device is currently being addressed. |
| BUSY# | I | **Busy** indicates that the math coprocessor is busy. If BUSY# is sampled low at the falling edge of RESET, the processor performs an internal self test. BUSY# is multiplexed with TMRGATE2. |
| CAS2:0 | O | **Cascade Address** carries the slave address information from the 8259A master interrupt module during interrupt acknowledge bus cycles. CAS2:0 are multiplexed with A18:16. |
| CLK2 | ST | **Clock Input** is connected to an external clock that provides the fundamental timing for the device. |
| COMCLK | I | **Serial Communications Baud Clock** is an alternate clock source for the asynchronous serial port. COMCLK is multiplexed with P3.7. |
| CTS1:0# | I | **Clear to Send 1 and 0** prevent the transmission of data to the asynchronous serial port's RXD1 and RXD0 pin, respectively. CTS1# is multiplexed with EOP#, and CTS0# is multiplexed with P2.7. CTS1# requires an external pull-up resistor. |

**Table 3. Intel386™ EX Microprocessor Pin Descriptions** (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| D15:0 | I/O | **Data Bus** inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles. During writes, this bus is driven during phase 2 of T1 and remains active until phase 2 of the next T1, T1P, or Ti. During reads, data is latched on the falling edge of phase 2. |
| DACK1:0 | O | **DMA Acknowledge 1 and 0** signal to an external device that the processor has acknowledged the corresponding DMA request and is relinquishing the bus. DACK1 is multiplexed with TXD1, and DACK0 is multiplexed with GCS5#. |
| D/C# | O | **Data/Control** indicates whether the current bus cycle is a data cycle (memory or I/O read or write) or a control cycle (interrupt acknowledge, halt, or code fetch). |
| DCD1:0# | I | **Data Carrier Detect SIO1 and SIO0** indicate that the modem or data set has detected the corresponding asynchronous serial channel's data carrier. DCD1# is multiplexed with DRQ0, and DCD0# is multiplexed with P1.0. |
| DRQ1:0 | I | **DMA External Request 1 and 0** indicate that a peripheral requires DMA service. DRQ1 is multiplexed with RXD1, and DRQ0 is multiplexed with DCD1#. |
| DSR1:0# | I | **Data Set Ready SIO1 and SIO0** indicate that the modem or data set is ready to establish a communication link with the corresponding asynchronous serial channel. DSR1# is not multiplexed; DSR0# is multiplexed with P1.3. |
| DTR1:0# | O | **Data Terminal Ready SIO1 and SIO0** indicate that the corresponding asynchronous serial channel is ready to establish a communication link with the modem or data set. DTR1# is multiplexed with SRXCLK, and DTR0# is multiplexed with P1.2. |
| EOP# | I/OD | **End of Process** indicates that the processor has reached terminal count during a DMA transfer. An external device can also pull this pin low. EOP# is multiplexed with CTS1#. |
| ERROR# | I | **Error** indicates that the math coprocessor has an error condition. ERROR# is multiplexed with TMROUT2. |
| FLT# | I | **Float** forces all bidirectional and output signals, including HLDA, to a high-impedance state. |
| GCS5:0# | O | **General Chip Selects** are activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. GCS5# is multiplexed with DACK0, and GCS4:0# are multiplexed with P2.4:0. |
| HLDA | O | **Bus Hold Acknowledge** indicates that the processor has surrendered control of its local bus to another bus master. HLDA remains active until HOLD is deasserted. HLDA is multiplexed with P1.7. |
| HOLD | I | **Bus Hold Request** allows another bus master to request control of the local bus. HLDA active indicates that bus control has been granted. HOLD is multiplexed with P1.6. |

**Table 3. Intel386™ EX Microprocessor Pin Descriptions** (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| INT7:0 | I | **Interrupt Requests** are maskable inputs that cause the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle. They are multiplexed as follows: INT7 with TMRGATE1, INT6 with TMRCLK1, INT5 with TMRGATE0, INT4 with TMRCLK0, and INT3:0 with P3.5:2. |
| LCS# | O | **Lower Chip Select** is activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. LCS# is inactive after reset. |
| LOCK# | O | **Bus Lock** prevents other bus masters from gaining control of the system bus. LOCK# is multiplexed with P1.5. |
| M/IO# | O | **Memory/IO** Indicates whether the current bus cycle is a memory cycle or an I/O cycle. When M/IO# is high, the bus cycle is a memory cycle; when M/IO# is low, the bus cycle is an I/O cycle. |
| NA# | I | **Next Address** requests address pipelining. |
| NMI | ST | **Non-Maskable Interrupt Request** is a non-maskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge cycle. |
| PEREQ | I | **Processor Extension Request** indicates that the math coprocessor has data to transfer to the processor. PEREQ is multiplexed with TMRCLK2. |
| PHCLK | O | **Peripheral Clock** represents the processor's internal operating frequency. The PHCLK frequency decreases when the processor is in power save mode. |
| P1.7:0 | I/O | **Port 1, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P1.7 with HLDA, P1.6 with HOLD, P1.5 with LOCK#, P1.4 with RI0#, P1.3 with DSR0#, P1.2 with DTR0#, P1.1 with RTS0#, and P1.0 with DCD0#. |
| P2.7:0 | I/O | **Port 2, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P2.7 with CTS0#, P2.6 with TXD0, P2.5 with RXD0, and P2.4:0 with GCS4:0#. |
| P3.7:0 | I/O | **Port 3, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P3.7 with COMCLK, P3.6 with PWRDOWN, P3.5:2 with INT3:0, and P3.1:0 with TMROUT1:0. |
| PWRDOWN | O | **Powerdown** indicates that the processor is in powerdown mode. PWRDOWN is multiplexed with P3.6. |
| RD# | O | **Read Enable** indicates that the current bus cycle is a read cycle. |
| READY# | I/OD | **Ready** indicates that the current bus transaction has completed. An external device or an internal signal can drive READY#. Internally, the chip-select wait-state logic can generate the ready signal and drive the READY# pin active. |

**Table 3. Intel386™ EX Microprocessor Pin Descriptions** (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| RESET | ST | **Reset** suspends any operation in progress and places the processor into a known reset state. |
| RFSH# | O | **Refresh** indicates that the current bus cycle is a refresh cycle. |
| RI1:0# | I | **Ring Indicator SIO1 and SIO0** indicate that the modem or data set has received a telephone ringing signal. RI1# is multiplexed with SSIORX, and RI0# is multiplexed with P1.4. |
| RTS1:0# | O | **Request-to-Send SIO1 and SIO0** indicate that corresponding asynchronous serial channel is ready to exchange data with the modem or data set. RTS1# is multiplexed with SSIOTX, and RTS0# is multiplexed with P1.1. |
| RXD1:0 | I | **Receive Data SIO1 and SIO0** accept serial data from the modem or data set to the corresponding asynchronous serial channel. RXD1 is multiplexed with DRQ1, and RXD0 is multiplexed with P2.5. |
| SMI# | ST | **System Management Interrupt** invokes System Management Mode (SMM). SMI# is the highest priority interrupt. It is latched on its falling edge and it forces the CPU into SMM upon completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# cannot interrupt LOCKed bus cycles or a currently executing SMM. If the processor receives a second SMI# while it is in SMM, it will latch the second SMI# on the SMI# falling edge. However, the processor must exit SMM by executing a Resume instruction (RSM) before it can service the second SMI#. |
| SMI_ACT# | O | **System Management Interrupt Active** indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (low) until the processor executes the Resume instruction (RSM). |
| SRXCLK | I/O | **SSIO Receive Clock** synchronizes data being accepted by the synchronous serial port. SSIORX is multiplexed with DTR1#. |
| STXCLK | I/O | **SSIO Transmit Clock** synchronizes data being sent by the synchronous serial port. STXCLK is multiplexed with DSR#1. |
| SSIORX | I | **SSIO Receive Serial Data** accepts serial data (most-significant bit first) being sent to the synchronous serial port. SSIORX is multiplexed with RI1#. |
| SSIOTX | O | **SSIO Transmit Serial Data** sends serial data (most-significant bit first) from the synchronous serial port. SSIOTX is multiplexed with RTS1#. |
| TCK | I | **JTAG TAP (Test Access Port) Controller Clock** provides the clock input for the JTAG logic. |
| TDI | I | **JTAG TAP (Test Access Port) Controller Data Input** is the serial input for test instructions and data. |

**Table 3. Intel386™ EX Microprocessor Pin Descriptions** (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| TDO | O | **JTAG TAP (Test Access Port) Controller Data Output** is the serial output for test instructions and data. |
| TMRCLK2:0 | I | **Timer/Counter Clock Inputs** can serve as external clock inputs for the corresponding timer/counters. (The timer/counters can also be clocked internally.) TMRCLK2 is multiplexed with PEREQ; TMRCLK1, with INT6; and TMRCLK0, with INT4. |
| TMRGATE2:0 | I | **Timer/Counter Gate Inputs** can control the corresponding timer/counter's counting (enable, disable, or trigger, depending on the programmed mode). (Alternatively, a $V_{CC}$ pin can serve this function.) TMRGATE2 is multiplexed with BUSY#; TMRGATE1, with INT7; and TMRGATE0, with INT5. |
| TMROUT2:0 | O | **Timer/Counter Outputs** provide the output of the corresponding timer/counter. The form of the output depends on the programmed mode. TMROUT2 is multiplexed with ERROR#; TMROUT1, with P3.1; and TMROUT0, with P3.0. |
| TMS | I | **JTAG TAP (Test Access Port) Controller Mode Select** controls the sequence of the TAP controller's states. |
| TRST# | ST | **JTAG TAP (Test Access Port) Controller Reset** resets the TAP controller at power-up. |
| TXD1:0 | O | **Transmit Data SSIO1/SSIO0** transmits serial data from the individual serial channel. TXD1 is multiplexed with DACK1 and TXD0 is multiplexed with P2.6. |
| UCS# | O | **Upper Chip Select** is activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. |
| $V_{CC}$ | P | **System Power** provides the nominal DC supply input. Connected externally to a $V_{CC}$ board plane. |
| $V_{SS}$ | G | **System Ground** provides the 0V connection from which all inputs and outputs are measured. Connected externally to a ground board plane. |
| WDTOUT | O | **Watchdog Timer Output** indicates that the watchdog timer has expired. |
| W/R# | O | **Write/Read** indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is high, the bus cycle is a write cycle; when W/R# is low, the bus cycle is a read cycle. |
| WR# | O | **Write Enable** indicates that the current bus cycle is a write cycle. |

## 3.0 FUNCTIONAL DESCRIPTION

The Intel386 EX microprocessor is a fully static, 32-bit processor optimized for embedded applications. It features low power and low voltage capabilities, integration of many commonly used DOS-type peripherals, and a 32-bit programming architecture compatible with the large software base of Intel386 processors. The following sections provide an overview of the integrated peripherals.

### 3.1 Clock Generation and Power Management Unit

The clock generation circuit includes a divide-by-two counter, a programmable divider for generating a prescaled clock (PSCLK), a divide-by-three counter for generating baud rate clock inputs, a power-save clock divider circuit, and Reset circuitry. The CLK2 input provides the fundamental timing for the chip. It is divided by two internally to generate a 50% duty cycle Phase1 (PH1) and Phase 2 (PH2) for the core and integrated peripherals. For power management, separate clocks are routed to the core (PH1C/PH2C) and the peripheral modules (PH1P/PH2P).

Three Power Management modes are provided for flexible power-saving options. During Idle mode, the clocks to the CPU core are frozen in a known state (PH1C low and PH2C high), while the clocks to the peripherals continue to toggle. In Powerdown mode, the clocks to both core and peripherals are frozen in a known state (PH1C low and PH2C high). The Bus Interface Unit will not honor any DMA, DRAM refresh, or HOLD requests in Powerdown mode because the clocks to the entire device are frozen. In Power-save mode, a programmable divider decreases the frequency of the incoming CLK2 signal. Allowable clock division settings are 1, 2, 4, 8, 16, 32, and 64 (divide-by-1 has no effect). Once Power-save is enabled, the core and peripherals continue to run at the divided clock rate. The prescaled clock (PSCLK) and the baud input clock do not change frequency in Power-save mode.

### 3.2 Chip Select Unit

The Chip Select Unit (CSU) decodes bus cycle address and status information and enables the appropriate chip-selects. The individual chip-selects become valid in the same bus state as the address and become inactive when either a new address is selected or the current bus cycle is complete.

The CSU is divided into eight separate chip-select regions, each of which can enable one of the eight chip-select pins. Each chip-select region can be mapped into memory or I/O space. A memory-mapped chip-select region can start on any $2^n$ Kbyte address location (where n = 0–22, depending upon the mask register). An I/O-mapped chip-select region can start on any $2^n$ word address location (where n = 0–15, depending upon the mask register). The size of the region is also dependent upon the mask used.

### 3.3 Interrupt Control Unit

The Intel386 EX microprocessor's Interrupt Control Unit (ICU) contains two 8259A modules connected in a cascade mode. The 8259A modules make up the heart of the ICU. These modules are similar to the industry-standard 8259A architecture.

The Interrupt Control Unit directly supports up to eight external (INT7:0) and up to eight internal (IR7:0) interrupt request signals. Pending interrupt requests are posted in the Interrupt Request Register, which contains one bit for each interrupt request signal. When an interrupt request is asserted, the corresponding Interrupt Request Register bit is set. The 8259A module can be programmed to recognize either an active-high level or a positive transition on the interrupt request lines. An internal Priority Resolver decides which pending interrupt request (if more than one exists) is the highest priority, based on the programmed operating mode. The Priority Resolver controls the single interrupt request line to the CPU. The Priority Resolver's default priority scheme places IR0 as the highest priority and IR7 as the lowest. The priority can be modified through software.

Besides the eight interrupt request inputs available to the Intel386 EX microprocessor, additional interrupts can be supported by cascaded external 8259A modules. Up to four external 8259A units can be cascaded to the master through connections to the INT3:0 pins. In this configuration, the interrupt acknowledge (INTA#) signal can be decoded externally using the ADS#, D/C#, R/W#, and M/IO# signals.

## 3.4 Timer/Counter Unit

The Timer/Counter unit on the Intel386 EX microprocessor has the same basic functionality as the industry-standard 82C54 counter/timer. It provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. This maximum frequency must be considered when programming the input clocks for the counters. Six programmable timer modes allow the timers to be used as event counters, elapsed-time indicators, programmable one-shots, and in many other applications. All modes are software programmable.

## 3.5 Watchdog Timer Unit

The Watchdog Timer (WDT) unit consists of a 32-bit down-counter that decrements every PH1P cycle, allowing up to 4.3 billion count intervals. The WDTOUT pin is driven high for sixteen CLK2 cycles when the down-counter reaches zero (the WDT times out). The WDTOUT signal can be used to reset the chip, to request an interrupt, or to indicate to the user that a ready-hang situation has occurred. The down-counter can also be updated with a user-defined 32-bit reload value under certain conditions. Alternatively, the WDT unit can be used as a bus monitor or as a general-purpose timer.

## 3.6 Asynchronous Serial I/O Unit

The Intel386 EX microprocessor's asynchronous serial I/O (SIO) unit is a Universal Asynchronous Receiver/ Transmitter (UART). Functionally, it is equivalent to the National Semiconductor NS16450 and INS8250. The Intel386 EX microprocessor contains two asynchronous serial channels.

The SIO unit converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the CPU to serial data. The CPU can read the status of the serial port at any time during its operation. The status information includes the type and condition of the transfer operations being performed and any errors (parity, framing, overrun, or break interrupt).

Each asynchronous serial channel includes full modem control support (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#) and is completely programmable. The programmable options include character length (5, 6, 7, or 8 bits), stop bits (1, 1.5, or 2), and parity (even, odd, forced, or none). In addition, it contains a programmable baud rate generator capable of DC to 512 Kbaud.

## 3.7 Synchronous Serial I/O Unit

The Synchronous Serial I/O (SSIO) unit provides for simultaneous, bidirectional communications. It consists of a transmit channel, a receive channel, and a dedicated baud rate generator. It is compatible with several popular synchronous protocols. The transmit and receive channels can be operated independently (with different clocks) to provide non-lockstep, full-duplex communications; either channel can originate the clocking signal (Master Mode) or receive an externally generated clocking signal (Slave Mode).

The SSIO provides numerous features for ease and flexibility of operation. With a maximum clock input of 20 MHz to the baud rate generator, the SSIO can deliver a baud rate of 5 Mbits per second. Each channel is double buffered. The two channels share the baud rate generator and a multiply-by-four transmit and receive clock. The SSIO supports 16-bit serial communications with independently enabled transmit and receive functions and gated interrupt outputs to the interrupt controller.

## 3.8 Parallel I/O Unit

The Intel386 EX microprocessor has three 8-bit, general-purpose I/O ports. All port pins are bidirectional, with CMOS-level input and outputs. All pins have both a standard operating mode and a peripheral mode (a multiplexed function), and all have similar sets of control registers located in I/O address space. Ports 1 and 2 provide 8 mA of drive capability, while port 3 provides 16 mA.

## 3.9 DMA and Bus Arbiter Unit

The Intel386 EX microprocessor's DMA controller is a two-channel DMA; each channel operates independently of the other. Within the operation of the individual channels, several different data transfer modes are available. These modes can be combined in various configurations to provide a very versatile DMA controller. Its feature set has enhancements beyond the 8237 DMA family; however, it can be configured such that it can be used in an 8237-like mode. Each channel can transfer data between any combination of memory and I/O with any combination (8 or 16 bits) of data path widths. An internal temporary register that can disassemble or assemble data to or from either an aligned or a nonaligned destination or source optimizes bus bandwidth.

The bus arbiter, a part of the DMA controller, works much like the priority resolving circuitry of a DMA. It receives service requests from the two DMA channels, the external bus master, and the DRAM Refresh controller. The bus arbiter requests bus ownership from the core and resolves priority issues among all active requests when bus mastership is granted.

Each DMA channel consists of three major components: the Requestor, the Target, and the Byte Count. These components are identified by the contents of programmable registers that define the memory or I/O device being serviced by the DMA. The Requestor is the device that requires and requests service from the DMA controller. Only the Requestor is considered capable of initializing or terminating a DMA process. The Target is the device with which the Requestor wishes to communicate. The DMA process considers the Target a slave that is incapable of controlling the process. The Byte Count dictates the amount of data that must be transferred.

## 3.10 Refresh Control Unit

The Refresh Control Unit (RCU) simplifies dynamic memory controller design with its integrated address and clock counters. Integrating the RCU into the processor allows an external DRAM controller to use chip-selects, wait state logic, and status lines.

The Intel386 EX microprocessor's RCU consists of four basic functions. First, it provides a programmable-interval timer that keeps track of time. Second, it provides the bus arbitration logic to gain control of the bus to run refresh cycles. Third, it contains the logic to generate row addresses to refresh DRAM rows individually. And fourth, it contains the logic to signal the start of a refresh cycle.

Additionally, it contains a 13-bit address counter that forms the refresh address, supporting DRAMs with up to 13 rows of memory cells (13 refresh address bits). This includes all practical DRAM sizes for the Intel386 microprocessor's 64 Mbyte address space.

### 3.11 JTAG Boundary Scan Unit

The JTAG Boundary Scan Unit provides access to the device pins and to a number of other testable areas on the device. It is fully compliant with the IEEE 1149.1 standard and thus interfaces with five JTAG-dedicated pins: TRST#, TCK, TMS, TDI, and TDO. It contains the Test Access Port (TAP) finite-state machine, a 4-bit instruction register, a 32-bit identification register, a single-bit bypass register, and an 8-bit test mode register. The JTAG unit also contains the necessary logic to generate clock and control signals for the chains that reside outside the JTAG unit itself: the SCANOUT and Boundary Scan chains.

Since the JTAG unit has its own clock and reset signals, it can operate autonomously. Thus, while the rest of the microprocessor is in Reset or Powerdown, the JTAG unit can read or write various register chains. This feature can be used, for example, to write to the test mode register while the rest of the chip is in Reset or Powerdown. Then when the microprocessor exits Reset or Powerdown, it will enter the specified test mode.

## 4.0 DESIGN CONSIDERATIONS

This section describes the Intel386 EX microprocessor's instruction set and its component and revision identifiers.

### 4.1 Instruction Set

The Intel386 EX microprocessor uses the same instruction set as the Intel386 SX microprocessor with the following exceptions.

The Intel386 EX microprocessor has one new instruction (RSM). This Resume instruction causes the processor to exit System Management Mode (SMM). RSM requires 338 clocks per instruction (CPI).

The Intel386 EX microprocessor requires more clock cycles than the Intel386 SX microprocessor to execute some instructions. Table 4 lists these instructions and the Intel386 EX microprocessor CPI. For the equivalent Intel386 SX microprocessor CPI, refer to the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).

### 4.2 Component and Revision Identifiers

To assist users, the microprocessor holds a component identifier and revision identifier in its DX register after reset. The upper 8 bits of DX hold the component identifier, 23H. (The lower nibble, 03H, identifies the Intel386 architecture, while the upper nibble, 02H, identifies the second member of the Intel386 microprocessor family.)

The lower 8 bits of DX hold the revision level identifier. The revision identifier will, in general, chronologically track those component steppings that are intended to have certain improvements or distinction from previous steppings. The revision identifier will track that of the Intel386 CPU whenever possible. However, the revision identifier value is not guaranteed to change with every stepping revision or to follow a completely uniform numerical sequence, depending on the type or intent of the revision or the manufacturing materials required to be changed. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Intel386 EX microprocessor is 09H.

**Table 4. Intel386™ CX Microprocessor Clocks Per Instruction**

| Instruction | Clock Count | | |
|---|---|---|---|
| | Virtual 8086 Mode(1) | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode(3) |
| POPA | | 28 | 35 |
| IN: | | | |
| Fixed Port | 27 | 14 | 7/29 |
| Variable Port | 28 | 15 | 8/29 |
| OUT: | | | |
| Fixed Port | 27 | 14 | 7/29 |
| Variable Port | 28 | 15 | 9/29 |
| INS | 30 | 17 | 9/32 |
| OUTS | 31 | 18 | 10/33 |
| REP INS | 31+6n(2) | 17+6n(2) | 10+6n/32+6n(2) |
| REP OUTS | 30+8n(2) | 16+8n(2) | 10+8n/31+8n(2) |
| HLT | | 7 | 7 |
| MOV C0, reg | | 10 | 10 |

**NOTES:**
1. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).
2. n = the number of times repeated.
3. When two clock counts are listed, the smaller value refers to a register operand and the larger value refers to a memory operand.

## 5.0 DC SPECIFICATIONS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

### ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....−65°C to +150°C
Case Temperature Under Bias...−65°C to +110°C
Supply Voltage with Respect to $V_{SS}$..−0.5V to 6.5V
Voltage on Other Pins .....−0.5V to $V_{CC}$ + 0.5V

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### OPERATING CONDITIONS*

$V_{CC}$ (Digital Supply Voltage) .....2.7V to 5.5V
$T_{CASE}$ (Case Temperature Under Bias) 0°C to 100°C
$F_{OSC}$ (Operating Frequency) .....0 MHz to 25 MHz

**Table 5. DC Characteristics**

| Symbol | Parameter | Min. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (for all pins except CLK2, RESET, NMI, TRST#, and SMI#) | −0.5 | 0.3 $V_{CC}$ | V | |
| $V_{IL1}$ | Input Low Voltage (CLK2, RESET, NMI, TRST#, and SMI#) | −0.5 | 0.35 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage (for all pins except CLK2, RESET, NMI, TRST#, and SMI#) | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage (CLK2, RESET, NMI, TRST#, and SMI#) | 0.65 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage<br>All pins except Port 3<br>Port 3 | | <br>0.40<br>0.40 | <br>V<br>V | $V_{CC}$ = 4.5V to 5.5V<br>$I_{OL}$ = 8 mA<br>$I_{OL}$ = 16 mA |
| $V_{OL1}$ | Output Low Voltage<br>All pins except Port 3<br>Port 3 | | <br>0.40<br>0.40 | <br>V<br>V | $V_{CC}$ = 2.7V to 3.6V<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA |
| $V_{OH}$ | Output High Voltage<br>All pins except Port 3<br>Port 3 | <br>$V_{CC}$ −0.8<br>$V_{CC}$ − 0.8 | | <br>V<br>V | $V_{CC}$ = 4.5V to 5.5V<br>$I_{OH}$ = −8 mA<br>$I_{OH}$ = −16 mA |
| $V_{OH1}$ | Output High Voltage<br>All pins except Port 3<br>Port 3 | <br>$V_{CC}$ − 0.6<br>$V_{CC}$ − 0.6 | | <br>V<br>V | $V_{CC}$ = 2.7V to 3.6V<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA |

**Table 5. DC Characteristics** (Continued)

| Symbol | Parameter | Min. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | ±15 | µA | $0 \le V_{IN} \le V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | ±15 | µA | $0.45V \le V_{OUT} \le V_{CC}$ |
| $I_{CC}$ | Supply Current | | 140<br>200<br>420 | mA<br>mA<br>mA | 16 MHz, 3.0V<br>20 MHz, 3.3V<br>25 MHz, 5.0V |
| $I_{IDLE}$ | Idle Mode Current | | TBD | mA | |
| $I_{PSV}$ | Power-save Current | | TBD<br>TBD<br>TBD<br>TBD<br>TBD<br>TBD<br>TBD | µA<br>µA<br>µA<br>µA<br>µA<br>µA<br>µA | divide by 1 clock<br>divide by 2 clock<br>divide by 4 clock<br>divide by 8 clock<br>divide by 16 clock<br>divide by 32 clock<br>divide by 64 clock |
| $I_{PD}$ | Powerdown Current | | TBD | µA | |
| $C_S$ | Pin Capacitance (any pin to $V_{SS}$) | | TBD | pF | |

## 6.0 AC SPECIFICATIONS

Table 6 lists output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the CLK2 rising edge crossing the $V_{CC}/2$ level.

Figure 4 shows the measurement points for AC specifications. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, D/C#, MI/O#, LOCK#, BHE#, BLE#, A25:1, HLDA and SMI_ACT# change only at the beginning of phase one. D15:0 (write cycles) change only at the beginning of phase two.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, FLT#, A20M# and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, INTR, SMI# and NMI inputs are sampled at the beginning of phase two.

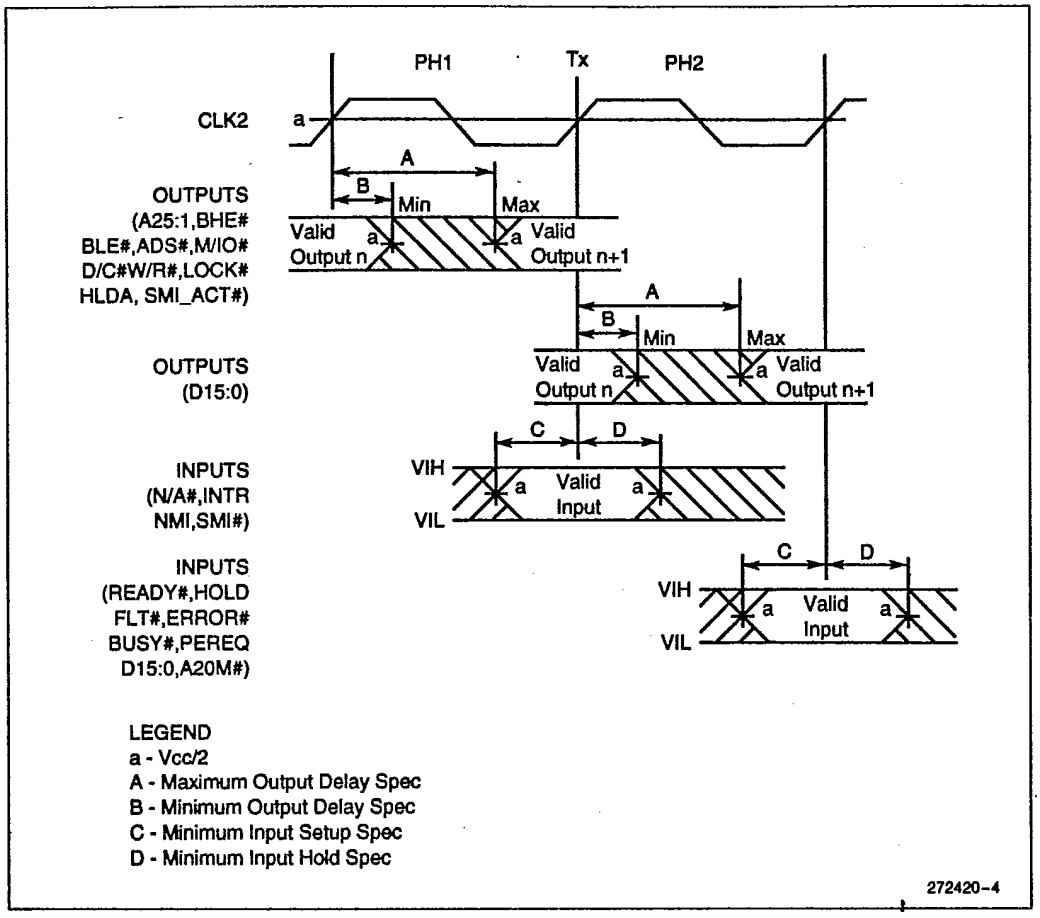


**Figure 4. Drive Levels and Measurement Points for AC Specifications**

**Table 6. AC Characteristics**

| Symbol | Parameter | 25 MHz 4.5V to 5.5V | | 20 MHz 3.0V to 3.6V | | 16 MHz 2.7V to 3.3V | | Test Conditions(1) |
|---|---|---|---|---|---|---|---|---|
| | | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | |
| | Operating Frequency | 0 | 25 | 0 | 20 | 0 | 16 | one-half CLK2 frequency in MHz(2) |
| t1 | CLK2 Period | 20 | | 25 | | 31 | | |
| t2a | CLK2 High Time | 7 | | 8 | | 9 | | at $V_{CC}/2$(3) |
| t2b | CLK2 High Time | 4 | | 5 | | 5 | | at $V_{CC}$ − 0.8V for HV, at $V_{CC}$ −0.6V for LV(3) |
| t3a | CLK2 Low Time | 7 | | 8 | | 9 | | at $V_{CC}/2$(3) |
| t3b | CLK2 Low Time | 5 | | 6 | | 7 | | at 0.8V(3) |
| t4 | CLK2 Fall Time | | 7 | | 8 | | 8 | $V_{CC}$ − 0.8V to 0.8V for HV, $V_{CC}$ − 0.6V to 0.8V for LV(3) |
| t5 | CLK2 Rise Time | | 7 | | 8 | | 8 | 0.8V to $V_{CC}$ − 0.8V for HV, 0.8V to $V_{CC}$ − 0.6V for LV(3) |
| t6 | A25:1 Valid Delay | 4 | 22 | 4 | 30 | 4 | 36 | $C_L$ = 50 pF(4) |
| t7 | A25:1 Float Delay | 4 | 30 | 4 | 32 | 4 | 40 | (Note 5) |

**NOTES:**
1. Throughout this table, HV refers to devices operating with $V_{CC}$ = 4.5V to 5.5V. LV refers to devices operating with $V_{CC}$ = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with $C_L$ set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with $C_L$ set at 120 pF and all other Note 4 timings are guaranteed with $C_L$ set at 75 pF.
5. Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

**Table 6. AC Characteristics** (Continued)

| Symbol | Parameter | 25 MHz 4.5V to 5.5V | | 20 MHz 3.0V to 3.6V | | 16 MHz 2.7V to 3.3V | | Test Conditions(1) |
|---|---|---|---|---|---|---|---|---|
| | | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | |
| t8 | BHE#, BLE#, LOCK# Valid Delay | 4 | 19 | 4 | 30 | 4 | 36 | $C_L$ = 50 pF(4) |
| t8a | SMI_ACT# Valid Delay | 4 | 19 | 4 | 26 | 4 | 33 | $C_L$ = 50 pF(4) |
| t9 | BHE#, BLE#, LOCK# Float Delay | 4 | 30 | 4 | 32 | 4 | 40 | (Note 5) |
| t10a | M/IO#, D/C# Valid Delay | 4 | 19 | 4 | 28 | 4 | 33 | $C_L$ = 50 pF(4) |
| t10b | W/R#, RD#, WR#, ADS# Valid Delay | 4 | 19 | 4 | 16 | 4 | 33 | $C_L$ = 50 pF(4) |
| t11 | W/R#, M/IO#, D/C#, RD#, WR#, ADS# Float Delay | 4 | 30 | 4 | 30 | 4 | 35 | (Note 5) |
| t12 | D15:0 Write Data Valid Delay | 4 | 28 | 4 | 38 | 4 | 40 | $C_L$ = 50 pF(4) |
| t13 | D15:0 Write DataD15:0 Write Data Float delay | 4 | 22 | 4 | 27 | 4 | 35 | (Note 5) |
| t14 | HLDA Valid Delay | 4 | 22 | 4 | 28 | 4 | 33 | $C_L$ = 50 pF(4) |
| t15 | NA# Setup Time | 5 | | 5 | | 5 | | |
| t16 | NA# Hold Time | 3 | | 12 | | 21 | | |
| t19 | READY#, A20M# Setup Time | 9 | | 12 | | 19 | | |
| t20 | READY#, A20M# Hold Time | 4 | | 4 | | 4 | | |

**NOTES:**
1. Throughout this table, HV refers to devices operating with $V_{CC}$ = 4.5V to 5.5V. LV refers to devices operating with $V_{CC}$ = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with $C_L$ set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with $C_L$ set at 120 pF and all other Note 4 timings are guaranteed with $C_L$ set at 75 pF.
5. Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

**Table 6. AC Characteristics** (Continued)

| Symbol | Parameter | 25 MHz 4.5V to 5.5V | | 20 MHz 3.0V to 3.6V | | 16 MHz 2.7V to 3.3V | | Test Conditions(1) |
|---|---|---|---|---|---|---|---|---|
| | | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | |
| t21 | D15:0 Read Setup Time | 7 | | 9 | | 9 | | |
| t22 | D15:0 Read Hold Time | 5 | | 6 | | 6 | | |
| t23 | HOLD Setup Time | 9 | | 17 | | 26 | | |
| t24 | HOLD Hold Time | 3 | | 5 | | 5 | | |
| t25 | RESET Setup Time | 8 | | 12 | | 13 | | |
| t26 | RESET Hold Time | 3 | | 4 | | 4 | | |
| t27 | NMI, INTR Setup Time | 6 | | 16 | | 16 | | (Note 6) |
| t27a | SMI# Setup Time | 6 | | 16 | | 16 | | (Note 6) |
| t28 | NMI, INTR Hold Time | 6 | | 16 | | 16 | | (Note 6) |
| t28a | SMI# Hold Time | 6 | | 16 | | 16 | | (Note 6) |
| t29 | PEREQ, ERROR#, BUSY#, FLT# Setup Time | 6 | | 14 | | 16 | | (Note 6) |
| t30 | PEREQ, ERROR#, BUSY#, FLT# Hold Time | 5 | | 5 | | 5 | | (Note 6) |

**NOTES:**
1. Throughout this table, HV refers to devices operating with $V_{CC}$ = 4.5V to 5.5V. LV refers to devices operating with $V_{CC}$ = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with $C_L$ set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with $C_L$ set at 120 pF and all other Note 4 timings are guaranteed with $C_L$ set at 75 pF.
5. Float condition occurs when maximum output current becomes less than $I_{LO}$ in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

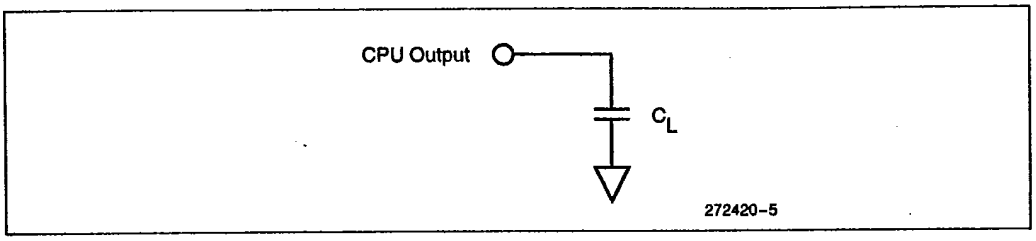


**Figure 5. AC Test Loads**

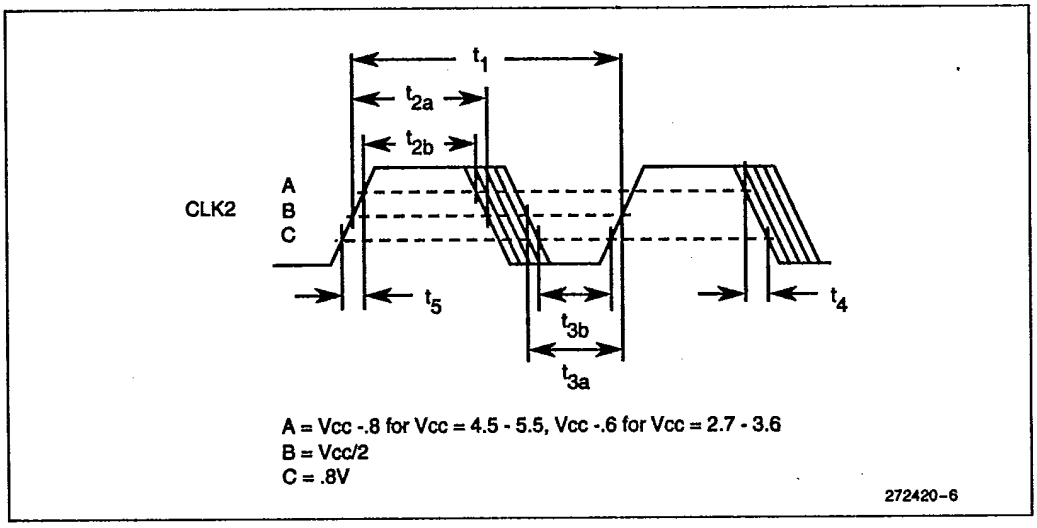


**Figure 6. CLK2 Waveform**

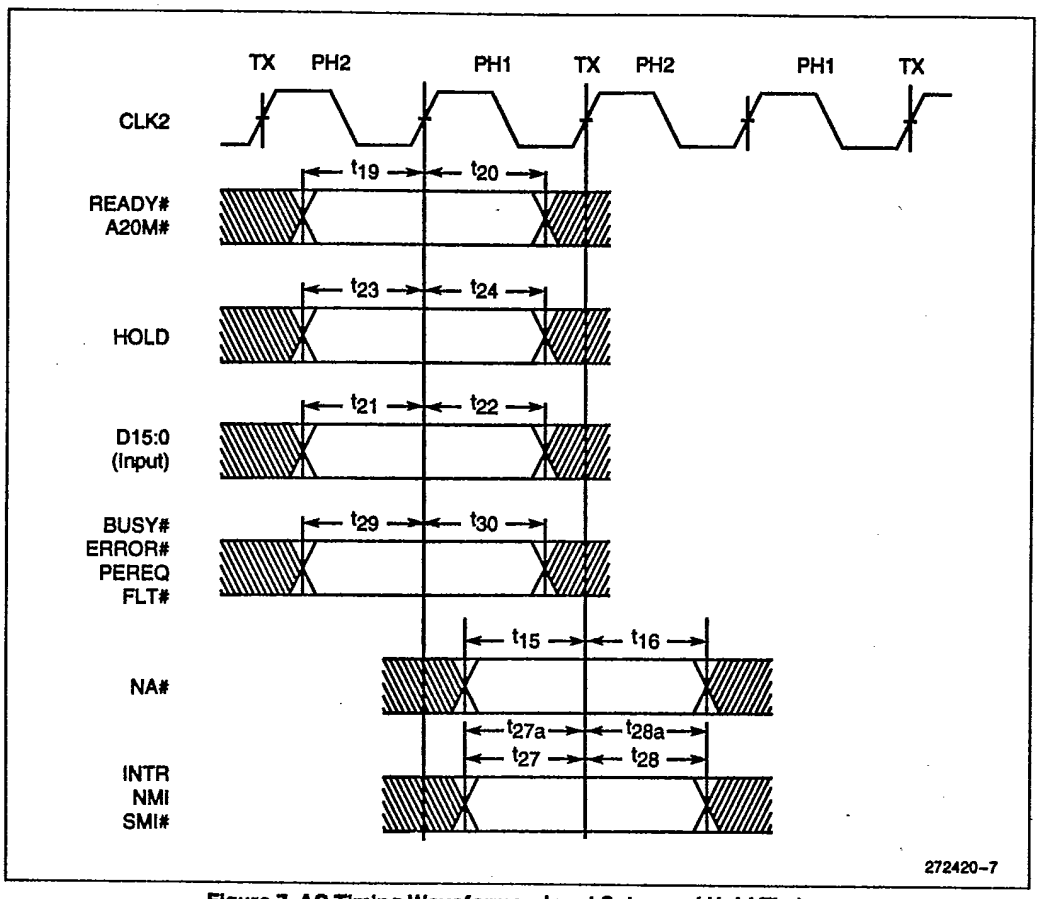


**Figure 7. AC Timing Waveforms—Input Setup and Hold Timing**

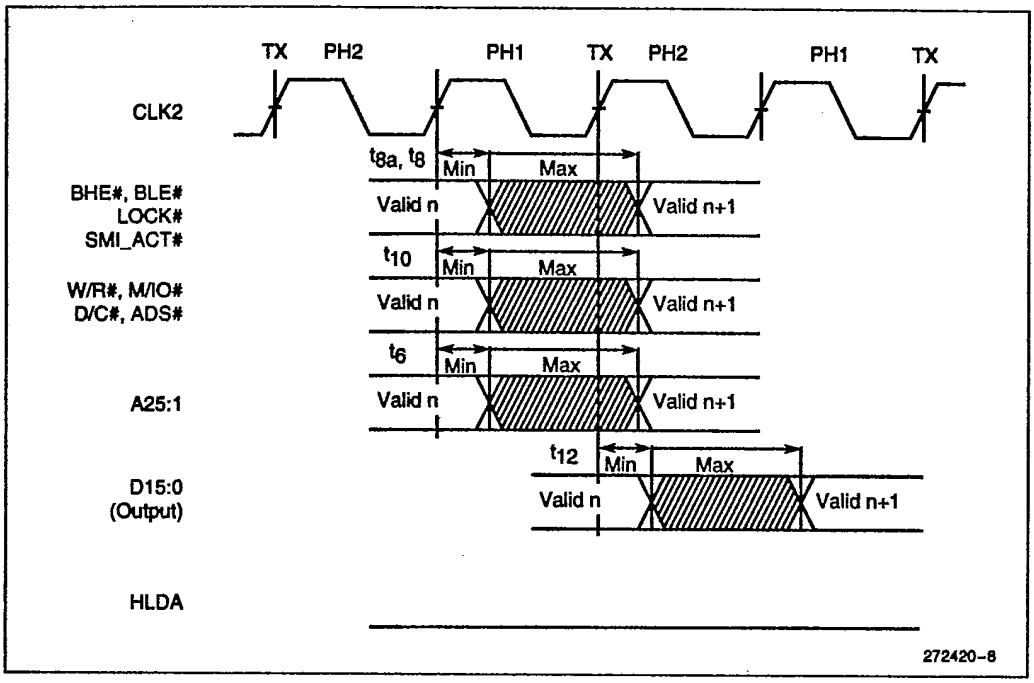


**Figure 8. AC Timing Waveforms—Output Valid Delay Timing**

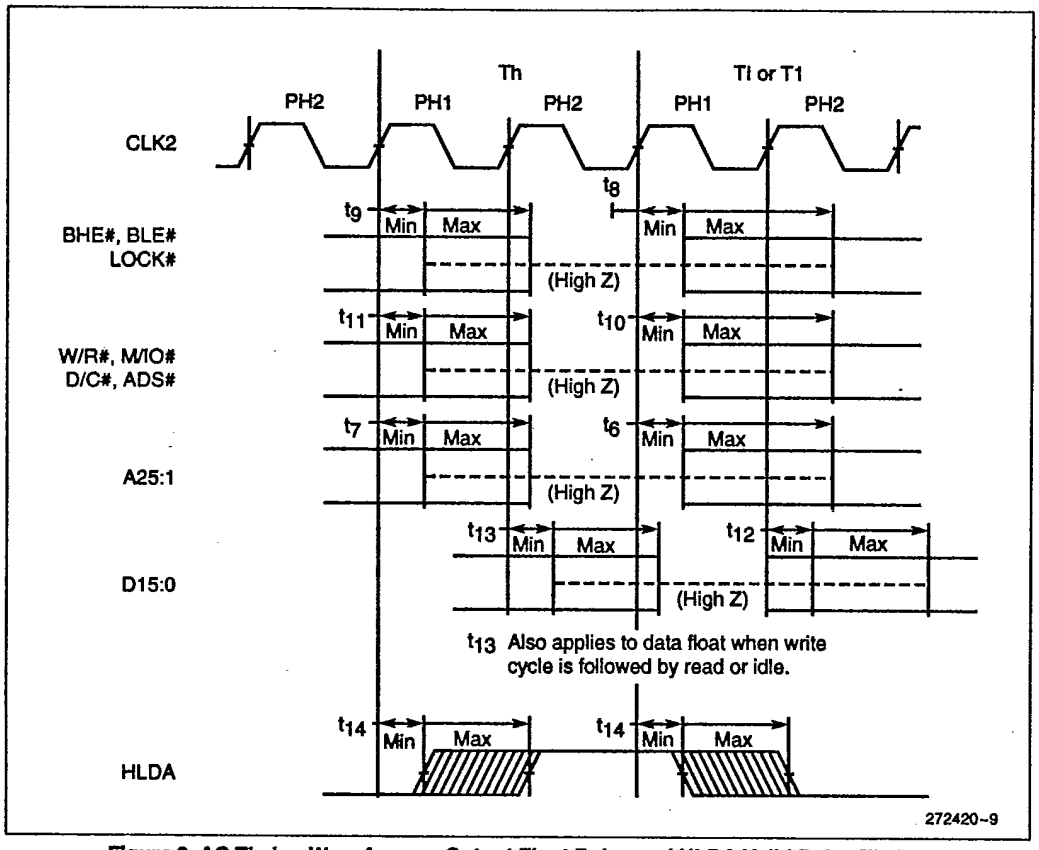


**Figure 9. AC Timing Waveforms—Output Float Delay and HLDA Valid Delay Timing**

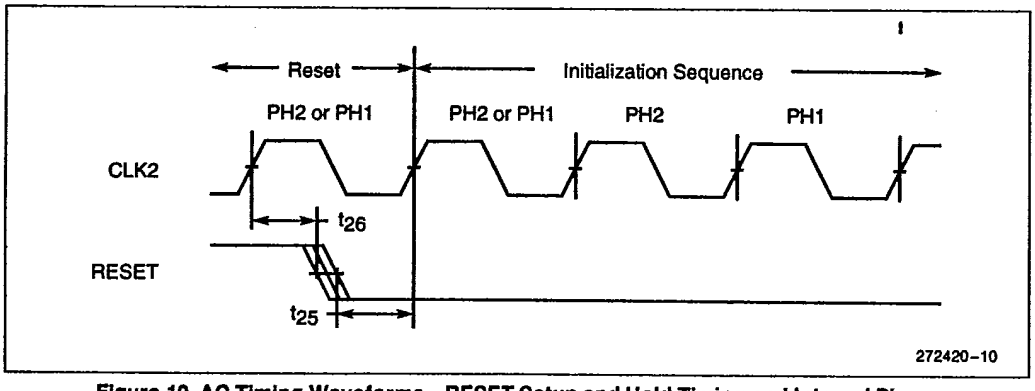


**Figure 10. AC Timing Waveforms—RESET Setup and Hold Timing and Internal Phase**