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DX-SMART

DX-LR02-433T22D

Module Technical Manual

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深圳大疆无线科技有限公司

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Update Record

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V1.0	2024/01/11	Initial release	SML
V1.1	2024/03/01	Optimizing RF parameters	SML

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1. Module Introduction

1.1. Overview

DX-LR02-433T22D is a low-power LoRa module designed by Shenzhen Daxia Longque Technology Co., Ltd. for intelligent wireless data transmission. Built with domestic ASR6601 SOC chip, the chip integrates SUb 1GHz RF transceiver, Arm China STAR-MC1 microprocessor, built-in Flash storage, SRAM. This module supports UART, I2C, I2S and other interfaces, supports IO port control, ADC acquisition, and has the advantages of low power consumption, high performance, long distance, networking, etc. It is suitable for a variety of application scenarios in the IoT field, such as smart meters, smart logistics, smart buildings, smart cities, smart agriculture and many other application scenarios.

1.2. Features

ÿ ASR6601 SOC chipÿ Arm China
STAR-MC1 architectureÿ 32-bit ARM STAR core,
maximum main frequency 48MHzÿ High-power PA, ultra-large output
power: +22dBmÿ Maximum receiving sensitivity: -138dBmÿ
Support UART, I2C, I2S, LPUART, SSP, QSPI
and other interfacesÿ Support sleep modeÿ External antennaÿ Working voltage: 3.3V-5.5
V (typical value: 5V)ÿ
Support working
frequency range: 150-960MHzÿ Open visual distance can reach
8km (for reference only, the actual distance is subject to
actual measurement)ÿ Urban distance can reach 3.8km (for reference only, the actual distance
is subject to actual measurement)

1.3. Application

ÿ Smart metering ÿ
Smart logistics ÿ
Smart buildings ÿ
Smart cities

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Functional block diagram

The figure below is the functional block diagram of the DX-LR02-433T22D module, which explains its main functions as follows:

ÿ Power supply

ÿ Baseband part

ÿ Memory

ÿ RF part

ÿ Peripheral interface

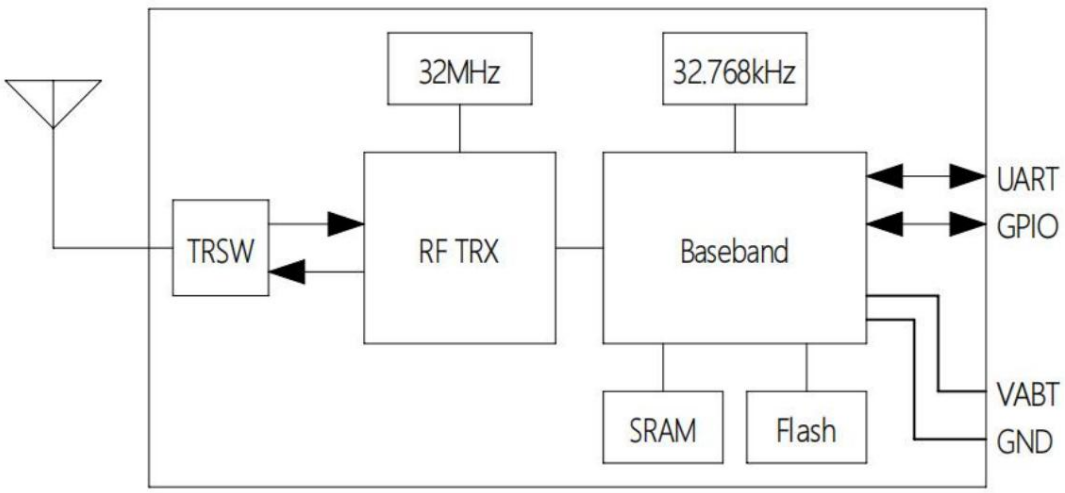

Figure 1: Functional block diagram

1.5. Basic parameters

Table 1: Basic parameter table

Parameter name	Details	Parameter name	Details
Chip Model	ASR6601	Module Model	DX-LR02-433T22D
Modulation	Spread spectrum modulation	Module size: 35.6(L) x 18(W) x 3.2(H) mm	
Operating voltage	3.3V-5.5V	protocol	LoRa Protocol
Sensitivity	-138dBm	Transmit power	0~+22dBm
RF input impedance	50ÿ	Frequency band	433-475MHz
Antenna interface	External Antenna	Hardware Interface	LPUART

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1.6. Transmission method

ÿ Transparent transmission: Data can be transmitted on the same channel between the sender and the receiver

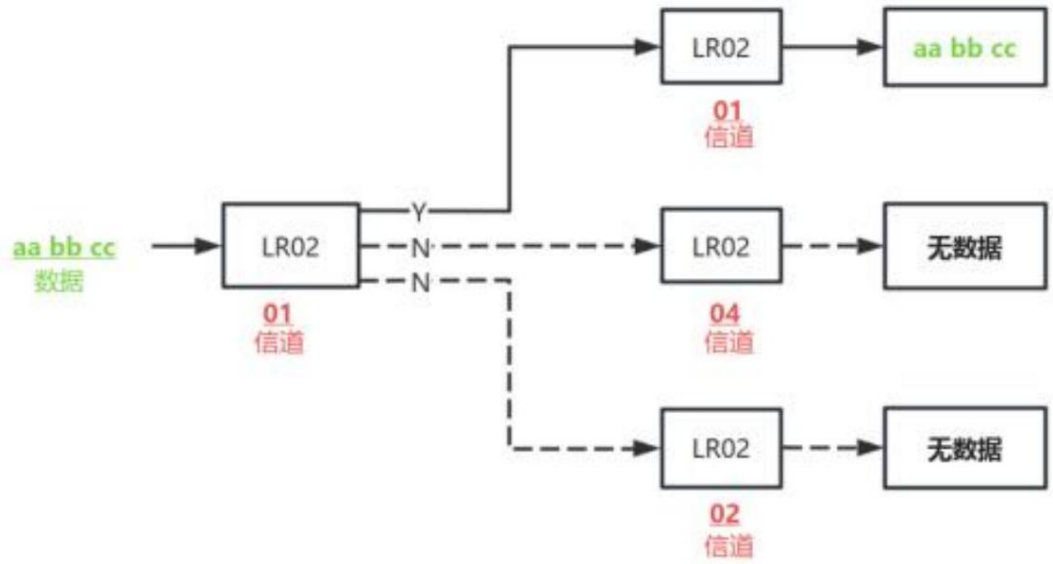

Figure 2: Transparent transmission

ÿ Fixed-point transmission: When the sender sends data, the target address and target channel contained in the data must be the same as the address and channel of the receiver. The data format is as follows: target address (hexadecimal, two bytes) + target channel (hexadecimal, one byte) + data (hexadecimal)

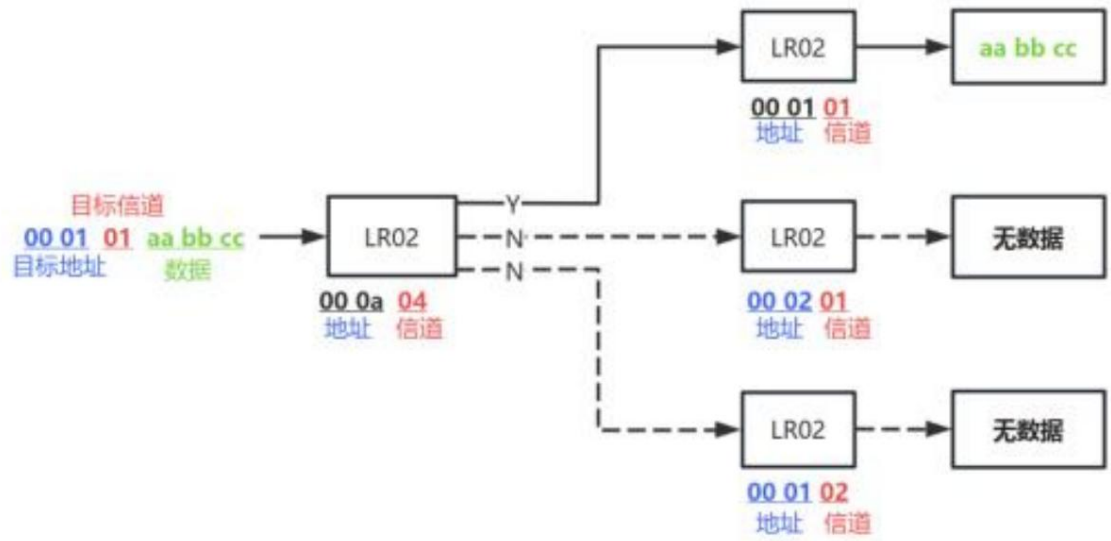

Figure 3: Fixed-point transmission

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ÿ Broadcast transmission: When the sender sends data, the target channel in the data must be the same as the receiving channel.

Data format such as: target channel (one byte, hexadecimal) + data (hexadecimal)

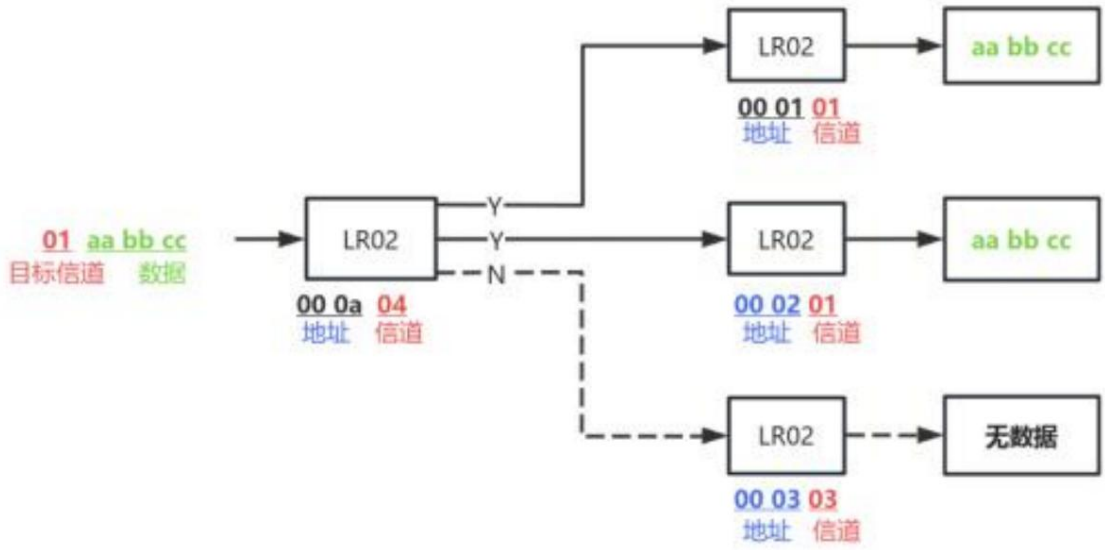

Figure 4: Broadcast transmission

2. Application interface

2.1. Module pin definition

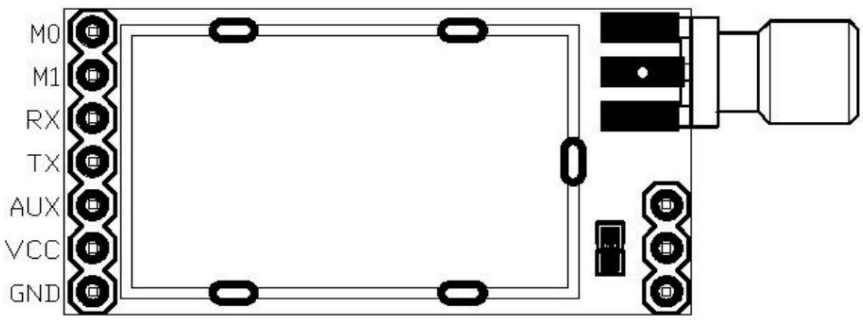

Figure 5: Module pin definition

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2.2. Pin Definition

Table 2: Pin definition table

Pin number	Pin Name	Pin Function	illustrate
1	M0	Reserve	Customizable IO ports
2	M1	Reserve	Customizable IO ports
3	UART_RX	Serial data input	-
4	UART_TX	Serial data output	-
5	AUX	For details on the module's RF status indicator pin, please refer to 2.3.3	
6	VCC	Power input pin	5V (typical)
7	GND	Power Ground	-

2.3. Power supply design

2.3.1. Power interface

Table 3: Power interface pin definition table

Pin Name	Pin Number	describe	Minimum	Typical	Maximum	unit
VCC	6	Module power supply	3.3	5	5.5	V
GND	7	land	-	0	-	V

2.3.2. Power supply stability requirements

The power supply range of DX-LR02-433T22D is 3.3~5.5V. It is necessary to ensure that the input voltage is not less than 3.3V.

VVCC_3V3 voltage drop during input.

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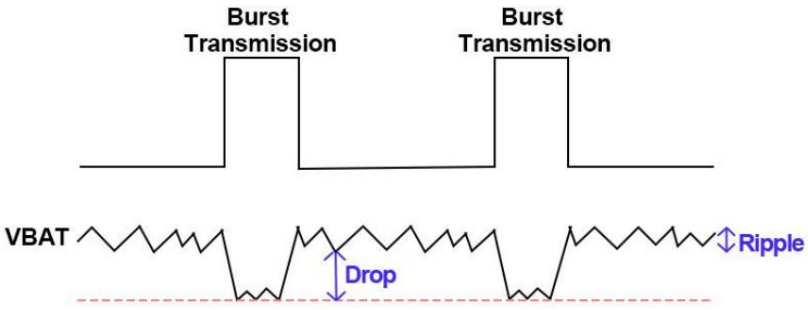

Figure 6: Burst transmission power requirements

In order to reduce voltage drop, it is recommended to reserve 2 (100uF, 0.1uF) multilayer ceramic capacitors with the best ESR performance for VBAT.
(MLCC) and the capacitor is placed close to the VBAT pin.

2.3.3. AUX module RF status indicator pin description

ÿ Low level: The module is currently in the receiving idle state or data transmission idle state, and can send data, or is waiting for a response.
The end module sends data.

ÿ High level: The module is currently in the data receiving or data sending accumulation state, please wait for the pin to become low level.

2.4. Power consumption

ÿ Sleep mode: In this mode, both the MCU and the RF enter sleep mode. Use the serial port to wake up. When waking up, you need to send 4 bytes to
The mode is not written and saved, and a command is used each time it is entered.

ÿ Air wake-up mode: In this mode, the module performs CAD detection in a cycle of four seconds (the overall sleep time is: 4s minus CAD
Detection time), if the module detects data, it will enter the receiving mode, and automatically enter sleep mode after receiving the data. During sleep,
The RF is in sleep mode, but the MCU is not in sleep mode. This mode can be used for writing and saving.

ÿ High time efficiency mode: In this mode, the module is always in receiving state and can receive data from other devices at any time.
When receiving data from the master control, it switches to the transmitting state and sends the data out. After the transmission is completed, it switches back to the receiving state.

Table 4: Power consumption table

Working status	state	Current	Unit
Sleep Mode	Standby	188.47	uA
Air wake-up mode	Standby	4.54	mA
	transmission	45.54	mA
	take over	8.43	mA

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	Standby	12.81	mA
High time efficiency mode	transmission	40.14	mA
	take over	11.81	mA

2.5. Hardware physical interface

2.5.1. General digital IO port

The module defines 20 general-purpose digital IO ports. All of these IO ports can be configured through software to achieve various functions, such as buttons Control, LED drive or interrupt signal of main controller, etc. Keep it floating when not in use.

2.5.2. I2C Interface

ASR6601 includes an I2C master mode, supports standard rate mode (100Kbps) and fast mode (400Kbps), and supports multiple Host and bus arbitration function. SDA is the data transmission line and SCL is the reference clock line.

When the software starts to perform a read or write operation, I2C switches from the default slave receive mode to the master transmit mode. The Start condition is followed by After receiving ACK, I2C enters one of the following two modes: Master Transmit Mode - Write Data, Host receive mode - read data.

The CPU writes the I2Cx_CR register to start a host transaction. The FIFO mode can only be used in the host mode. For transmit and receive, to help reduce I2Cx_DBR register empty and full interrupts, FIFO allows reading and writing multiple bytes without the need Interrupts the CPU after each byte operation.

Figure 8 shows the I2C timing diagram, which is the same as the I2C slave timing diagram.

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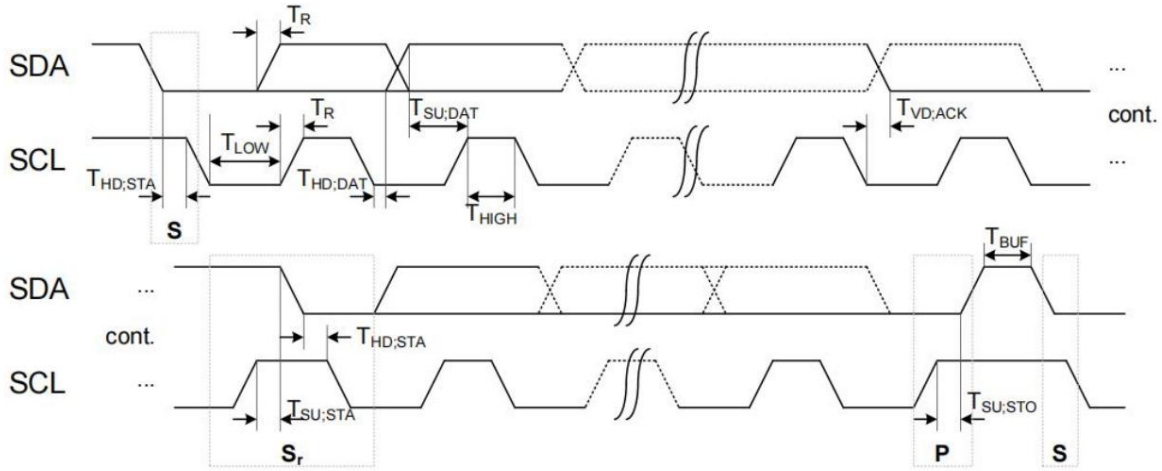

Figure 7: IIC communication timing diagram

The ASR6601 also includes an I2C slave mode that supports standard rate mode (100Kbps) and fast mode (400Kbps).

The slave reception is the default mode, I2Cx_CR{UE} must be set to 1, and I2C monitors the Start condition on the bus. If the Start condition is detected, the interface reads the first 8 bits of data and compares the first 7 bits with its own slave address. If they match, it responds to ACK. If the 8th bit (R/nW) of the first byte is low, then I2C remains in the slave reception mode and clears I2Cx_SR{SAD} to 0. If R/nW is high, I2C switches to the slave transmission mode and sets I2Cx_SR{SAD} to 1.

As a receiving slave, I2C pulls the SDA line low when SCL is high to generate ACK and sends it to the master.

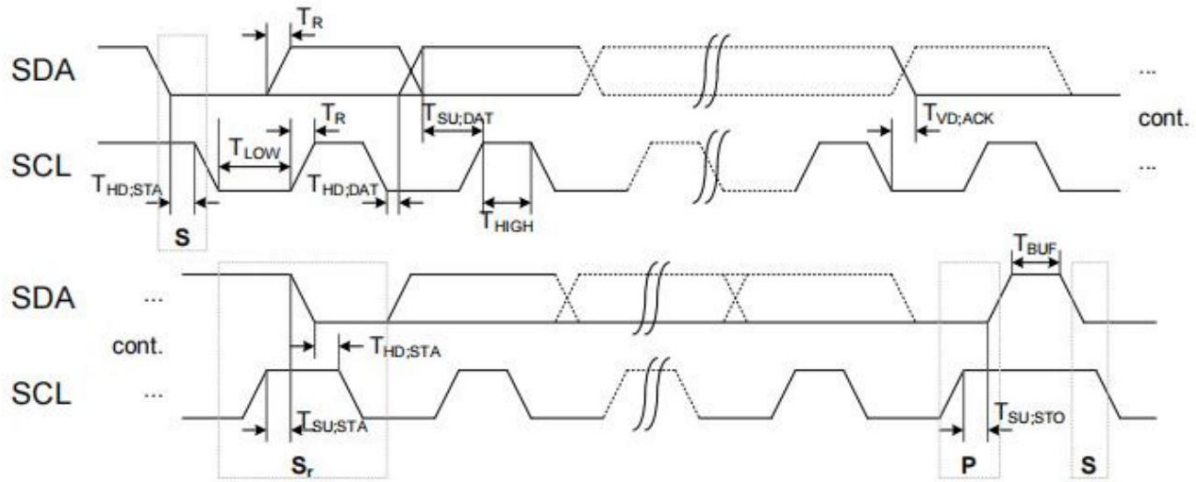

Figure 8: I2C slave timing diagram

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2.5.3. UART Interface

ASR6601 supports UART and IrDA modes. The transmit and receive FIFOs are independent, with 16-bit baud rate divisor integer part and 6-bit baud rate Divisor decimal part. Standard asynchronous communication bit, support 5, 6, 7 and 8-bit data, support parity check, support 1 or 2 stop bits. Support DMA, support false start bit detection, support Line Break generation and detection, support hardware flow control. Each UART port can be uniquely identified through the ID register.

The frequency of UARTCLK must meet the requirements of baud rate generation: FUARTCLK(min)>=16 x baudrate(max), FUARTCLK(max)<=16 x 65535 x baudrate(min) .

For example, to generate baud rates between 110 and 460800, the UARTCLK frequency must be between 7.3728MHz and 115.34MHz.

At the same time, UARTCLK cannot be greater than 5/3 times PCLK: FUARTCLK<=5/3 * FPCLK.

The transmit and receive FIFOs are independent and can be turned on or off by the line control register UARTx_LCR_H{FEN}. Transmit 16 x 8, receive 16 x 12, receive FIFO has a 4-bit status code for each character, and the FIFO water level can be configured to 1/8, 1/4, 1/2, 3/4 and 7/8 through the FIFO interrupt water level selection register UARTx_IFLS. When the FIFO is disabled, it is equivalent to a depth of 1. The FIFO status is obtained by querying the flag register UARTx_FR.

The IrDA SIR ENDEC provides the function of converting between the UART data stream and the half-duplex serial SIR interface, converting the data from the UART to the Code output and decode input to UART, there are two modes:

In IrDA mode, a logic 0 level is converted to a high level pulse with a width of 3/16 of the nSIROUT baud rate bit period, and a logic 1 level is converted to a high level pulse with a width of 3/16 of the nSIROUT baud rate bit period. level is converted to a low level.

In Low-Power IrDA mode, the high-level pulse width sent is 3 times the internal IrLPBaud16 cycle (1.63us, assuming the nominal frequency is 1.842MHz). The IrDA SIR physical layer is a half-duplex communication link, and the switching between sending and receiving must maintain a delay of at least 10ms. This delay must be completed by software because UART does not support automatic delay.

The following figure shows the effect of IrDA 3/16 data modulation:

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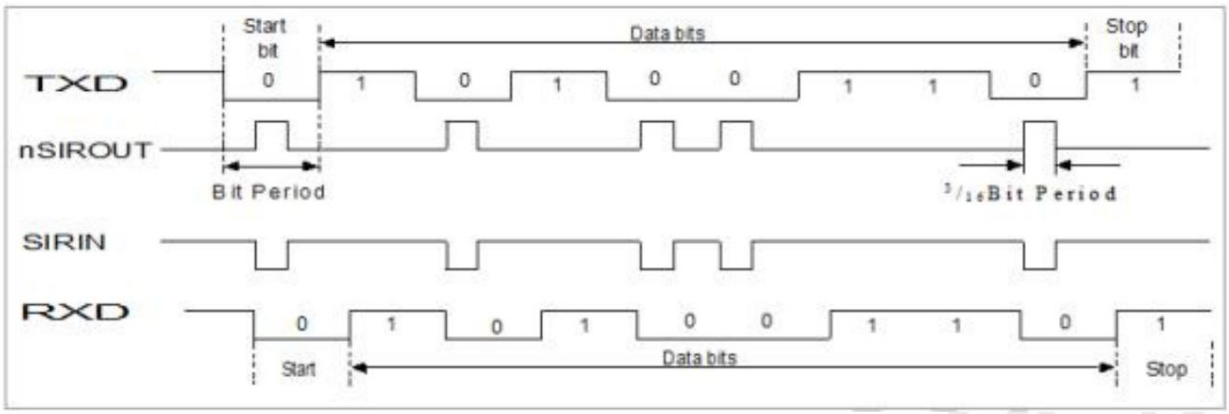

Figure 9: IrDA data control

Enable UART through UARTx_CR{UARTEN}, and configure data bit, stop bit, parity through line control register UARTx_LCR_H Check parameters etc.

When the receiver is idle, UARTRXD is pulled low, the Baud16 enabled receive counter starts counting, and the UART mode starts sampling at the 8th counting cycle. The IrDA mode starts sampling at the 4th counting cycle to allow for shorter logic 0 pulses.

If UARTRXD remains low in the 8th counting cycle, then a valid start bit is detected, otherwise it is judged as a false start and and is ignored.

If the start bit is valid, data sampling will be performed every 16 Baud16 cycles, and the length is determined by UARTx_LCR_H{WLEN}. If parity checking is enabled, a parity bit comparison will be performed.

Finally, when UARTRXD goes high, a valid stop bit is recognized, otherwise a frame error occurs. The complete received character is stored in the receive FIFO along with the error bit.

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2.5.4. SSP Interface

ASR6601 supports SSP interface, which is a synchronous serial interface that supports MASTER and SLAVE modes. It supports multiple frame formats. The data width and output rate can be configured as needed, with a maximum output of 16MHz and 16-bit wide and 8-bit deep TX/RX FIFOs.

SSP mainly has 4 pins: SSP_NSS, SSP_CLK, SSP_TX and SSP_RX.

ÿ SSP_NSS: SSP chip select signal, low effective. ÿ

SSP_CLK: SSP clock signal, clock output for MASTER mode, clock input for SLAVE mode. ÿ SSP_TX: SSP transmit signal, whether in MASTER mode or SLAVE mode, it is the transmit pin. ÿ SSP_RX: SSP receive signal, whether in MASTER mode or SLAVE mode, it is the receive pin.

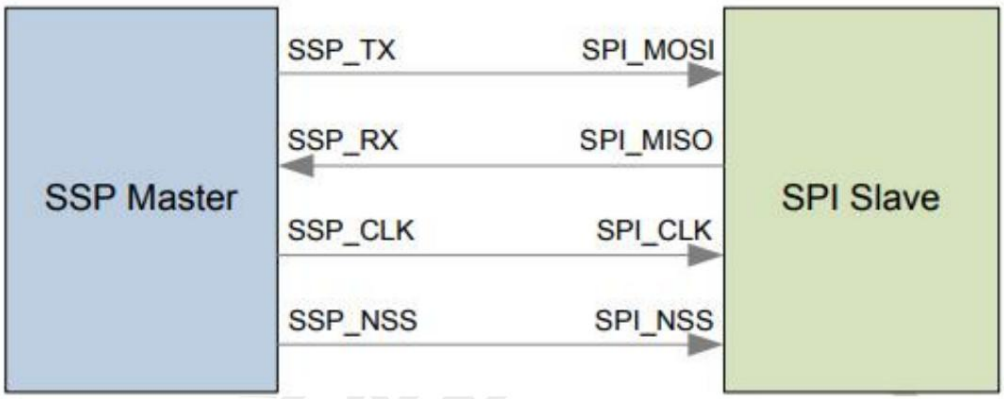

Figure 10: Connection between SSP master and SPI slave

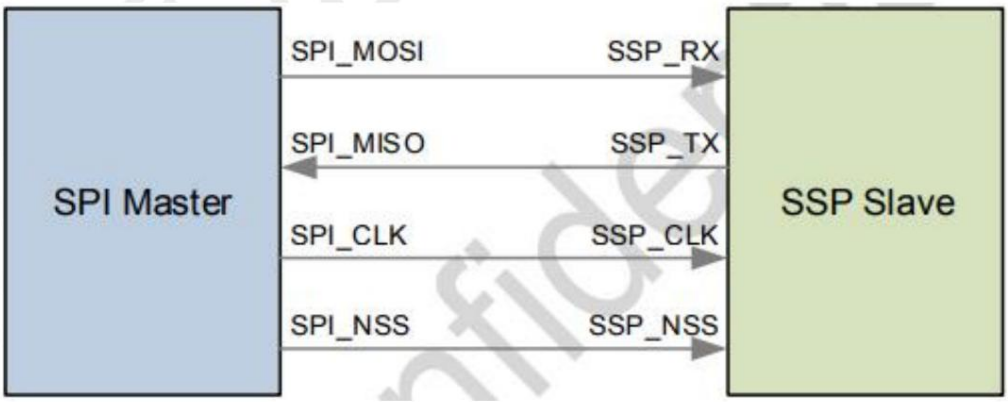

Figure 11: Connection between SPI slave and SSP master

SSP clock constraints:

ÿ The maximum supported output clock is 16MHz

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ÿ In MASTER mode, the maximum clock is 1/2 of PCLK ÿ In SLAVE

mode, the maximum clock is 1/12 of PCLK

SSPCLK is the interface clock of SSP, and SSPCLKOUT is the output clock of SSP. Taking the default 24MHz as an example, if you want to output For a 1MHz clock, set CPSDVR to 2 and SCR to 11.

2.5.5. LPUART

ASR6601 includes LPUART interface, which is a low-power serial port peripheral that supports baud rate up to 9600 at 32K clock. In ultra-low power mode, LPUART can also be awakened by received data. LPUART supports CTS/RTS flow control and DMA request.

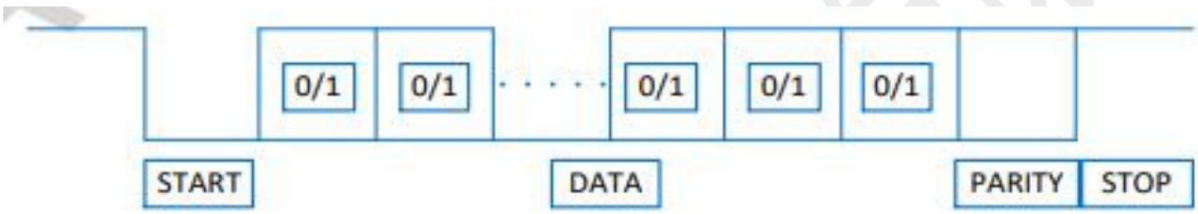

Figure 12: LPUART data transmission format

When idle, the data line of LPUART should be kept at a high level. During data transmission, the start bit (START), data bit (DATA), parity bit (PARITY) and stop bit (STOP) are transmitted in sequence.

The meaning of each bit is as follows:

ÿ Start bit: A 0 signal is sent first to indicate the start of data transmission. ÿ Data bit:

According to the configuration, 5-8 bits are transmitted in sequence. ÿ

Parity bit: After the data bit, a parity bit of one bit is transmitted, which can also be configured as no parity bit. ÿ Stop bit: The sign of the

end of data transmission, which can be 1 or 2 bits.

The configuration of LPUART baud rate supports fractional division, which is mainly configured through two registers: LPUART_BAUD_RATE_INT and LPUART_BAUD_RATE_FRA. Taking the LPUART interface clock frequency of 32.768KHz and the baud rate of 9600 as an example, the division coefficient is 32768/9600=3.413, then the register LPUART_BAUD_RATE_INT is configured to 3, and the register LPUART_BAUD_RATE_FRA is configured to 7 (0.413*16=6.608, rounded to 7).

The connection between two LPUARTs is as follows:

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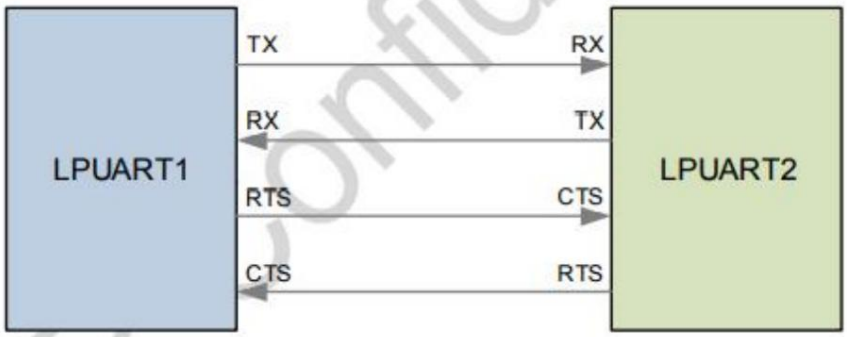

Figure 13: Connection between two LPUART devices

RTS is an output signal, which indicates that the device is ready to receive data. Low level is effective, which means that the device can receive data. CTS is an input signal, which is used to determine whether data can be sent to the other party. Low level is effective, which means that the device can send data to the other party.

The low power wake-up of LPUART includes RX low level wake-up, valid START wake-up, and RX_DONE wake-up.

The wake-up mode is enabled by using the LPUART_WAKEUP_EN bit in the LPUART_CR0 register.

2.5.6. Analog-to-Digital Converter (ADC)

ADC is a 12-bit analog-to-digital converter, which supports 8 external channels and 7 internal channels. The internal channels can collect VBAT/3 and support a maximum sampling rate of 1M. It supports single-ended and differential modes, with a single-ended range of 0.1V~1.1V and a differential range of -1.0~1.0V. It can configure 16 sampling sequences and support continuous, single, and non-continuous sampling modes. It supports software triggering and hardware triggering, and the trigger source can be configured. It supports DMA requests and interrupt requests.

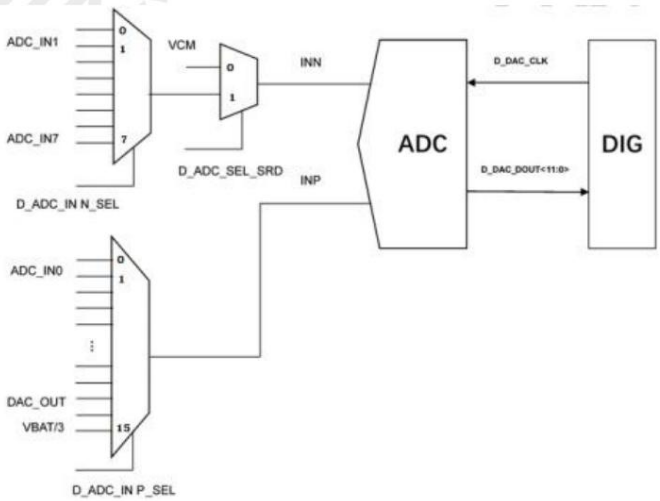

Figure 14: ADC block diagram

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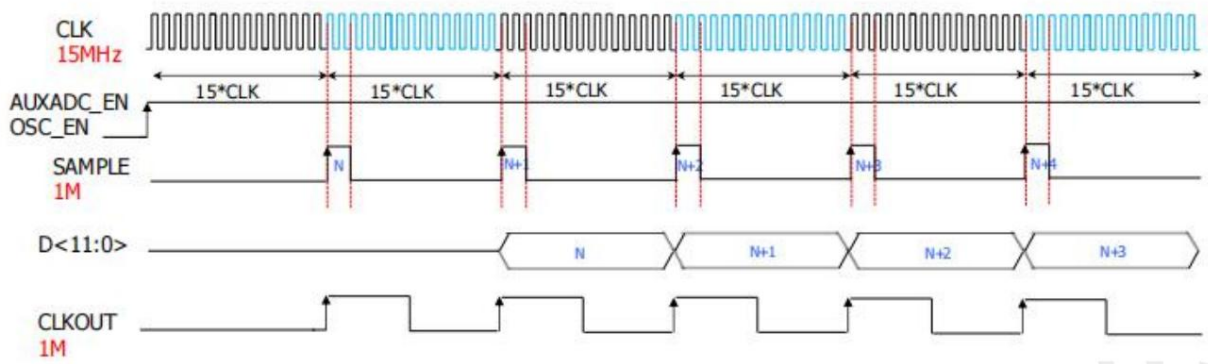

Figure 15: 12-bit ADC timing diagram

Supports configuration in single-ended and differential modes. External channels support single-ended and differential modes, while internal channels only support single-ended mode. Differential is fixed Combination, does not support random pairing, where 0/1 channels are a group, 2/3 channels are a group, 4/5 channels are a group, and 6/7 channels are a group. Single-ended and differential are controlled differently only in the sampling phase, and there is no difference in the holding phase. In the final data, the highest bit of the differential input is the sign bit (11bit data bit, 1 sign bit), and the single-ended input is 12bit data bit, without a sign bit. The input mode is configured through the sampling channel differential/single-ended selection register ADC_DIFFSEL.

Configure the sampling mode through ADC_CFGR{CONV_MODE}: support sampling sequence configuration, sampling sequence up to 16 channels, single-ended Both differential and differential channels can be configured. In differential mode, the sampling sequence only needs to configure the P terminal. The sampling channel can repeatedly configure the same channel to determine the channel to be sampled multiple times each time. The sampling sequence is configured through the channel sampling sequence control registers ADC_SEQR0 and ADC_SEQR1. Every 4 bits configure 1 sampling channel. Two 32-bit registers have a total of 64 bits, and up to 16 sampling channels can be configured.

ÿ Continuous sampling: Once the trigger is valid, the selected input sequence will be continuously converted. After each cycle is completed, a new cycle will automatically start until the software is configured to stop. ÿ Single sampling: Each trigger executes a sampling sequence cycle, and the sampling is automatically terminated after completion. ÿ Discontinuous sampling: Each ADC conversion in the sequence requires a hardware or software trigger. If a sequence is completed and triggered again, the ADC will be converted again. Starts from the beginning of the sequence; in Continuous and Single modes, each trigger completes a full sequence.

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2.6. Reference connection circuit

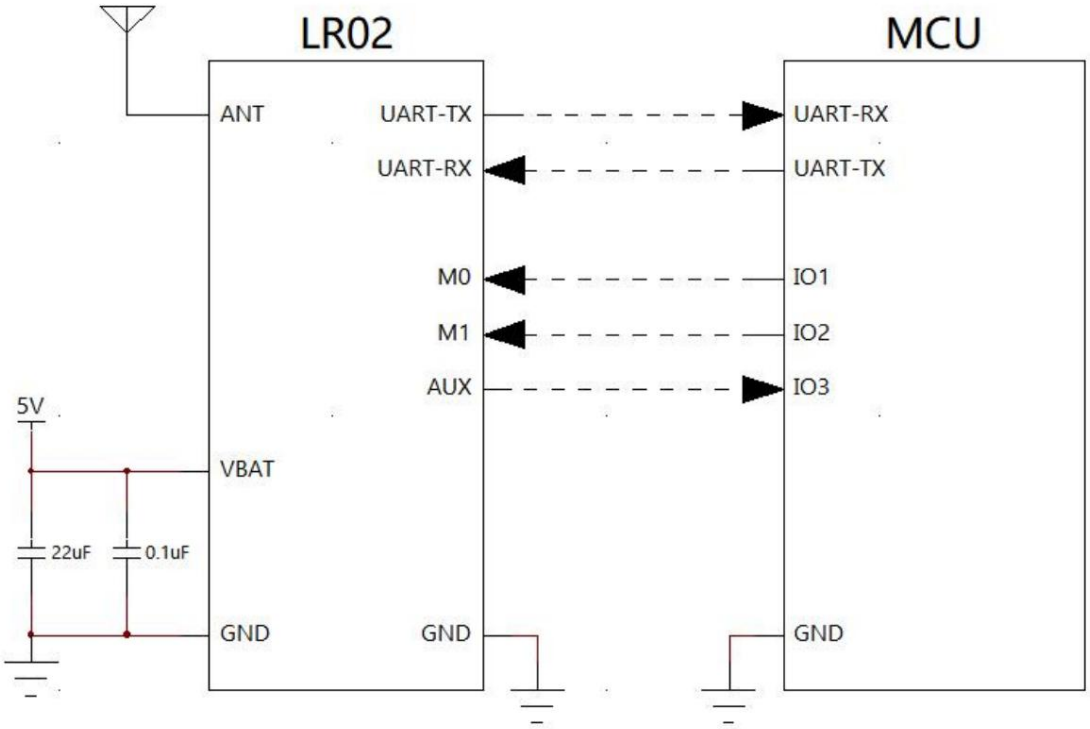

Figure 16: Typical application circuit

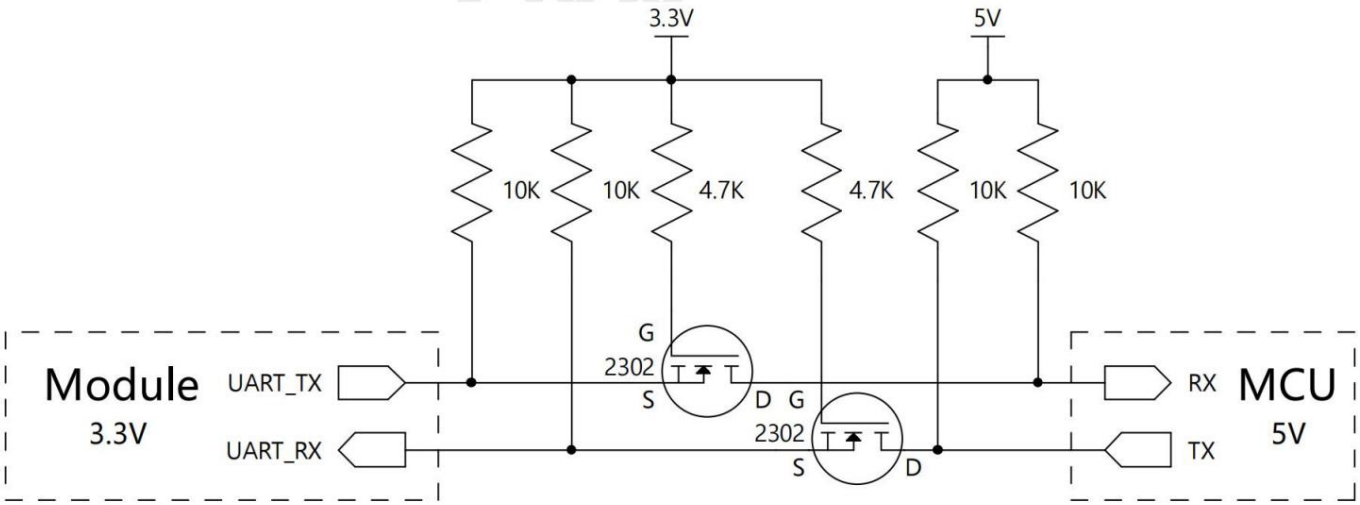

Figure 17: Serial port level conversion reference circuit

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3. Electrical characteristics, RF characteristics and reliability

3.1. Maximum ratings

Stresses exceeding the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and do not imply that the device Functional operation at these or any other conditions beyond those indicated in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may May affect the reliability of the equipment.

Table 5: Absolute Maximum Ratings Table

parameter	Minimum	Maximum	unit
VBAT	-0.2	5.5	V
I/O supply voltage (VDDIO)	-0.2	3.7	V
Storage temperature range	-40	+125	°C

Table 6: Recommended operating conditions

parameter	Minimum	Typical Value	Maximum	unit
VBAT	3.3	5	5.5	V
I/O supply voltage (VDDIO)	3	3.3	3.7	V
Operating temperature range (TA)	-40	+25	+85	ÿ

3.2. Electrostatic protection

In module applications, static electricity generated by human static electricity, charged friction between microelectronics, etc., is discharged to the module through various channels, which may The module may be damaged to a certain extent, so ESD protection should be taken seriously.

For example, ESD protection measures should be taken at the interfaces of circuit design and points that are susceptible to damage or impact from electrostatic discharge. Static electricity protection, anti-static gloves should be worn during production.

Table 7: ESD withstand voltage of module pins

Test interface	Contact discharge	Air discharge	unit
VBAT and GND	+4	+8	kV
Main antenna interface	+2.5	+4	kV

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4. Mechanical dimensions and layout recommendations

4.1. Module mechanical dimensions

This section describes the mechanical dimensions of the module. All dimensions are in millimeters. For all dimensions without tolerance, the tolerance is ±0.3 mm.

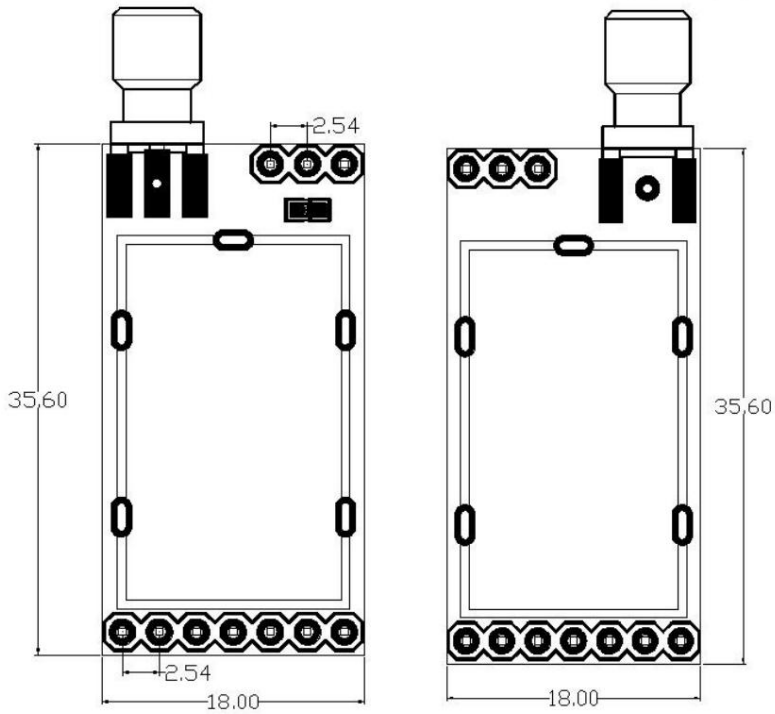

Figure 18: Top and bottom views of recommended package dimensions

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4.2. Module top view/bottom view

Figure 19: Module top and bottom views

Remark:

The above picture is for reference only. For the actual product appearance and label information, please refer to the actual module.

4.3. Hardware Design Layout Recommendations

The DX-LR02-433T22D module works in the SUB-G wireless band and uses an external antenna. The antenna's VSWR and efficiency

Depending on the patch location, various factors that may affect the wireless transceiver signal should be avoided as much as possible. Note the following points:

1. Avoid using metal for the product shell surrounding the LR02-433T22D. When using a partial metal shell, try to keep the module antenna part

Keep away from metal parts. The metal connecting wires or metal screws inside the product should be kept as far away from the module antenna as possible.

2. The module antenna should be placed close to the edge of the PCB or directly exposed from the PCB. Try not to place it in the middle of the board.

3. It is recommended to use insulating materials to isolate the module mounting position on the substrate, such as placing a whole piece of silk screen at this position.

(TopOverLay).

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5. Storage and packaging

5.1. Storage conditions

The module is shipped in a vacuum sealed bag. The module has a moisture sensitivity level of 3 (MSL 3) and its storage must comply with the following conditions:

1. Recommended storage conditions: temperature 23±5°C and relative humidity 35~60%.

2. Under recommended storage conditions, modules can be stored in vacuum sealed bags for 12 months.

3. Under workshop conditions with a temperature of 23±5°C and relative humidity below 60%, the workshop life of the module after unpacking is 168 hours.

Under these conditions, the module can be directly subjected to reflow production or other high temperature operations. Otherwise, the module needs to be stored in an environment with a relative humidity of less than 10%. (e.g., moisture-proof cabinet) to keep the module dry.

4. If the module is in the following conditions, it is necessary to pre-bake the module to prevent the module from absorbing moisture and then causing PCB blistering, cracks and delamination after high-temperature soldering:

ÿ Storage temperature and humidity do not meet the recommended storage conditions ÿ After the module is unpacked, it is not produced or stored according to the above 3 ÿ Vacuum packaging leaks, materials are in bulk ÿ Before the module is returned for repair

5.2. Packaging specifications

The DX-LR02-433T22D module is packaged in trays and sealed in vacuum sealed bags with desiccant and humidity

Each carrier tape measures 260*150*21.5 (unit: mm) and contains 20 modules. The specific specifications are as follows:

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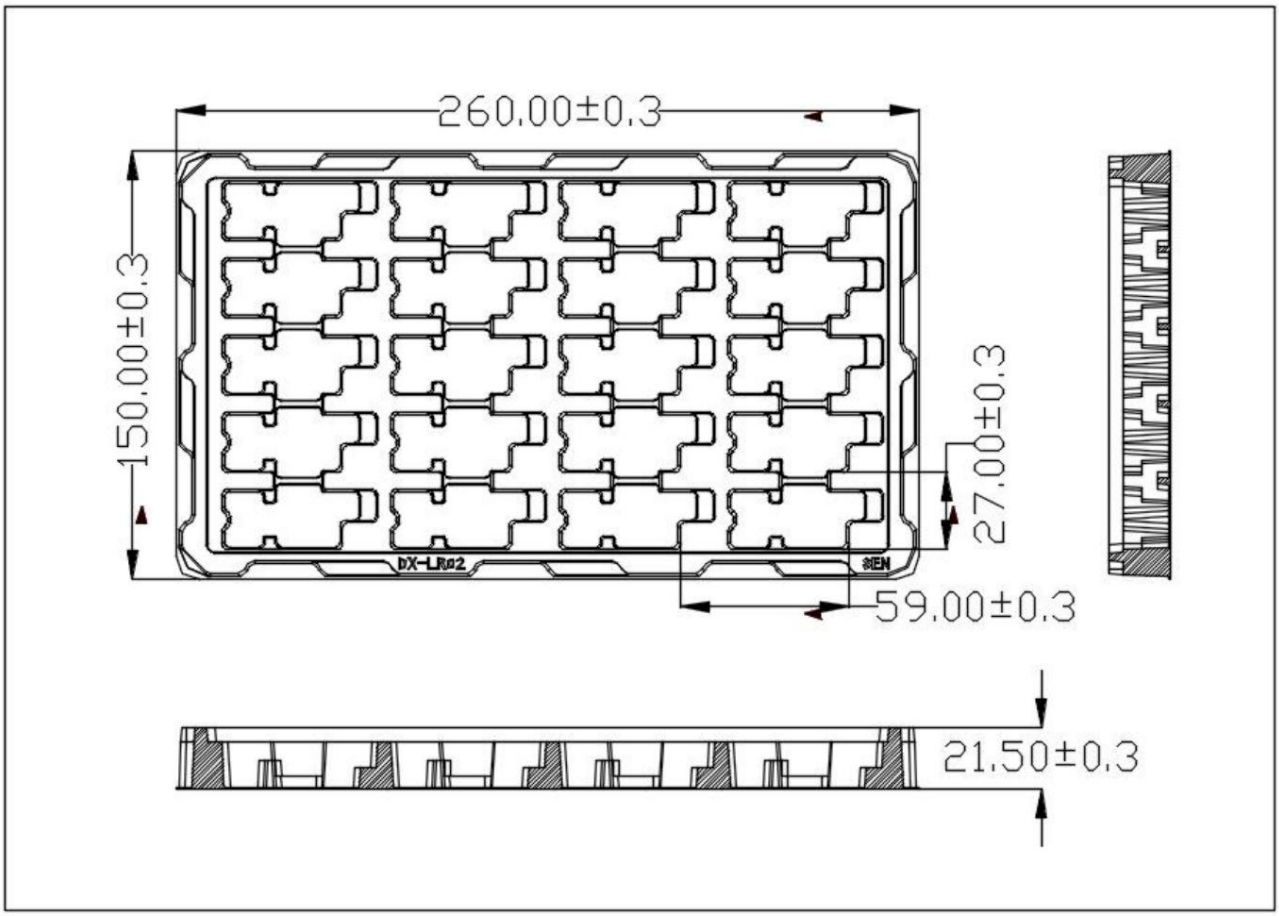

Figure 20: Pallet dimensions (unit: mm)