Review Test Submission: Exam II - Fall 2019

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Course	(MERGED) CS 3340.501 - SE 3340.501 - F19
Test	Exam II - Fall 2019
Started	10/31/19 5:36 PM
Submitted	10/31/19 6:56 PM
Status	Completed
Comments	Very good, keep it up!
Attempt Score	83.5 out of 100 points
Time Elapsed	1 hour, 20 minutes out of 1 hour and 20 minutes
Instructions	• Exam time is 75 minutes, and a 5 mins extension is allowed if needed. A timer will start when the exam begins and expires after 80 minutes. Your work will be auto-submitted when the timer expires. • Only handwriting notes and the MIPS reference card are allowed to use. No other printed materials, no books, no slides! • The use of the simple **software based calculator** available on the Respondus lockdown browser is allowed, but no hardware based calculator can be used! • Multiple answer questions have at least one correct and at least one incorrect answer. **Select all correct answers and avoid incorrect answers, as incorrect answers have a penalty. Do NOT select all answers, no credit will be given if all answers are selected.** • Matching questions also have a **penalty** when an incorrect match was selected. • If a question asks for hexadecimal and '0x' is given do NOT write '0x' in your answer. • Do not omit leading '0's unless specified by the question. • **Read the questions carefully!!!!** • **Good luck!**
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

2 out of 6 points

The last step in the process of translating a program written in a high-level language (e.g. C) into an executable program is called linking. This is done by a system program named **[a]**. There are two types of linking: **[b]** linking and **[c]** linking where an executable program created by the latter type is larger than one created by the former type.

Specified Answer for: a ✓ Linker

Specified Answer for: b ✗ static

Specified Answer for: c ✗ dynamic

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	linker	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	dynamic	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	static	

Question 2

2 out of 5 points

Match the events in a computing system with processor exception types.

Question	Correct Match	Selected Match
The accelerometer detects a rotation of the device.	✓ b. external exception	✓ b. external exception
The network interface receives a messages.	✓ b. external exception	✓ b. external exception
The processor accesses address 0.	✓ d. internal exception.	✗ c. internal trap.
A timer has expired	✓ b. external exception	✓ b. external exception
Overflow.	✓ d. internal exception.	✗ c. internal trap.

All Answer Choices

a. unrecoverable trap

b. external exception

c. internal trap.

d. internal exception.

e. external trap.

Question 3

5 out of 5 points

There are many addressing modes supported by a MIPS processor. Match the way an operand is obtained by the processor with its addressing mode.

Question	Correct Match	Selected Match
The operand is a constant within the instruction itself	a. Immediate addressing	a. Immediate addressing
The operand is the content of a register	b. Register addressing	b. Register addressing
The operand is at the memory location whose address is the sum of a register and a constant in the instruction	c. Base or displacement addressing	c. Base or displacement addressing
The branch destination address is the sum of the PC and a constant in the instruction	d. PC-relative addressing	d. PC-relative addressing
The jump destination address is the 26 bits of the instruction concatenated with the upper bits of the PC and '00'.	g. Pseudodirect addressing	g. Pseudodirect addressing

All Answer Choices

a. Immediate addressing

b. Register addressing

c. Base or displacement addressing

d. PC-relative addressing

e. Direct addressing

f. Indirect addressing

g. Pseudodirect addressing

Question 4

6 out of 6 points

In a computer system, I/O devices are controlled by I/O controller hardware that is abstracted to the processor as three sets of registers: **[a]** registers for asking the I/O device to perform some operations, **[b]** registers for data transfer to/from the device, and **[c]** registers for knowing that an error has occurred.

Specified Answer for: a command

Specified Answer for: b data

Specified Answer for: c status

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	command	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	data	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	status	

Question 5

2 out of 2 points

In a MIPS processor interrupts do not change the flow of control of the processor.

Selected Answer: False

Answers: True

False

Response Feedback: Interrupt IS an exception.

Question 6

2 out of 5 points (Extra Credit)

Write a MIPS assembly code snippet (that can run on MARS, i.e. that must have both data segment and text segment) to calculate the perimeter of a square whose sides' length is stored in a memory word labeled 'SideLen' and store that in another memory word labeled 'Perimeter'.

Selected Answer:

```
.data
SIdeLen: .word 6
Perimeter: .word 0
.text
li  $t1, 0
lw  $t2, SideLen($t1)
sll $t2, 2($t2)
sw $t2, Perimeter($t1)
```

Correct Answer: [None]
Response Feedback: [None Given]

Question 7

0 out of 3 points

Considering the following MIPS assembly code snippet:

```
mydata:  .word 0x01020304, 0x05060708, 0x090A0B0C, 0x0D0E0F10, 1, 2
  ...
  li   $t1, 3
  sll  $t1, $t1, 2
  lb   $s0, mydata($t1)
```

What is the value of register `$s0` after the instruction `lb` was executed? _____

Selected Answer: 6
Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	(0x000000)?0D	
Exact Match	13	
Pattern Match	(0x000000)?10	
Exact Match	16	

Question 8

4.5 out of 6 points

Match each requirement for subroutine call support in a computer system with the feature provided by MIPS to support that requirement.

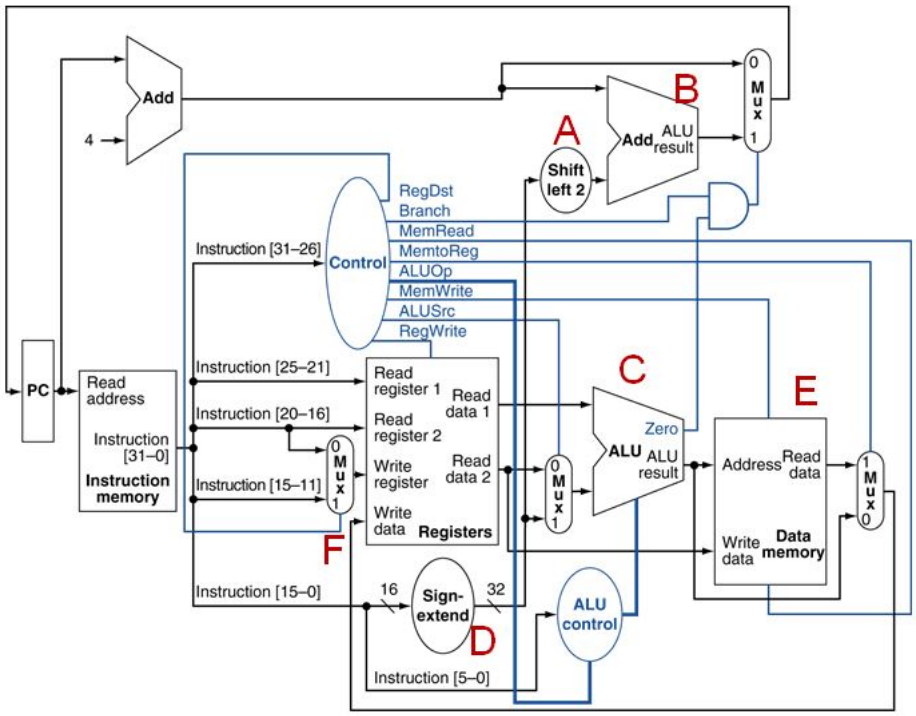
Question	Correct Match	Selected Match
Can pass *arguments* (input) to the subroutine	f. registers $a0, $a1, $a2 and $a3	f. registers $a0, $a1, $a2 and $a3
Can call the subroutine from *anywhere* in the program	i. jal instruction	i. jal instruction
Can always *return back* to the statement just after the subroutine call	b. instruction jr and register $ra	b. instruction jr and register $ra
	d. stack	d. stack
Support *non-leaf (nested)* and *recursive* subroutines		
Preservation of registers	c. register convention	d. stack
Get results from a subroutine call	a. registers $v0 and $v1	a. registers $v0 and $v1

All Answer Choices

a. registers $v0 and $v1
b. instruction jr and register $ra
c. register convention
d. stack
e. j instruction
f. registers $a0, $a1, $a2 and $a3
g. heap
h. global pointer register ($gp)
i. jal instruction

Question 9

4 out of 4 points



The figure above shows the datapath of a MIPS processor with relevant datapath elements are labeled from A to F.

When this processor is executing the `lw $t0, 8($s0)` instruction the **active** datapath elements, in ***alphabetic order***, are **[a]**, **[b]**, **[c]** and **[d]**.

Note: Use only a single letter label in your answers.

Specified Answer for: a C

Specified Answer for: b D

Specified Answer for: c E

Specified Answer for: d F

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	C	Case Sensitive
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	D	Case Sensitive
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	E	Case Sensitive
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	F	Case Sensitive

Question 10

5 out of 5 points

Considering the code of subroutine `sub1` below, fill the blanks to complete it.

```
0x90 sub1:      addi $sp, $sp, [a]  # make room on the stack to save $a0 and $ra
0x94            sw   $a0, 4($sp)    #
0x98            sw   $ra, 0($sp)    #
0x9C            addi $t0, $0, 2
0xA0            slt  $t0, $a0, $t0 #
0xA4            beq  $t0, $0, else #
0xA8            addi $v0, $0, 1    #
0xAC            addi $sp, $sp, [b]   # restore $sp
0xB0            jr   $ra           # return
0xB4      else: addi $a0, $a0, -1  #
0xB8            jal  sub1          #
0xBC            lw   $ra, 0($sp)   # restore $ra
0xC0            lw   $a0, 4($sp)   # restore $a0
0xC4            [c]  $sp, [d], [e] #
0xC8            mul  $v0, $a0, $v0 #
0xCC            jr   $ra           # return
```

There are two types of subroutines: leaf and non-leaf, and the subroutine `sub1` above is a _____ subroutine.

Specified Answer for: a -8

Specified Answer for: b 8

Specified Answer for: c addi

Specified Answer for: d $sp

Specified Answer for: e 8

Correct Answers for: a		
Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	\ *\-8 *	
Correct Answers for: b		
Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	\ *8 *	
Correct Answers for: c		
Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	\ *addi *	
Correct Answers for: d		
Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	\ *\$sp *	
Correct Answers for: e		
Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	\ *8 *	

Question 11

6 out of 6 points

Assuming registers of an 8-bit processor are used to store signed integers represented in the 2's complementary format, and the two 8-bit registers A and B contain 01010011 and 00001101, respectively.

If 8-bit registers H and L are used to store the result of A x B (i.e. C = A multiplied by B), with H and L contain the upper 8 bits and the lower 8 bits of the result respectively, the content of H is **[a]** and that of L is **[b]**.

Note: Answers must be in 2's complementary binary format and do not omit leading 0s. If overflow or underflow happens the answer must be OVF and UDF, respectively.

Specified Answer for: a 00000100

Specified Answer for: b 00110111

Correct Answers for: a		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	00000100	
Correct Answers for: b		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	00110111	

Question 12

2 out of 2 points

Similarly to the MIPS ISA, an instruction word in the ARM ISA has 32 bits and the first field of an instruction word is used to encode the operation of an instruction.

Selected Answer: False

Answers: True
False

Response Feedback: The first field is Opx, not Op.

Question 13

4 out of 4 points

Differences between ARM and MIPS ISAs include

Selected Answers: b. implementation of branching (conditional jumping).
c. number of addressing modes.

Answers: a. data alignment.
b. implementation of branching (conditional jumping).
c. number of addressing modes.
d. address space.

Question 14

4 out of 4 points

When a MIPS processor executes the `sub $s0, $t0, $t1` instruction, overflow may occur if

Selected Answers: b. $t0 contains a positive integer and $t1 contains a negative integer.
d. $t0 contains a negative integer and $t1 contains a positive integer.

Answers: a. both $t0 and $t1 contains a positive integer.
b. $t0 contains a positive integer and $t1 contains a negative integer.
c. both $t0 and $t1 contains a negative integer.

d. $t0 contains a negative integer and $t1 contains a positive integer.

Question 15

4 out of 6 points

The coprocessor_0 in a MIPS processor has a set of registers used to store necessary information when an exception occurs:

$8 BadVaddr

$12 Status

$13 Cause

$14 EPC.

When a MIPS processor executes the following instructions:

Address Instruction

```
0x00401000 li    $t0, 0x7FFFF0F0
0x00401004 lw    $t0, 2($t0)
0x00401008 ...
```

the contents of these registers are:

$8: 0x**[a]**

$13 : 0x**[b]** Note: assuming all Interrupt Pending (IP) bits are 0, i.e. no interrupt pending.

$14: 0x**[c]**.

Specified Answer for: a 7FFFF0F2

Specified Answer for: b 00000010

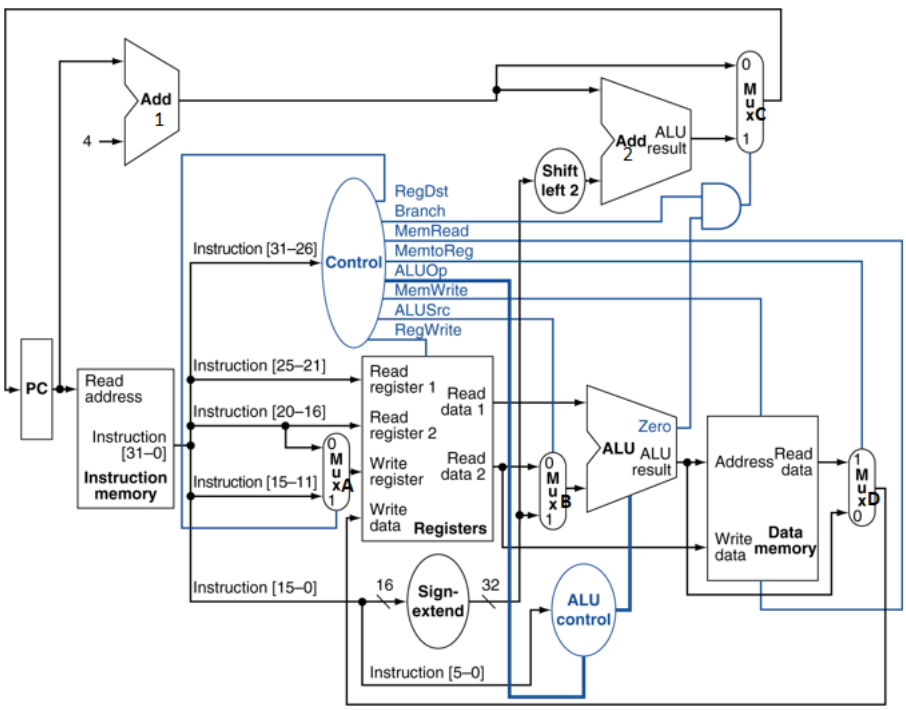
Specified Answer for: c 00401008

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	(?i) *7FFFF0F2 *	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	(?i) *00000010 *	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	(?i) *00401004 *	

Question 16

4 out of 4 points

An (incomplete) datapath of a MIPS processor is shown in the diagram below.



Fill the table below with single character Y or N, with Y indicating that the datapath element is needed when the processor is executing the instruction in the first colum

Instruction being executed	Mux A	Sign-extender	Shift left 2	Mux B	Adder 2	ALU	Data Memory	Mux
beq $t0, $zero, Top	**[ma]**	**[se]**	**[sl]**	**[mb]**	**[a2]**	**[alu]**	**[dm]**	**[mc**

Specified Answer for: ma N
Specified Answer for: se Y
Specified Answer for: sl Y
Specified Answer for: mb Y
Specified Answer for: a2 Y
Specified Answer for: alu Y
Specified Answer for: dm N
Specified Answer for: md N

Correct Answers for: ma

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	n	

Correct Answers for: se

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	

Correct Answers for: sl

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	

Correct Answers for: mb

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	

Correct Answers for: a2

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	

Correct Answers for: alu

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	

Correct Answers for: dm

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	n	

Correct Answers for: md

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	n	

Question 17

4 out of 4 points

Addressing modes supported by a MIPS processor include

Selected Answers:
- a. Register Indirect
- b. Immediate
- d. Register
- f. Displacement.

Answers:
- a. Register Indirect
- b. Immediate
- c. Indirect
- d. Register
- e. Direct
- f. Displacement.

Question 18

3 out of 3 points

In a computer system, **[a]** are **[b]** that happen **[c]** and they require a **[d]** in **[e]** of **[f]**.

Selected Answer: In a computer system, **exceptions** are **events** that happen **unexpectedly** and they require a **change** in **flow** of **control**.

Answers: In a computer system, **exceptions** are **events** that happen **unexpectedly** and they require a **change** in **flow** of **control**.

All Answer Choices

- control
- branchings
- unexpectedly
- flow
- frequently
- change
- abnormal
- events
- exceptions
- frequently
- instructions
- data

Question 19 5 out of 5 points

Match computer components with the most appropriate interconnect elements to connect with an x86 processor.

Question	Correct Match	Selected Match
graphic card	b. north bridge.	b. north bridge.
main memory	b. north bridge.	b. north bridge.
Solid Stated Drive (SSD)	e. south bridge.	e. south bridge.
keyboard	e. south bridge.	e. south bridge.
high speed Network Interface Card (NIC)	e. south bridge.	e. south bridge.

All Answer Choices

a. north side bus.

b. north bridge.

c. processor bus

d. front side bus

e. south bridge.

f. south side bus.

g. memory bus

Question 20 4 out of 4 points

A MIPS assembly language code snippet is shown below.

```
#
# Data segment
#
    .data
const5: .float 5.0
const9: .float 9.0
const32: .float 32.0
x: .float 77.0
y: .float 30.0
#
# Text segment
#
     .text
     lwc1  $f16, const5
     lwc1  $f18, const9
     lwc1  $f6,  const32
     div.s $f2, $f16, $f18
     div.s $f4, $f18, $f16
#
     lwc1 $f10, y
     mul.s $f10, $f10, $f4
     add.s $f12, $f10, $f6
#
# Syscall with $v0=2: Print the floating point number in $f12
#
     li    $v0, 2
     syscall

  #
#     END
#
```

When this code snippet is executed by MARS, the console will display a floating point number which is [a].

Note: only ONE digit after the floating point is needed.

Selected Answer: 86.0

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	86.0	

Question 21

4 out of 4 points

```
#
# data segment
#
            .data
#
x:          .word 16777216
y:          .word 1024
z:          .word 0
#
# program segment
#
             .text
#
             lw $t0, x
             lw $t1, y
             mult $t0, $t1
             mfhi $s0
             sw $s0, z
#
# continue
#
```

After a MIPS processor executes the above MIPS instructions, the content of memory word labeled as z is 0x_____.

Note: Do not omit leading 0s and do not include blanks between hexadecimal digits.

Selected Answer: 00000004

Correct Answer:

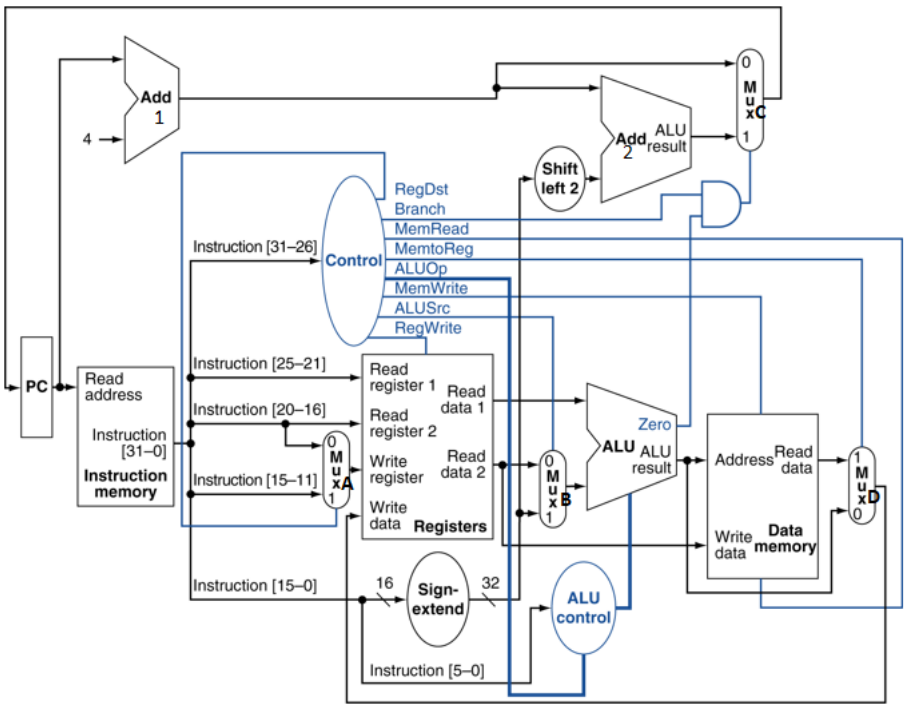
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	00000004	

Question 22

3 out of 4 points

In the datapath of a MIPS processor, multiplexers (MUXes) are used to select one out of multiple input data. The control unit of the processor generates the necessary control signals to select the right input when the processor is executing an instruction.

There are four MUXes (Mux A, Mux B, Mux C, and Mux D) shown in the diagram below.



Fill the table below with the correct value of the control signal of those MUXes when the processor is executing the instruction in the 1st column.

Values of the control signals can be 0, 1 or x. A 0 means the input labeled 0 is selected and x indicating 'does not matter'.

Instruction being executed	Mux A	Mux B	Mux C	Mux D
`add $t0, $zero, $s0`	[ma]	[mb]	[mc]	[md]
`sw $t0, 8($s1)`	[a]	[b]	[c]	[d]

Specified Answer for: ma ✓ 1
Specified Answer for: mb ✓ 0
Specified Answer for: mc ✓ 0
Specified Answer for: md ✓ 0
Specified Answer for: a ✗ 0
Specified Answer for: b ✓ 1
Specified Answer for: c ✓ 0
Specified Answer for: d ✗ 1

Correct Answers for: ma		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	1	
Correct Answers for: mb		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	0	
Correct Answers for: mc		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	0	
Correct Answers for: md		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	0	
Correct Answers for: a		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	x	
Correct Answers for: b		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	1	
Correct Answers for: c		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	0	
Correct Answers for: d		
Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	x	

Question 23

0 out of 4 points

In a MIPS computer system it was determined that the following code:

```
mfc0   $a0, $13     #

srl    $a0, $a0, 2

andi   $a0, $a0, 31 #
```

was executed right after the processor executes the following instructions:

```
li     $t0, 0x7FFFFFFF
addi   $t0, $t0, 2
```

What does register `$a0` contain after the instruction **`andi`** was executed?

Note: the answer must be in decimal.

Selected Answer: ✗ 24
Correct Answer: ✓ 12
Answer range +/- 0 (12 - 12)

Question 24

4 out of 4 points

A MIPS assembly language code snippet is shown below.

```
#
# Data segment
#
    .data
A:  .word  987654321
B:  .word  123

#
# Text segment
#
    .text
    lw $t0, A
    lw $t1, B
    multu $t0, $t1
#
    mfhi $t0

#
#     END
#
```

When this code is executed by MARS, the value of register $t0 in decimal will be [a].

Selected Answer: ✓ 28

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
✓ *Exact Match*	28	

Wednesday, November 13, 2019 9:50:01 PM CST

← OK