Cycle	Instruction Retired	Reason
7	Lbi r0, 0	Write the immediate 0 into r0 in the WB stage. No stall.
8	lbi r5, 43	Write the immediate 43 into r5 in the WB stage. No stall.
9	lbi r6, 43	Write the immediate 43 into r6 in the WB stage. No stall.
10	lbi r7, 43	Write the immediate 43 into r7 in the WB stage. No stall.
11	ld r1, r0, 0	Load MEM[r0 + 0] into r1. No dependency with previous instructions. No stall.
12	NOP	Stalls for one cycle and perform MEM->EX forwarding.
13	st r5, r1, 0	Store r5 in MEM[r1 + 0]. Needs to wait for the ld instruction to update r1 value, stalls for one cycle and then forward r1 data from MEM to EX.
14	ld r1, r0, 2	Load MEM[r0 + 2] in r1. No dependency on previous instructions. No stall.
15	NOP	Stalls for one cycle and perform MEM->EX forwarding.
16	st r6, r1, 1	Store r6 in MEM[r1 + 1]. Needs to wait for the ld instruction to update r1 value, stalls for one cycle and then forward r1 data from MEM to EX.
17	ld r1, r0, 4	Load MEM[r0 + 4] in r1. No dependency on previous instructions. No stall.
18	NOP	Stalls for one cycle and perform MEM->EX forwarding.
19	st r7, r1, 1	Store r7 in MEM[r1 + 1]. Needs to wait for the ld instruction to update r1 value , stalls for one cycle and then forward r1 data from MEM to EX.
20	halt	Stops PC in WB stage.