CSS351 Assignment

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1. Design full adder using half adder.

Theory:

If we draw the truth table of the full adder, we will get:

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

On doing its K-map simplification, we will get:

Sum = (A $\oplus$ B $\oplus$ C)

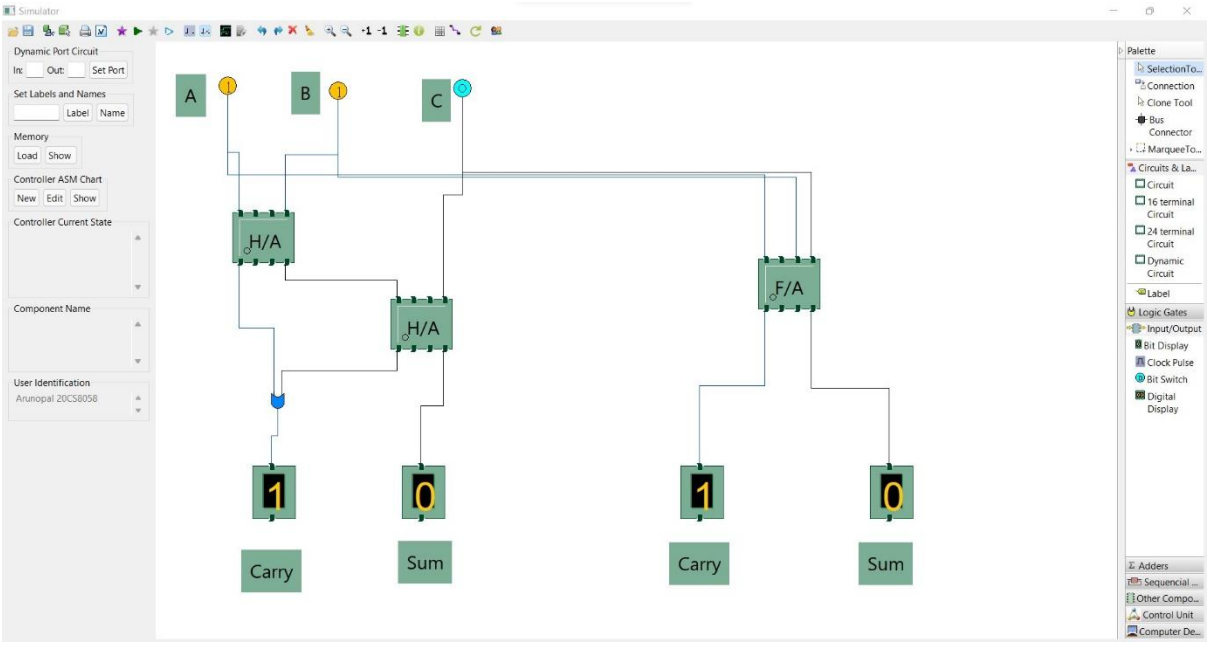
Carry = (A $\oplus$ B).C + A.B

Now for a half adder, we have:

Sum = (A $\oplus$ B)

Carry = A.B

Thus for a full adder, we need 2 half-adders such that, we are adding A and B in one and adding its result with C in 2nd half adder.



2. Design a 4 bit CLA using basic logic gates.

Theory:

In ripple carry adder (RCA) the delay is added from beginning to last. So, the total gate delay increases a lot. To reduce this we will use the Carry Look Ahead Adder (CLA).

If we denote $P_i = A_i \oplus B_i$

and $G_i = A_i \cdot B_i$

We will get sum, $S_i = P_i \oplus C_i$

and carry-out, $C_{i+1} = G_i + P_i \cdot C_i$

Thus, we can derive,

$C_1 = G_0 + P_0 \cdot C_0$

$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0)$

$= G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$

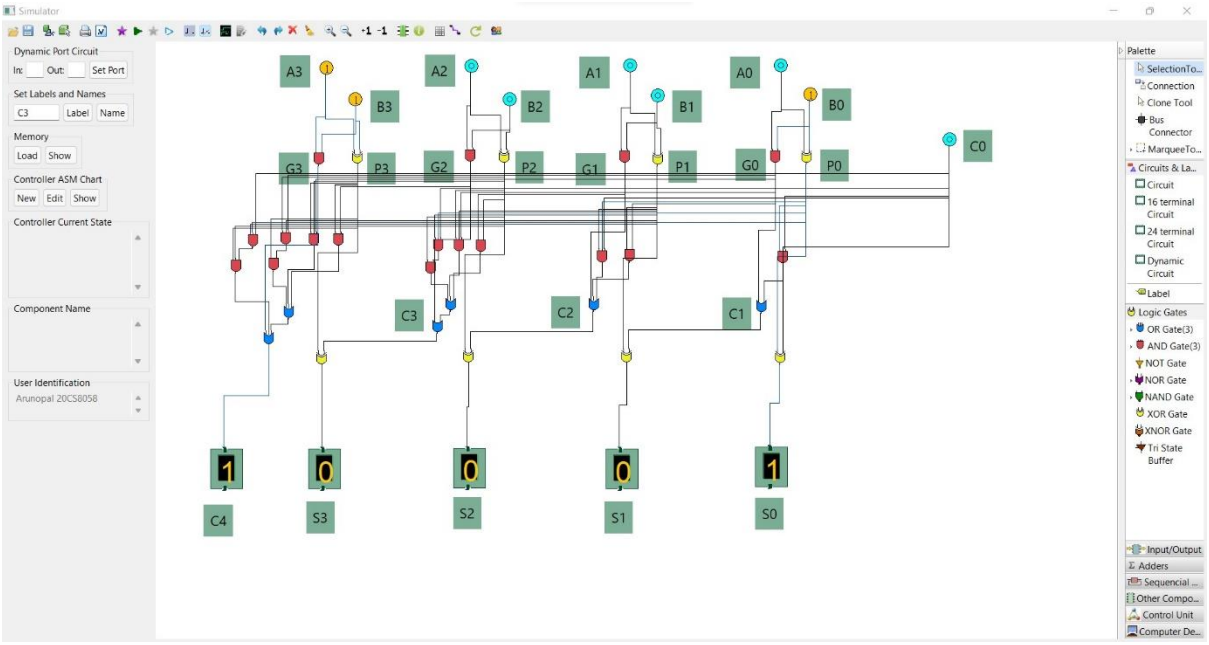
$C_3 = G_2 + P_2 \cdot C_2 = G_2 + P_2 \cdot (G_1 + P_1 \cdot G_0 + P_1 P_0 C_0)$

$= G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$

$C_4 = G_3 + P_3 \cdot C_3 = G_3 + P_3 \cdot (G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0)$

$= G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$

This will significantly reduce the gate delay by making C_4 to be affected by only 2 stages of gate delays, namely, and-gates and or-gates.



3. Convert:

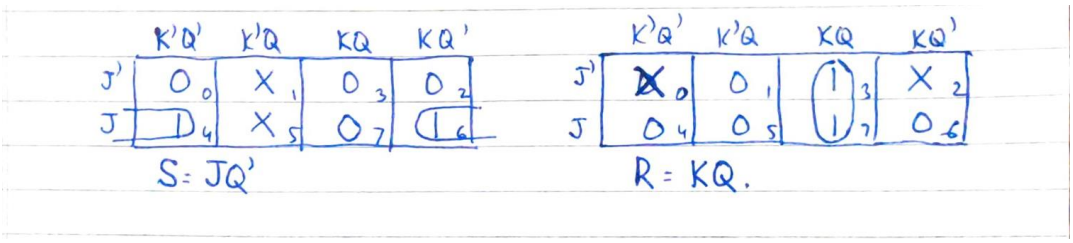
a) SR flip-flop to JK flip-flop.

Truth table:

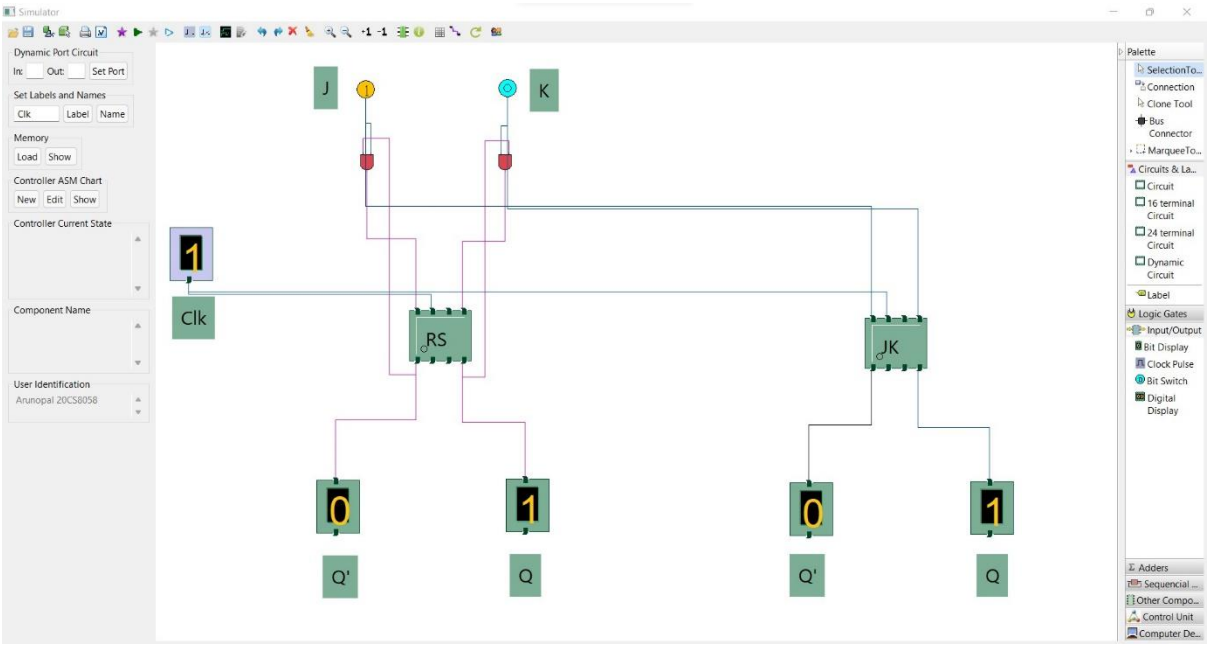
J	K	Q(t)	Q(t+1)	S	R
0	0	0	0	0	X

0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Using K-map we get S = JQ’ and R = KQ.



Simulator:



Waveform:

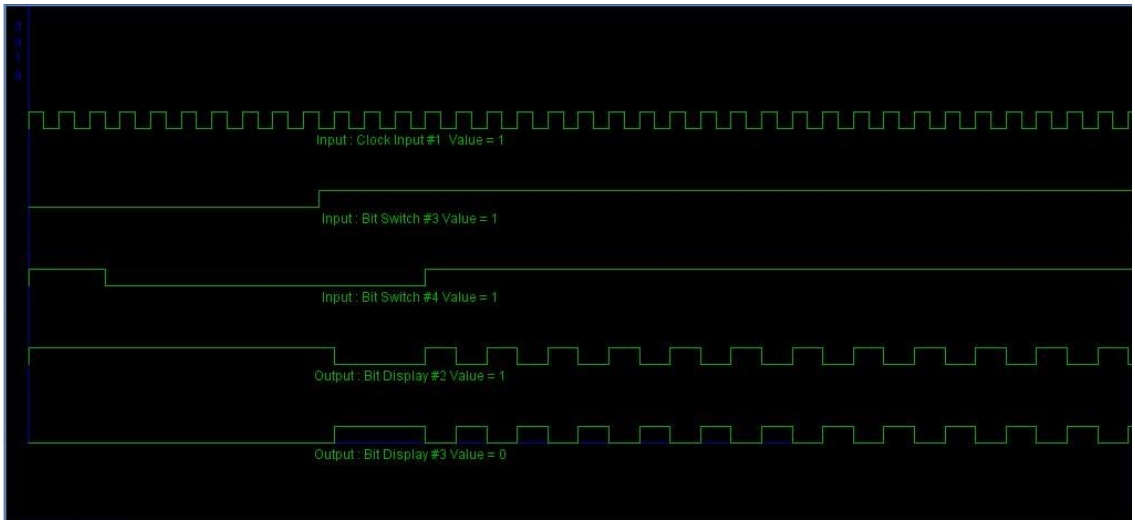
Clk

J

K

Q

Q’

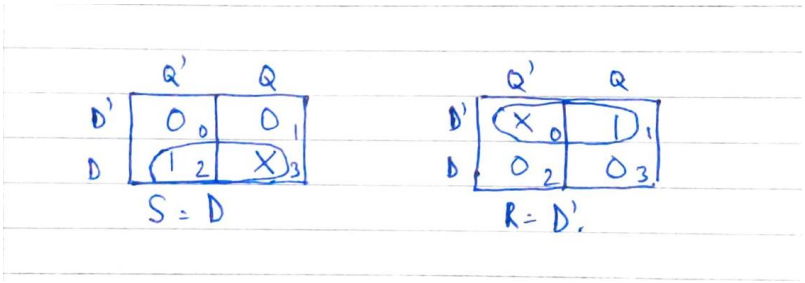


b) SR flip-flop to D flip-flop.

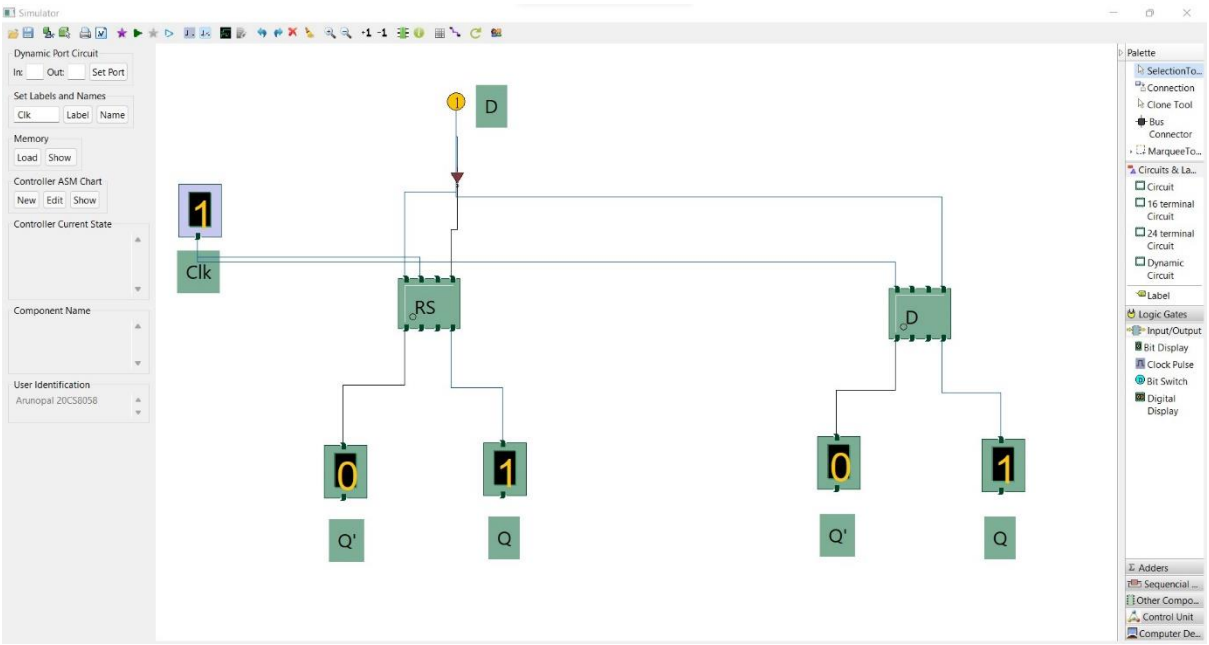
Truth table:

D	Q(t)	Q(t+1)	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

From K-map we get S = D and R = D’.



Simulator:



Waveform:

Clk

D

Q

Q’